Intel386™ SXSA EMBEDDED MICROPROCESSOR

- Static Intel386™ CPU Core
  - Low Power Consumption
  - Operating Power Supply
    4.5V to 5.5V—25 MHz and 33 MHz
    4.75V to 5.25V—40 MHz
  - Operating Frequency
    SA-40 = 40 MHz
    SA-33 = 33 MHz
    SA-25 = 25 MHz
- Clock Freeze Mode Allows Clock Stopping at Any Time
- Full 32-bit Internal Architecture
  - 8-, 16-, 32-bit Data Types
  - 8 General Purpose 32-bit Registers
- Runs Intel386 Architecture Software in a Cost-Effective, 16-bit Hardware Environment
  - Runs Same Applications and Operating Systems as the Intel386 SX and Intel386 DX Processors
  - Object Code Compatible with 8086, 80186, 80286, and Intel386 Processors
- TTL-Compatible Inputs
- High-Performance 16-bit Data Bus
  - Two-Clock Bus Cycles
  - Address Pipelining Allows Use of Slower, Inexpensive Memories
- Integrated Memory Management Unit (MMU)
  - Virtual Memory Support
  - Optional On-Chip Paging
  - 4 Levels of Hardware-Enforced Protection
  - MMU Fully Compatible with Those of the 80286 and Intel386 DX Processors
- Virtual 8086 Mode Allows Execution of 8086 Software in a Protected and Paged System
- Large, Uniform Address Space
  - 16 Megabyte Physical
  - 64 Terabyte Virtual
  - 4 Gigabyte Maximum Segment Size
- Numerics Support with Intel387™ SX and Intel387 SL Math Coprocessors
- On-Chip Debugging Support Including Breakpoint Registers
- Complete System Development Support
- High-Speed CHMOS Technology
- 100-pin Plastic Quad Flatpack Package

3

The Intel386™ SXSA embedded microprocessor is a 5-volt, 32-bit, fully static CPU with a 16-bit external data bus and a 24-bit external address bus. The Intel386 SXSA CPU brings the vast software library of the Intel386 architecture to embedded systems. It provides the performance benefits of 32-bit programming with the cost savings associated with 16-bit hardware systems.

The Intel386 SXSA microprocessor is manufactured on Intel's 0.8-micron CHMOS V process. This process provides high performance and low power consumption for power-sensitive applications. Figure 3 and Figure 4 illustrate the flexibility of low power devices with respect to temperature and frequency relationships.

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December 1994
Order Number: 272419-003

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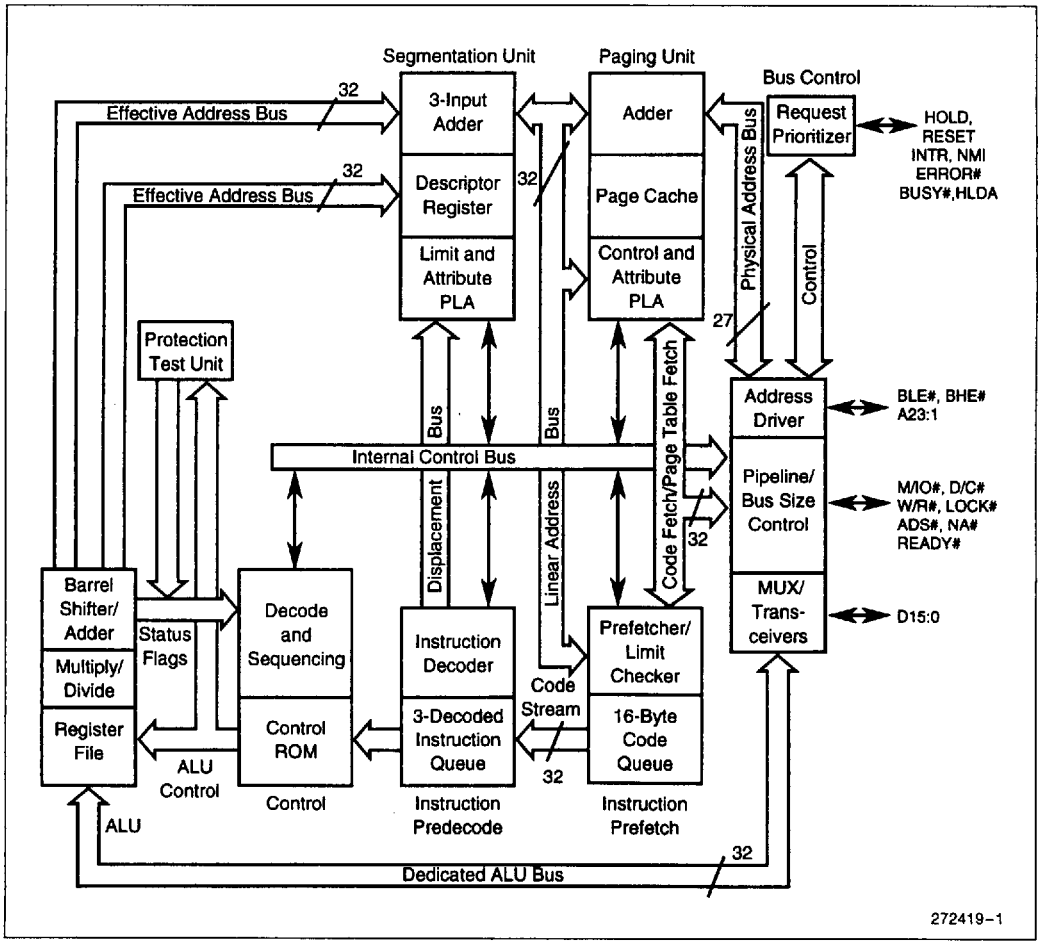

Figure 1. Intel386™ SXSA Microprocessor Block Diagram

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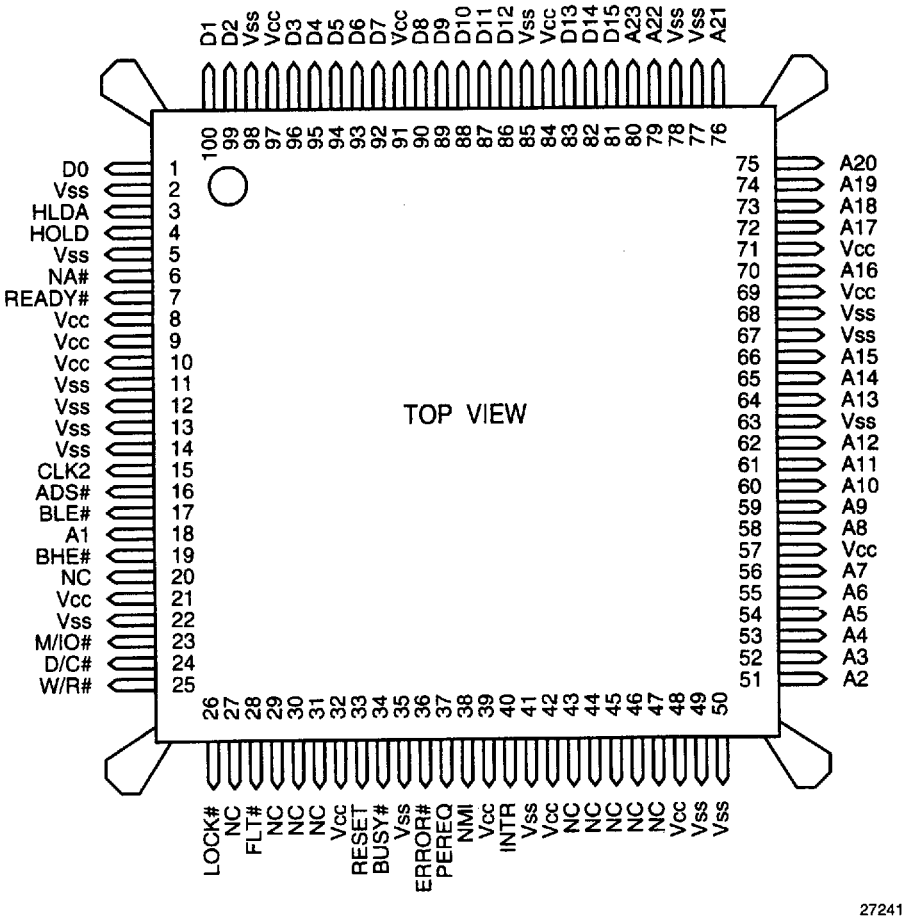
1.0 PIN ASSIGNMENT



NOTE:
NC = No Connection

Figure 2. Intel386™ SXSA Microprocessor Pin Assignment (PQFP)

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Table 1. Pin Assignment

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	D0	26	LOCK#	51	A2	76	A21
2	V_{SS}	27	NC	52	A3	77	V_{SS}
3	HLDA	28	FLT#	53	A4	78	V_{SS}
4	HOLD	29	NC	54	A5	79	A22
5	V_{SS}	30	NC	55	A6	80	A23
6	NA#	31	NC	56	A7	81	D15
7	READY#	32	V_{CC}	57	V_{CC}	82	D14
8	V_{CC}	33	RESET	58	A8	83	D13
9	V_{CC}	34	BUSY#	59	A9	84	V_{CC}
10	V_{CC}	35	V_{SS}	60	A10	85	V_{SS}
11	V_{SS}	36	ERROR#	61	A11	86	D12
12	V_{SS}	37	PEREQ	62	A12	87	D11
13	V_{SS}	38	NMI	63	V_{SS}	88	D10
14	V_{SS}	39	V_{CC}	64	A13	89	D9
15	CLK2	40	INTR	65	A14	90	D8
16	ADS#	41	V_{SS}	66	A15	91	V_{CC}
17	BLE#	42	V_{CC}	67	V_{SS}	92	D7
18	A1	43	NC	68	V_{SS}	93	D6
19	BHE#	44	NC	69	V_{CC}	94	D5
20	NC	45	NC	70	A16	95	D4
21	V_{CC}	46	NC	71	V_{CC}	96	D3
22	V_{SS}	47	NC	72	A17	97	V_{CC}
23	M/IO#	48	V_{CC}	73	A18	98	V_{SS}
24	D/C#	49	V_{SS}	74	A19	99	D2
25	W/R#	50	V_{SS}	75	A20	100	D1

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2.0 PIN DESCRIPTIONS

Table 2 lists the Intel386 SXSA microprocessor pin descriptions. The following definitions are used in the pin descriptions:

The named signal is active low.
I Input signal.
O Output signal.
I/O Input and output signal.
P Power pin.
G Ground pin.

Table 2. Pin Descriptions

Symbol	Type	Pin	Name and Function
A23:1	O	80–79, 76–72, 70, 66–64, 62–58, 56–51, 18	**ADDRESS BUS** outputs physical memory or port I/O addresses.
ADS#	O	16	**ADDRESS STATUS** indicates that the processor is driving a valid bus-cycle definition and address onto its pins (W/R#, D/C#, M/IO#, BHE#, BLE#, and A23:1).
BHE#	O	19	**BYTE HIGH ENABLE** indicates that the processor is transferring a high data byte.
BLE#	O	17	**BYTE LOW ENABLE** indicates that the processor is transferring a low data byte.
BUSY#	I	34	**BUSY** indicates that the math coprocessor is busy.
CLK2	I	15	**CLK2** provides the fundamental timing for the device.
D/C#	O	24	**DATA/CONTROL** indicates whether the current bus cycle is a data cycle (memory or I/O) or a control cycle (interrupt acknowledge, halt, or code fetch). When D/C# is high, the bus cycle is a data cycle; when D/C# is low, the bus cycle is a control cycle.
D15:0	I/O	81–83, 86–90, 92–96, 99–100, 1	**DATA BUS** inputs data during memory read, I/O read, and interrupt acknowledge cycles and outputs data during memory and I/O write cycles.
ERROR#	I	36	**ERROR** indicates that the math coprocessor has an error condition.
FLT#	I	28	**FLOAT** forces all bidirectional and output signals, including HLDA, to a high-impedance state.
HLDA	O	3	**BUS HOLD ACKNOWLEDGE** indicates that the CPU has surrendered control of its local bus to another bus master.
HOLD	I	4	**BUS HOLD REQUEST** allows another bus master to request control of the local bus.
INTR	I	40	**INTERRUPT REQUEST** is a maskable input that causes the CPU to suspend execution of the current program and then execute an interrupt acknowledge cycle.
LOCK#	O	26	**BUS LOCK** prevents other system bus masters from gaining control of the system bus while it is active (low).

Table 2. Pin Descriptions (Continued)

Symbol	Type	Pin	Name and Function
M/IO#	O	23	**MEMORY/IO** indicates whether the current bus cycle is a memory cycle or an input/output cycle. When M/IO# is high, the bus cycle is a memory cycle; when M/IO# is low, the bus cycle is an I/O cycle.
NA#	I	6	**NEXT ADDRESS** requests address pipelining.
NC		20, 27, 29–31, 43–47	**NO CONNECTION** should always be left unconnected. Connecting a NC pin may cause the processor to malfunction or cause your application to be incompatible with future steppings of the device.
NMI	I	38	**NONMASKABLE INTERRUPT REQUEST** is a nonmaskable input that causes the CPU to suspend execution of the current program and execute an interrupt acknowledge function.
PEREQ	I	37	**PROCESSOR EXTENSION REQUEST** indicates that the math coprocessor has data to transfer to the processor.
READY#	I	7	**BUS READY** indicates that the current bus cycle is finished and the external device is ready to accept more data from the processor.
RESET	I	33	**RESET** suspends any operation in progress and places the processor into a known reset state.
W/R#	O	25	**WRITE/READ** indicates whether the current bus cycle is a write cycle or a read cycle. When W/R# is high, the bus cycle is a write cycle; when W/R# is low, it is a read cycle.
V_{CC}	P	8–10, 21, 32, 39, 42, 48, 57, 69, 71, 84, 91, 97	**SYSTEM POWER** provides the nominal DC supply input.
V_{SS}	G	2, 5, 11–14, 22, 35, 41, 49–50, 63, 67–68, 77–78, 85, 98	**SYSTEM GROUND** provides the 0V connection from which all inputs and outputs are measured.

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3.0 DESIGN CONSIDERATIONS

This section describes the Static Intel386 SXSA microprocessor instruction set, component and revision identifier, and package thermal specifications.

3.1 Instruction Set

The Static Intel386 SXSA microprocessor uses the same instruction set as the dynamic Intel386 SX microprocessor. However, the Static Intel386 SXSA microprocessor requires more clock cycles than the dynamic Intel386 SX microprocessor to execute some instructions. Table 4 lists these instructions and the Static Intel386 SXSA microprocessor execution times. For the equivalent dynamic Intel386 SX microprocessor execution times, refer to the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).

3.2 Component and Revision Identifier

To assist users, the microprocessor holds a component identifier and revision identifier in its DX register after reset. The upper 8 bits of DX hold the component identifier, 23H. (The lower nibble, 3H, identifies the Intel386 architecture, while the upper nibble, 2H, identifies the second member of the Intel386 microprocessor family.)

The lower 8 bits of DX hold the revision level identifier. The revision identifier will, in general, chronologically track those component steppings that are intended to have certain improvements or distinction from previous steppings. The revision identifier will track that of the Intel386 CPU whenever possible. However, the revision identifier value is not guaranteed to change with every stepping revision or to follow a completely uniform numerical sequence, depending on the type or intent of the revision or the manufacturing materials required to be changed. Intel has sole discretion over these characteristics of the component. The initial revision identifier for the Static Intel386 SXSA microprocessor is 09H.

3.3 Package Thermal Specifications

Static Intel386 SXSA microprocessor is specified for operation with case temperature (T_{CASE}) as specified in the "DC SPECIFICATIONS" on page 9. The case temperature can be measured in any environment to determine whether the microprocessor is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

An increase in the ambient temperature (T_A) causes a proportional increase in the case temperature (T_{CASE}) and the junction temperature (T_J). See Figure 3 and Figure 4 for case and ambient temperature relationships to frequency. A packaged device produces thermal resistance between junction and case temperatures (θ_{JC}) and between junction and ambient temperatures (θ_{JA}). The relationships between the temperature and thermal resistance parameters are expressed by these equations (P = power dissipated as heat = $V_{CC} \times I_{CC}$):

1. $T_J = T_{CASE} + P \times \theta_{JC}$
2. $T_A = T_J - P \times \theta_{JA}$
3. $T_{CASE} = T_A + P \times [\theta_{JA} - \theta_{JC}]$

A safe operating temperature can be calculated from equation 1 by using the maximum safe T_J of 115°C, the maximum power drawn by the chip in the specific design, and the θ_{JC} value from Table 3. The θ_{JA} value depends on the airflow (measured at the top of the chip) provided by the system ventilation. The θ_{JA} values are given for reference only and are not guaranteed.

Table 3. Thermal Resistances (0°C/W) θ_{JA}, θ_{JC}

Pkg	θ_{JC}	θ_{JA} vs Airflow (ft/min)		
		0	100	200
100 PQFP	5.1	46.0	44.8	41.2

Table 4. Intel386™ SXSA Microprocessor Instruction Execution Times (in Clock Counts)

Instruction	Clock Count		
	Virtual 8086 Mode (Note 1)	Real Address Mode or Virtual 8086 Mode	Protected Virtual Address Mode (Note 3)
POPA		28	35
IN:			
Fixed Port	27	14	7/29
Variable Port	28	15	8/29
OUT:			
Fixed Port	27	14	7/29
Variable Port	28	15	9/29
INS	30	17	9/32
OUTS	31	18	10/33
REP INS	31 + 6n (Note 2)	17 + 6n (Note 2)	10 + 6n/32 + 6n (Note 2)
REP OUTS	30 + 8n (Note 2)	16 + 8n (Note 2)	10 + 8n/31 + 8n (Note 2)
HLT		7	7
MOV C0, reg		10	10

NOTES:
1. The clock count values in this column apply if I/O permission allows I/O to the port in virtual 8086 mode. If the I/O bit map denies permission, exception fault 13 occurs; see clock counts for the INT 3 instruction in the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).
2. n = the number of times repeated.
3. When two clock counts are listed, the smaller value refers to a register operand and the larger value refers to a memory operand.

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4.0 DC SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +150°C
Case Temperature under Bias ... −65°C to +112°C
Supply Voltage with Respect to V_{SS} ..... −0.5V to +6.5V
Voltage on Other Pins ..... −0.5V to V_{CC} + 0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS*

V_{CC} (Digital Supply Voltage— 25 MHz and 33 MHz) .....4.5V to 5.5V

V_{CC} (Digital Supply Voltage— 40 MHz) .....4.75V to 5.25V

T_{CASE} Minimum (Case Temperature under Bias) .....0°C

T_{CASE} Maximum .....see Figure 4

Operating Frequency .....0 MHz to 40 MHz

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Table 5. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{ILC}	CLK2 Input Low Voltage	−0.3	+0.8	V	
V_{IHC}	CLK2 Input High Voltage	V_{CC} − 0.8	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5 mA
V_{OH}	Output High Voltage	2.4 V_{CC} − 0.5		V V	I_{OH} = −1 mA I_{OH} = −0.2 mA
I_{LI}	Input Leakage Current (for all pins except PEREQ, BUSY#, FLT#, ERROR#)		±15	μA	$0 \le V_{IN} \le V_{CC}$
I_{IH}	Input Leakage Current (PEREQ)		150	μA	V_{IH} = 2.4V (Note 1)
I_{IL}	Input Leakage Current (BUSY#, FLT#, ERROR#)		−120	μA	V_{IL} = 0.45V (Note 2)
I_{LO}	Output Leakage Current		±15	μA	$0.45V \le V_{OUT} \le V_{CC}$

NOTES:
1. PEREQ input has an internal weak pull-down resistor.
2. BUSY#, FLT# and ERROR# inputs each have an internal weak pull-up resistor.
3. I_{CC} max measurement at worst-case frequency, V_{CC}, and temperature with reset active.
4. I_{CC} typical and I_{CCF} typical are measured at nominal V_{CC} and are not fully tested.
5. Not fully tested.

Table 5. DC Characteristics (Continued)

Symbol	Parameter	Min	Max	Unit	Test Condition
I_{CC}	Supply Current				(Notes 3, 4)
	CLK2 = 80 MHz, CLK = 40 MHz		275	mA	Typical = 200 mA
	CLK2 = 66 MHz, CLK = 33 MHz		225	mA	Typical = 175 mA
	CLK2 = 50 MHz, CLK = 25 MHz		175	mA	Typical = 140 mA
I_{CCF}	Standby Current (Freeze Mode)		150	μA	Typical = 10 μA (Notes 3, 4)
C_{IN}	Input Capacitance		10	pF	F_C = 1 MHz (Note 5)
C_{OUT}	Output or I/O Capacitance		12	pF	F_C = 1 MHz (Note 5)
C_{CLK}	CLK2 Capacitance		20	pF	F_C = 1 MHz (Note 5)

NOTES:
1. PEREQ input has an internal weak pull-down resistor.
2. BUSY#, FLT# and ERROR# inputs each have an internal weak pull-up resistor.
3. I_{CC} max measurement at worst-case frequency, V_{CC}, and temperature with reset active.
4. I_{CC} typical and I_{CCF} typical are measured at nominal V_{CC} and are not fully tested.
5. Not fully tested.

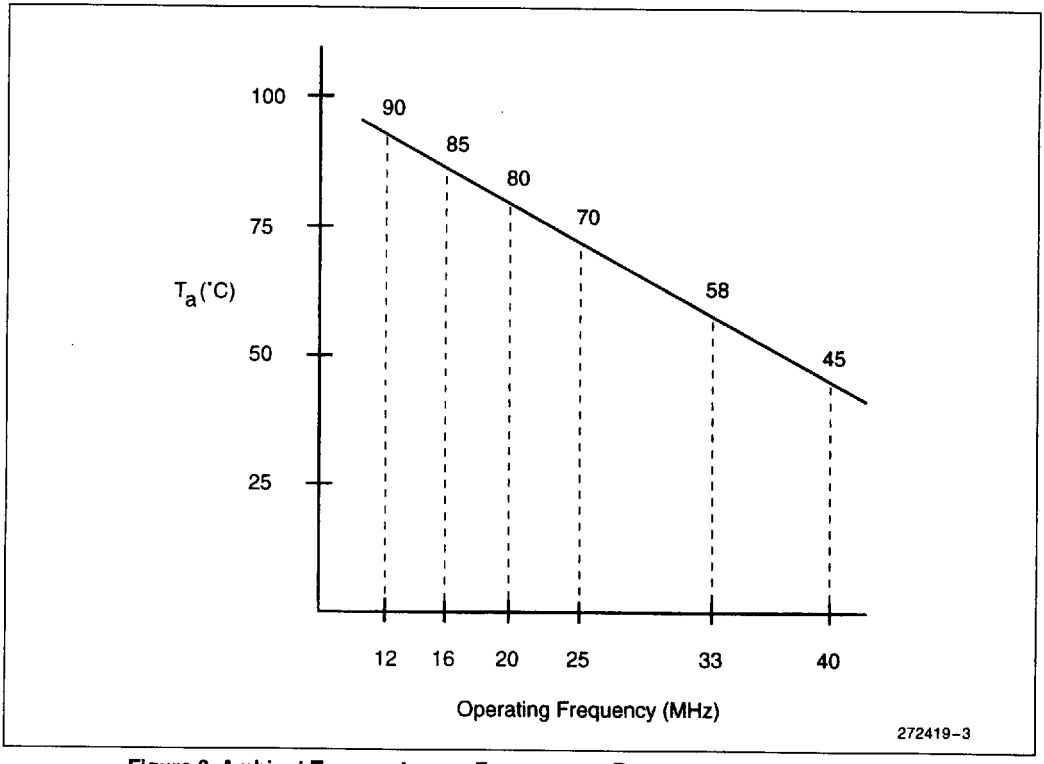

Figure 3. Ambient Temperature vs Frequency at Zero Air Flow and T_J = 115°C

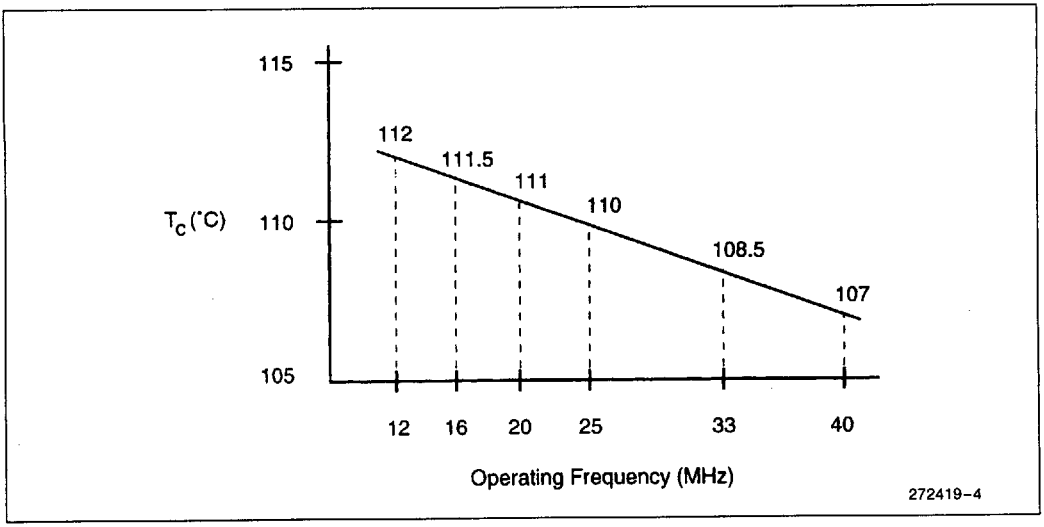

Figure 4. Case Temperature vs Frequency at T_J = 115°C

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5.0 AC SPECIFICATIONS

Table 6 lists output delays, input setup requirements, and input hold requirements. All AC specifications are relative to the CLK2 rising edge crossing the 2.0V level.

Figure 5 shows the measurement points for AC specifications. Inputs must be driven to the indicated voltage levels when AC specifications are measured. Output delays are specified with minimum and maximum limits measured as shown. The minimum delay times are hold times provided to external circuitry. Input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct operation.

Outputs ADS#, W/R#, D/C#, MI/O#, LOCK#, BHE#, BLE#, A23:1 and HLDA change only at the beginning of phase one. D15:0 (write cycles) change only at the beginning of phase two.

The READY#, HOLD, BUSY#, ERROR#, PEREQ, FLT# and D15:0 (read cycles) inputs are sampled at the beginning of phase one. The NA#, INTR and NMI inputs are sampled at the beginning of phase two.

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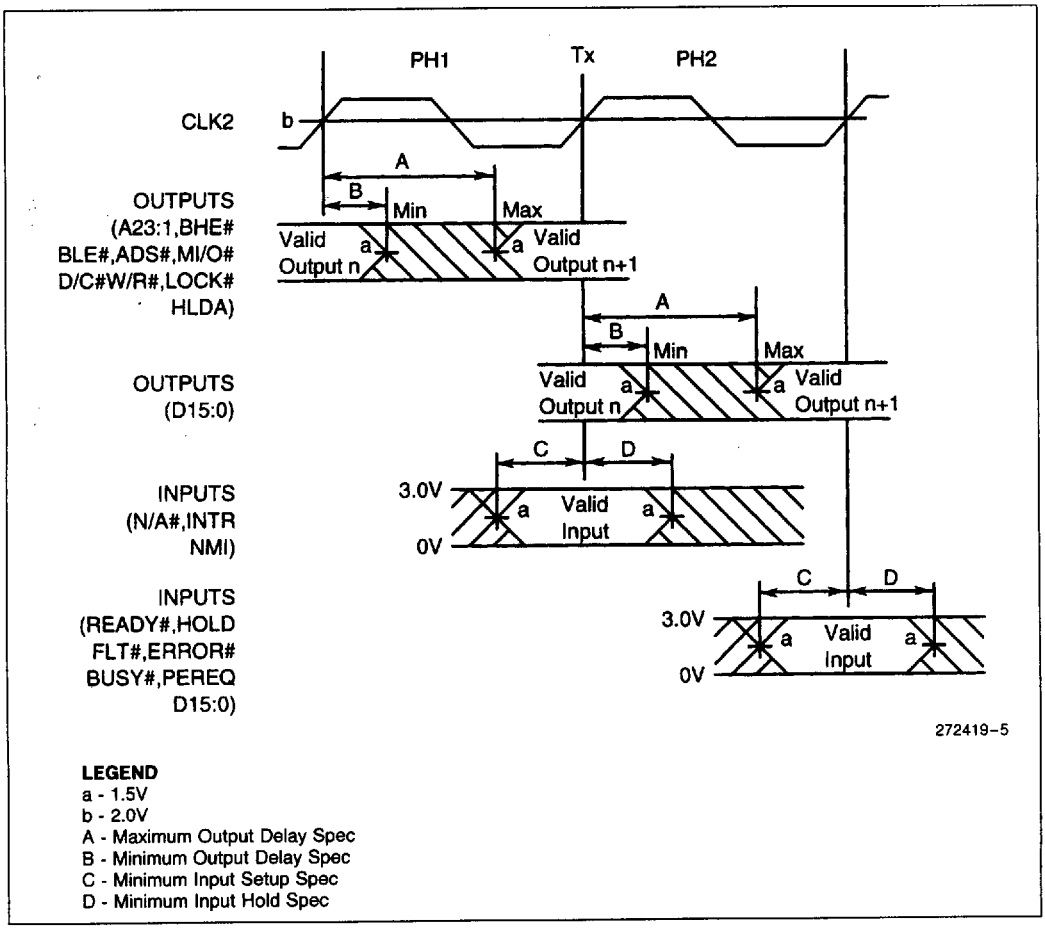

LEGEND
a - 1.5V
b - 2.0V
A - Maximum Output Delay Spec
B - Minimum Output Delay Spec
C - Minimum Input Setup Spec
D - Minimum Input Hold Spec

Figure 5. Drive Levels and Measurement Points for AC Specifications

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Table 6. AC Characteristics

Symbol	Parameter	40 MHz		33 MHz		25 MHz		Test Condition
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	
	Operating Frequency	0	40	0	33	0	25	MHz (Note 1)
t_1	CLK2 Period	12.5		15		20		
t_{2a}	CLK2 High Time	4.5		6.25		7		(Note 2)
t_{2b}	CLK2 High Time	3.5		4		4		(Note 2)
t_{3a}	CLK2 Low Time	4.5		6.25		7		(Note 2)
t_{3b}	CLK2 Low Time	3.5		4.5		5		(Note 2)
t_4	CLK2 Fall Time		4		4		7	(Note 2)
t_5	CLK2 Rise Time		4		4		7	(Note 2)
t_6	A23:1 Valid Delay	4	13	4	15	4	17	C_L = 50 pF
t_7	A23:1 Float Delay	4	20	4	20	4	30	(Note 3)
t_8	BHE#, BLE#, LOCK# Valid Delay	4	13	4	15	4	17	C_L = 50 pF
t_9	BHE#, BLE#, LOCK# Float Delay	4	20	4	20	4	30	(Note 3)
t_{10}	W/R#, M/IO#, D/C#, ADS# Valid Delay	4	13	4	15	4	17	C_L = 50 pF
t_{11}	W/R#, M/IO#, D/C#, ADS# Float Delay	4	20	4	20	4	30	(Note 3)
t_{12}	D15:0 Write Data Valid Delay	7	18	7	23	7	23	C_L = 50 pF
t_{12a}	D15:0 Write Data Hold Time	2		2		2		C_L = 50 pF
t_{13}	D15:0 Write Data Float Delay	4	17	4	17	4	22	(Note 3)
t_{14}	HLDA Valid Delay	4	17	4	20	4	22	C_L = 50 pF
t_{15}	NA# Setup Time	5		5		5		
t_{16}	NA# Hold Time	2		2		3		
t_{19}	READY# Setup Time	7		7		9		
t_{20}	READY# Hold Time	4		4		4		
t_{21}	D15:0 Read Setup Time	4		5		7		
t_{22}	D15:0 Read Hold Time	3		3		5		

NOTES:
1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.

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Table 6. AC Characteristics (Continued)

Symbol	Parameter	40 MHz		33 MHz		25 MHz		Test Condition
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	
t_{23}	HOLD Setup Time	4		9		9		
t_{24}	HOLD Hold Time	2		2		3		
t_{25}	RESET Setup Time	4		5		8		
t_{26}	RESET Hold Time	2		2		3		
t_{27}	NMI, INTR Setup Time	5		5		6		(Note 4)
t_{28}	NMI, INTR Hold Time	5		5		6		(Note 4)
t_{29}	PEREQ, ERROR#, BUSY#, FLT# Setup Time	5		5		6		(Note 4)
t_{30}	PEREQ, ERROR#, BUSY#, FLT# Hold Time	4		4		5		(Note 4)

NOTES:
1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.

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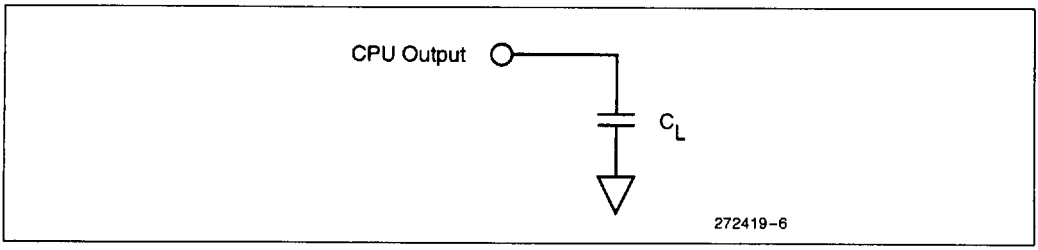

Figure 6. AC Test Loads

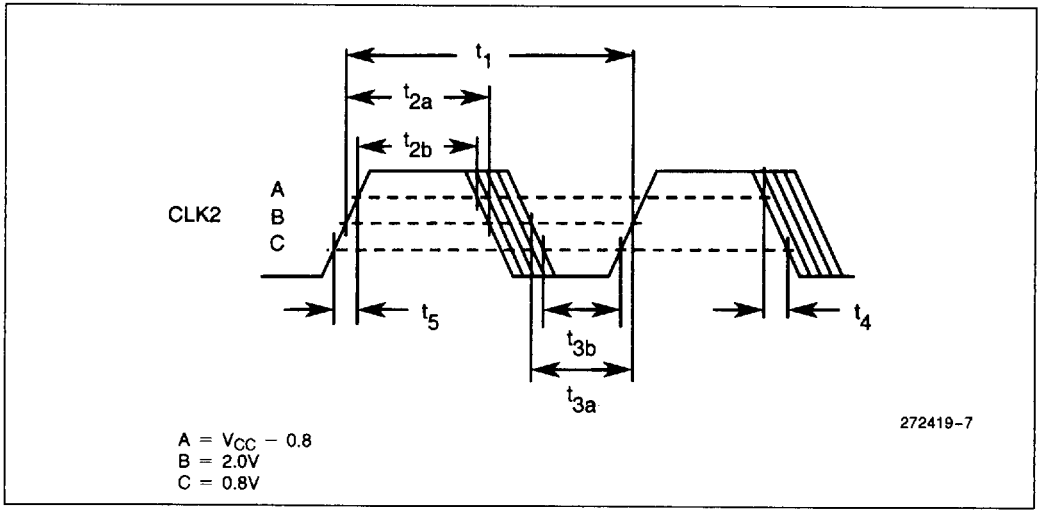

Figure 7. CLK2 Waveform

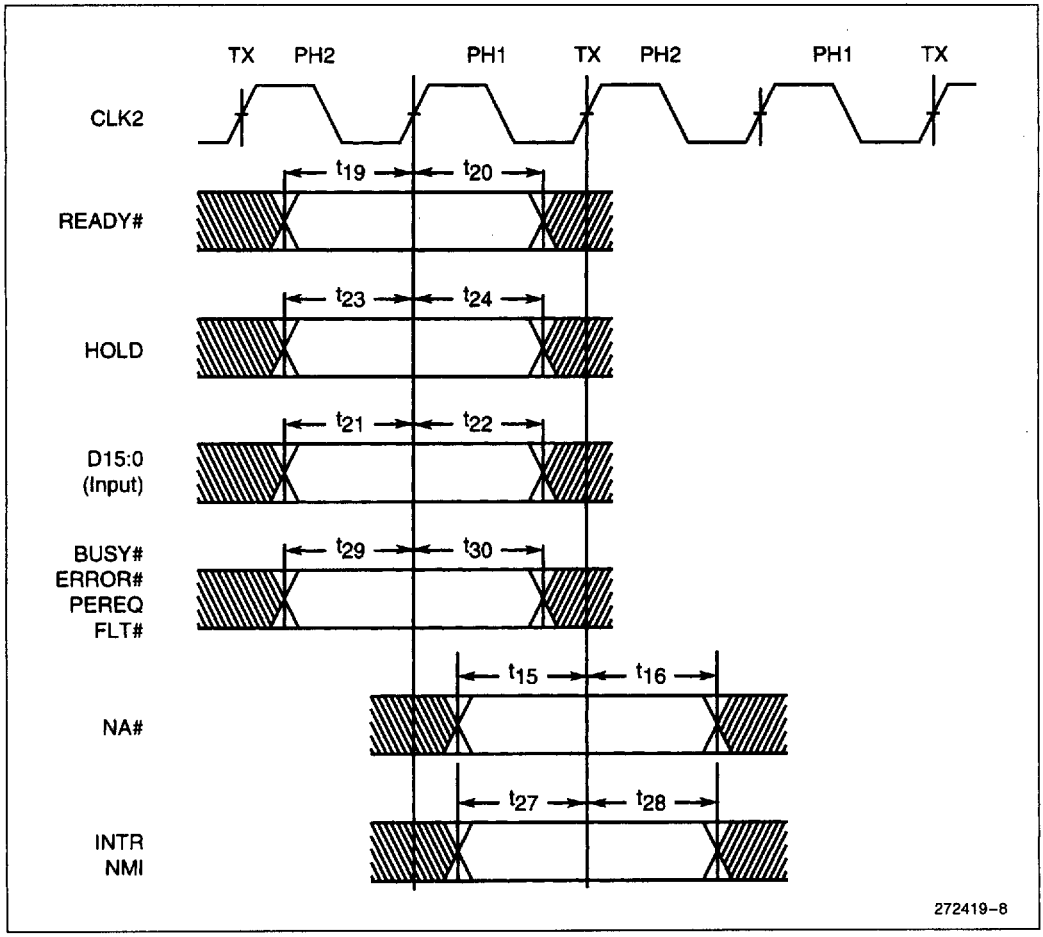

Figure 8. AC Timing Waveforms—Input Setup and Hold Timing

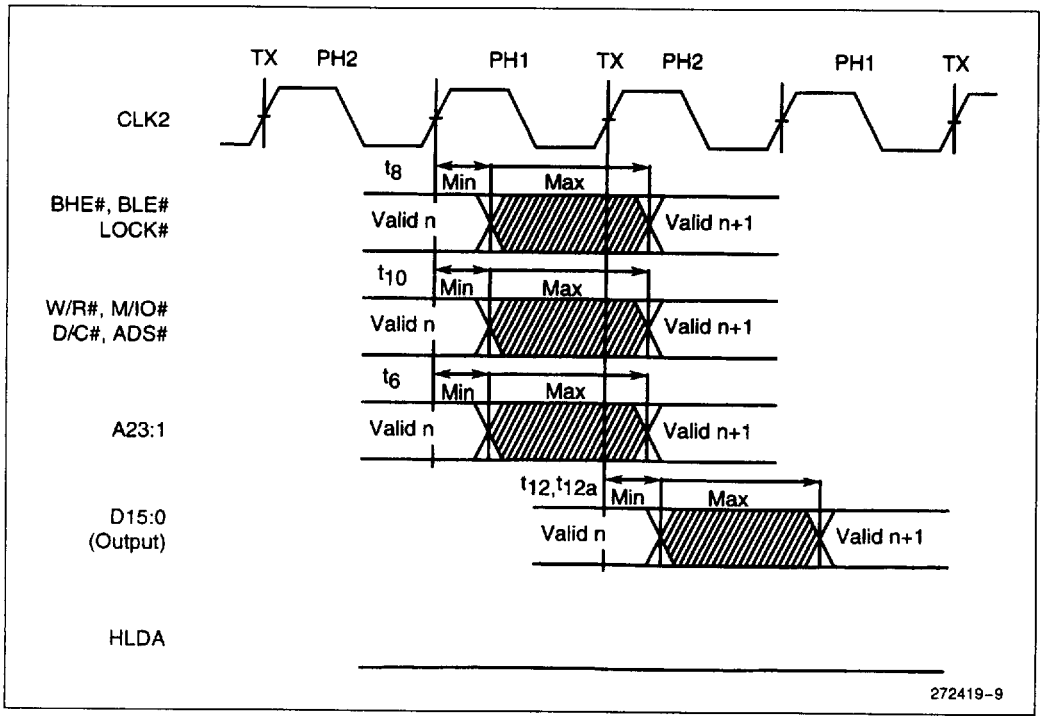

Figure 9. AC Timing Waveforms—Output Valid Delay Timing

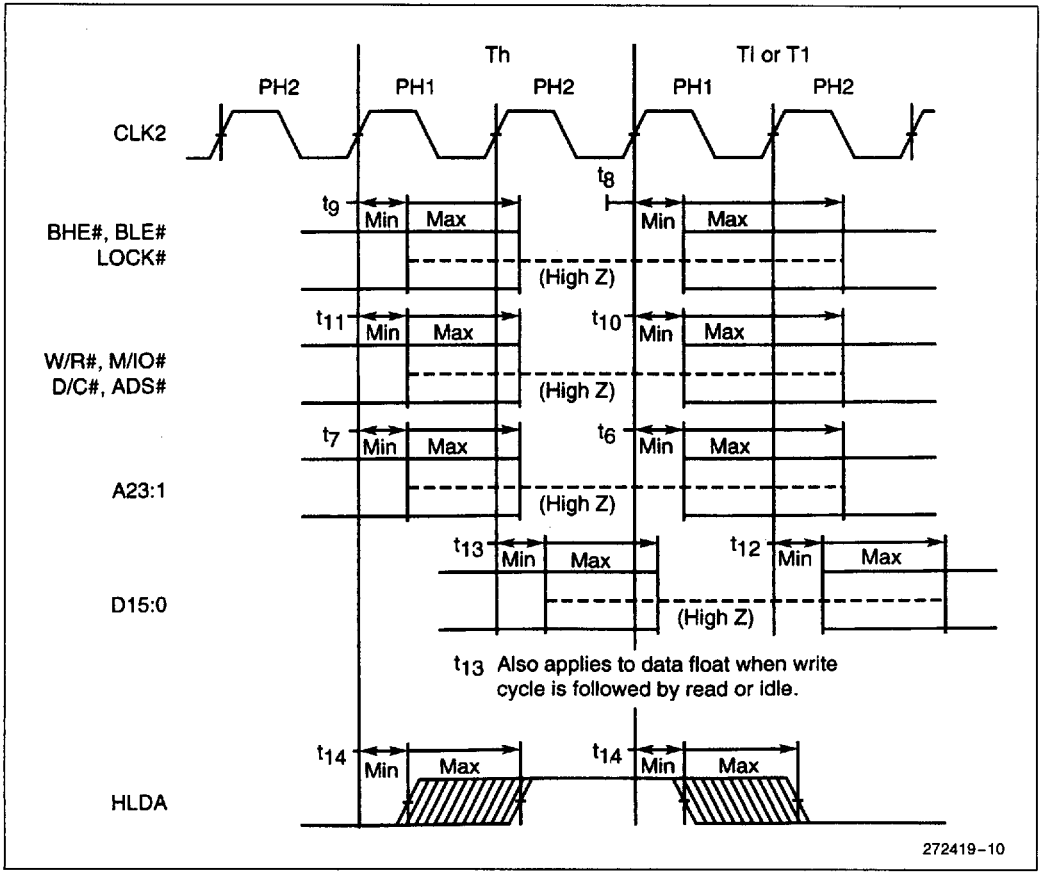

Figure 10. AC Timing Waveforms—Output Float Delay and HLDA Valid Delay Timing

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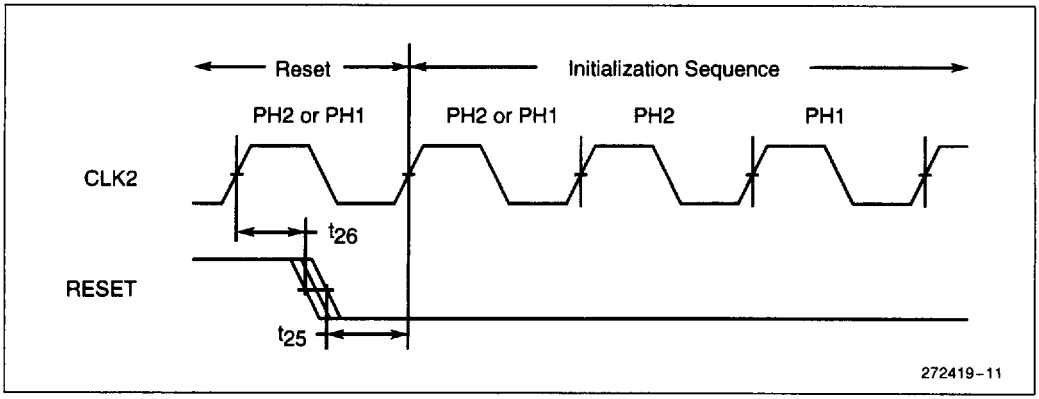

Figure 11. AC Timing Waveforms—RESET Setup and Hold Timing and Internal Phase

6.0 REVISION HISTORY

This -003 data sheet contains the following changes from the -002 version.

- Changed V_{CC} at 40 MHz to 4.75V to 5.25V (Pages 1 and 9)
- Renamed "Powerdown Mode" to "Clock Freeze Mode" on page 1.
- Added Clarifications to Figure 1.
- Corrected pin numbering for A23:1 in Table 2.
- Changed Section 3.3 first sentence from "... on page 12" to "... on page 9".
- Changed first sentence on page 12 from "Table 7 lists ..." to "Table 6 lists ...". Also changed fourth paragraph, first sentence on page 12 from "... A25:1" to "... A23:1".

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