Document Title

2Mx16 bit Uni-Transistor Random Access Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft - Design target	September 4, 2000	Advance
0.1	Revised - Change package type from FBGA to TBGA. - Improve operating current from 30mA to 25mA. - Change input and output reference voltage from 1.1V to 1.5V at AC test condition. - Expand max operating voltage from 3.0V to 3.3V. - Expand max operating temperature from 70°C to 85°C. - Release speed from 70/85ns to 100ns. - Release standby current form 170µA to 200µA. - Add Power up timing diagram. - Add AC characteristics for continuous write.	February 9, 2001	Preliminary
1.0	Finalize - Release standby current form 200µA to 250µA. - Release deep power down current form 10µA to 20µA. - Release t_{WC} for continuous write operation from 100ns to 110ns. - Release t_{CW} for continuous write operation from 90ns to 100ns. - Release t_{AW} for continuous write operation from 90ns to 100ns. - Release t_{BW} for continuous write operation from 90ns to 100ns. - Release t_{WP} for continuous write operation from 90ns to 100ns.	March 30, 2001	Final
2.0	Revised - Add product list	April 16, 2001	Final
3.0	Revised - Improve standby current from 250µA to 150µA.	May 28, 2001	Final

2M x 16 bit Uni-Transistor CMOS RAM

FEATURES

- Process Technology: CMOS
- Organization: 2M x16 bit
- Power Supply Voltage: 2.7~3.3V
- Three state output status
- Deep Power Down: Memory cell data hold invalid
- Package Type: 48-TBGA-9.00x12.00
- Compatible with Low Power SRAM

GENERAL DESCRIPTION

The K1S321615M is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device support, extended temperature range and 48 ball Chip Scale Package for user flexibility of system design. The device also supports deep power down mode for low standby current.

PRODUCT FAMILY

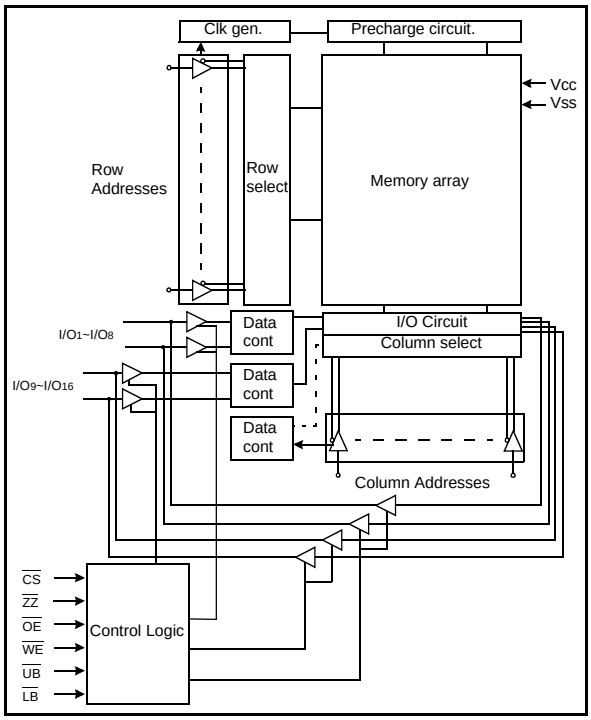
Product Family	Operating Temp.	Vcc Range	Speed (t_{RC})	Power Dissipation			PKG Type
				Standby (I_{SB1}, Max.)	Deep power down(I_{SBD}, Max.)	Operating (I_{CC2}, Max.)	
K1S321615M-E	Extended(-25~85°C)	2.7~3.3V	100ns	150µA	20µA	25mA	48-TBGA-9.00x12.00

PIN DESCRIPTION

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	$\overline{ZZ}$
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CS}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	Vss	I/O12	A17	A7	I/O4	Vcc
E	Vcc	I/O13	DNU	A16	I/O5	Vss
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	A19	A12	A13	$\overline{WE}$	I/O8
H	A18	A8	A9	A10	A11	A20

48-TBGA: Top View(Ball Down)

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{ZZ}$	Deep Power Down	Vss	Ground
$\overline{OE}$	Output Enable Input	$\overline{UB}$	Upper Byte($I/O_{9\sim16}$)
$\overline{WE}$	Write Enable Input	$\overline{LB}$	Lower Byte($I/O_{1\sim8}$)
A_0~A_{20}	Address Inputs	DNU	Do Not Use[1)]
I/O_1~I/O_{16}	Data Inputs/Outputs		

1) Reserved for future user

POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power(Vcc min.=2.7V) for a minium 200µs with $\overline{CS}$=high.
3. Issue read operation at least twice.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{ZZ}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~8	I/O9~16	Mode	Power
H	H	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	Standby
X[1)]	L	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	Deep Power Down
L	H	X[1)]	X[1)]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1)]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1)]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1)]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1)]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1)]	L	L	L	Din	Din	Word Write	Active

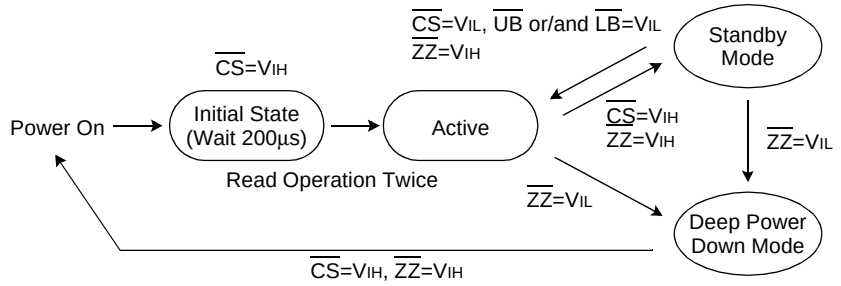
1. X means dont care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 3.6V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-25 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions longer than 1seconds may affect reliability.

STANDBY MODE STATE MACHINES



STANDBY MODE CHARACTERISTIC

Power Mode	Memory Cell Data	Standby Current(mA)	Wait Time(ms)
Standby	Valid	150	0
Deep Power Down	Invaild	20	200

PRODUCT LIST

Extended Temperature Products(-25~85°C)	
Part Name	**Function**
K1S321615M-EE10	48-TBGA with 48 ball, 100ns, 3.0V

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.7	3.0	3.3	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

1. T_A=-25 to 85°C, otherwise specified.
2. Overshoot: Vcc+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)](f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

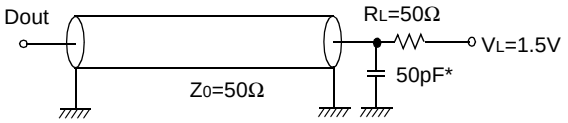
Item	Symbol	Test Conditions	Min	Typ[1)]	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{ZZ}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc	-1	-	1	µA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, $\overline{ZZ}$≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	-	2	5	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, $\overline{ZZ}$=V_{IH}, VIN=V_{IL} or V_{IH}	-	18	25	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V
Standby Current(CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, $\overline{ZZ}$≥Vcc-0.2V, Other inputs=Vss to Vcc	-	120	150	µA
Deep Power Down	I_{SBD}	$\overline{ZZ}$≤0.2V, Other inputs=Vss to Vcc	-	5	20	µA

1. Typical values are tested at V_{CC}=3.0V, T_A=25°C and not guaranteed.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load(See right): C_L=50pF



* Include scope and jig capacitance

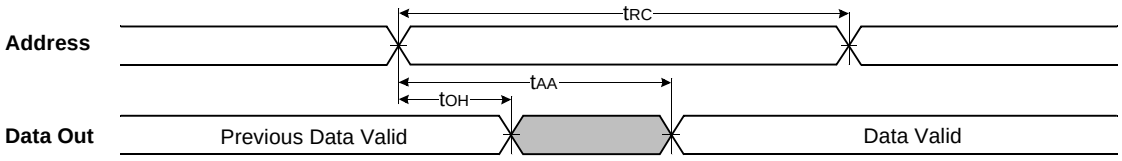
AC CHARACTERISTICS(V_{CC}=2.7~3.3V, T_A=-25 to 85°C)

Parameter List		Symbol	Speed Bins				Units
			100ns[1]		100ns[2]		
			Min	Max	Min	Max	
Read	Read Cycle Time	t_{RC}	100	-	100	-	ns
	Address Access Time	t_{AA}	-	100	-	100	ns
	Chip Select to Output	t_{CO}	-	100	-	100	ns
	Output Enable to Valid Output	t_{OE}	-	50	-	50	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	100	-	100	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	0	25	ns
	Output Hold from Address Change	t_{OH}	5	-	5	-	ns
Write	Write Cycle Time	t_{WC}	100	-	110	-	ns
	Chip Select to End of Write	t_{CW}	80	-	100	-	ns
	Address Set-up Time	t_{AS}	0	-	0	-	ns
	Address Valid to End of Write	t_{AW}	80	-	100	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	80	-	100	-	ns
	Write Pulse Width	t_{WP}	70	-	100	-	ns
	Write Recovery Time	t_{WR}	0	-	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	30	0	30	ns
	Data to Write Time Overlap	t_{DW}	40	-	40	-	ns
	Data Hold from Write Time	t_{DH}	0	-	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	5	-	ns

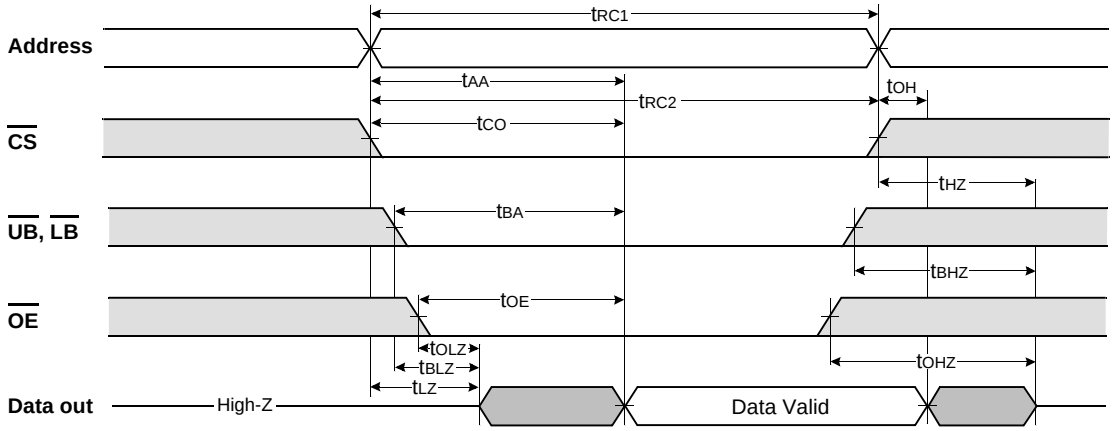
1. The characteristics which is restricted for continuous write operation over 20 times, please refer to technical note.
2. The characteristics for continuous write operation.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{ZZ}$=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



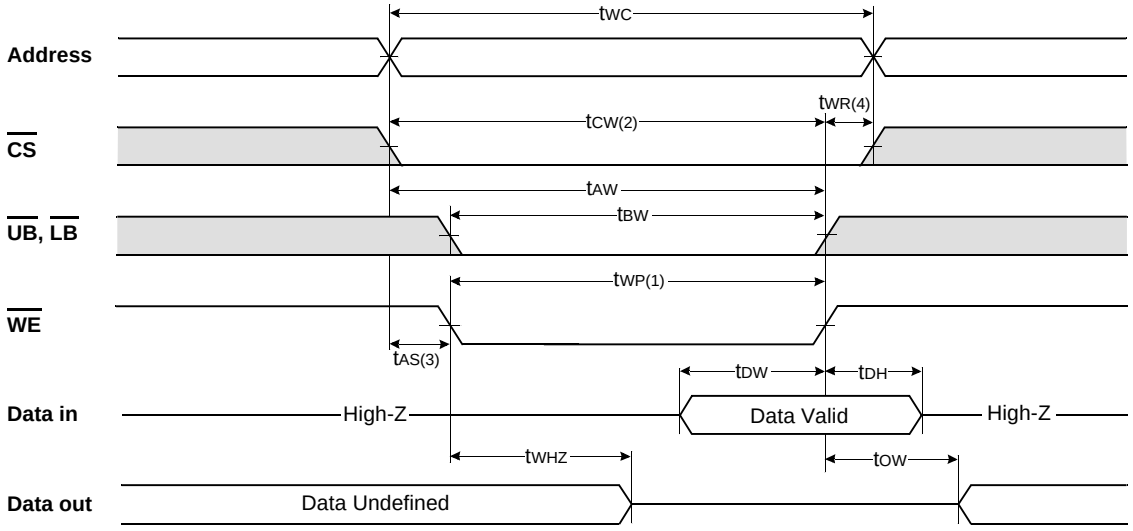
TIMING WAVEFORM OF READ CYCLE(2)($\overline{ZZ}$=$\overline{WE}$=V_{IH})



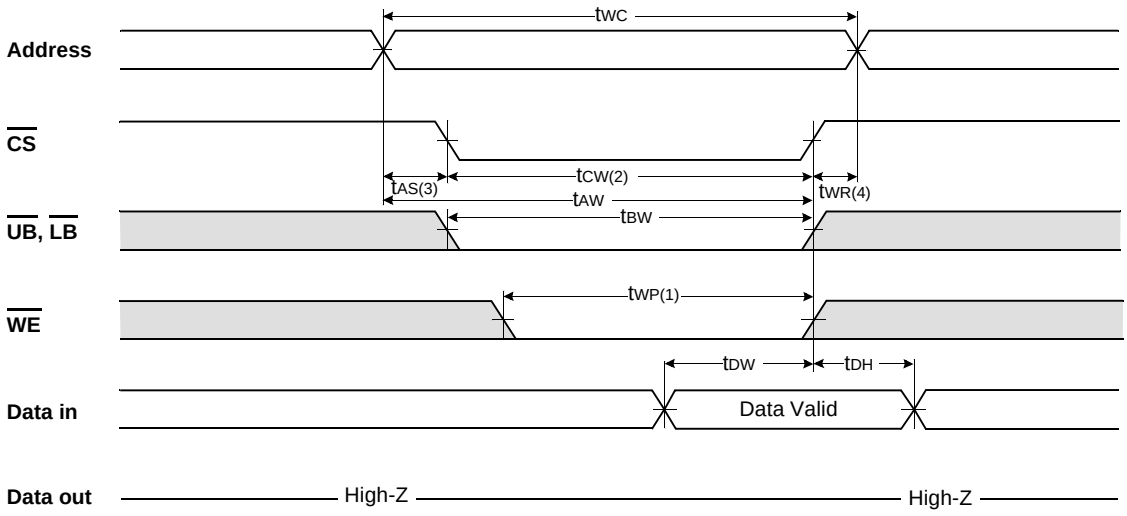
(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. The minimum read cycle(t_{RC}) is determined later one of the t_{RC1} and t_{RC2}.

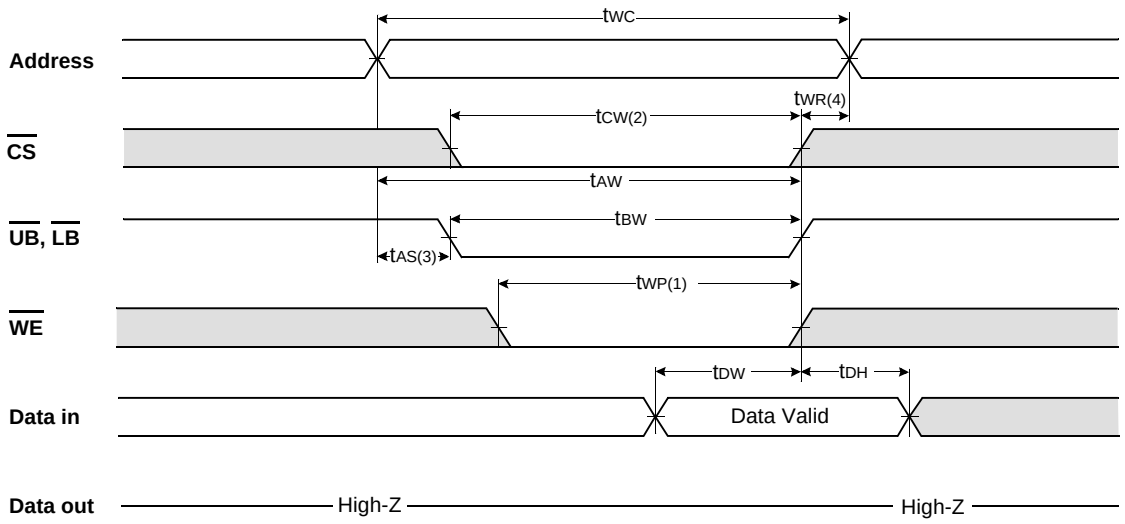
TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{WE}$ Controlled, $\overline{ZZ}$=V_{IH})



TIMING WAVEFORM OF WRITE CYCLE(2)($\overline{CS}$ Controlled, $\overline{ZZ}$=V_{IH})



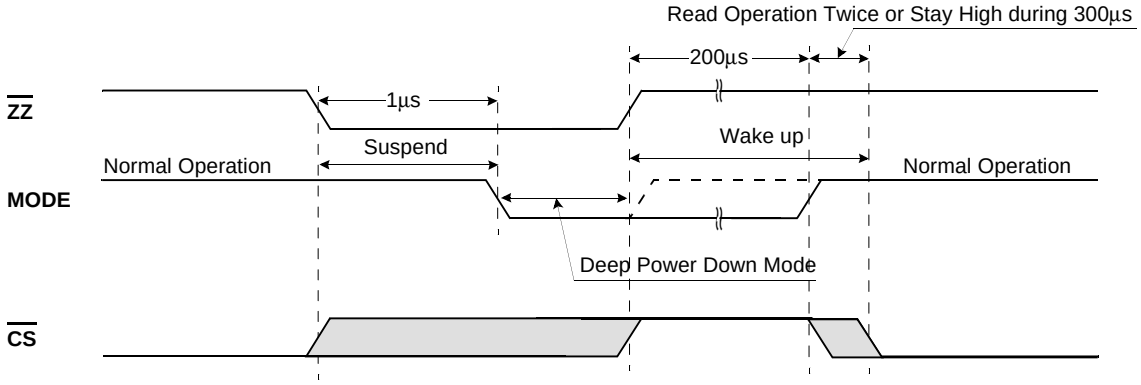
TIMING WAVEFORM OF WRITE CYCLE(3)($\overline{UB}$, $\overline{LB}$ Controlled, $\overline{ZZ}$=V_{IH})



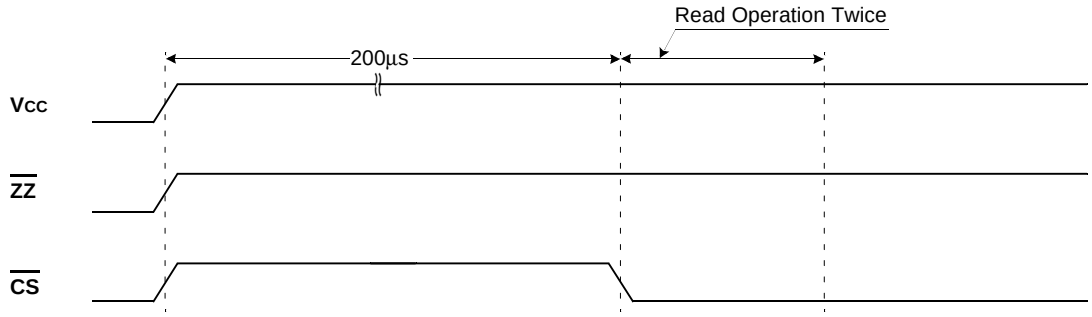
(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

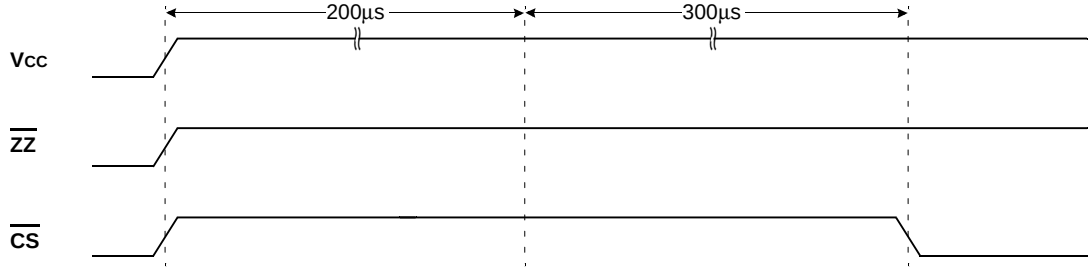
TIMING WAVEFORM OF DEEP POWER DOWN MODE



TIMING WAVEFORM OF POWER UP(1)



TIMING WAVEFORM OF POWER UP(2)(No Dummy Cycle)

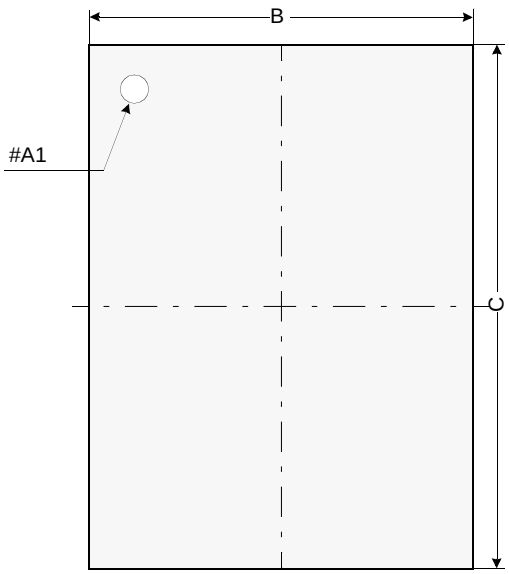


PACKAGE DIMENSION

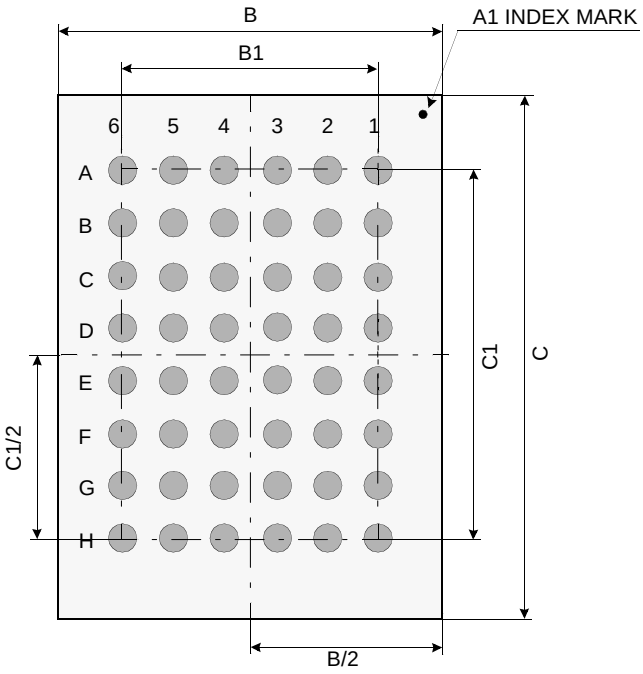
Unit: millimeters

48 TAPE BALL GRID ARRAY(0.75mm ball pitch)

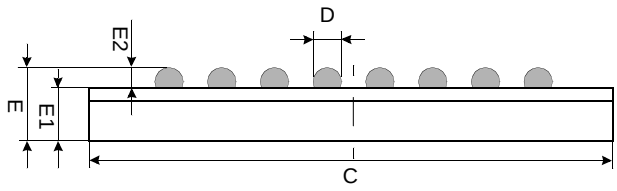
Top View



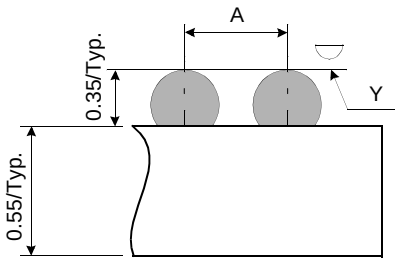
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.75	-
B	8.90	9.00	9.10
B1	-	3.75	-
C	11.90	12.00	12.10
C1	-	5.25	-
D	0.40	0.45	0.50
E	-	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.08

Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are ±0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)

TECHNICAL NOTE

UtRAM USAGE AND TIMING

INTRODUCTION

UtRAM is based on single-transistor DRAM cells. As with any other DRAM, the data in these cells must be periodically refreshed to prevent data loss. What makes the UtRAM unique is that it offers a true SRAM style interface that hides all refresh operations from the memory controller.

START WITH A DRAM TECHNOLOGY

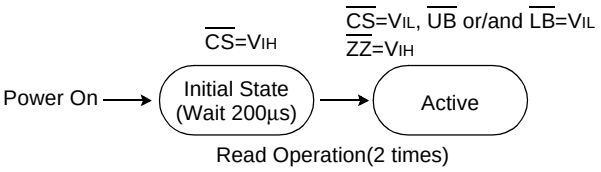
The key to the UtRAM is its high speed and low power. This speed comes from the use of many small blocks, often just 32Kbits each, to create UtRAM arrays. The small blocks have short word lines with little capacitance, eliminating a major source of operating current in conventional DRAM blocks.

Each independent macro-cell on a UtRAM device consists of a number of these blocks. Each chip has one or more macro.

The address decoding logic is also fast. UtRAM perform a complete read operation in every tRC, but UtRAM needs power up sequence like a DRAM.

Power Up Sequence and Diagram

1. Apply power.
2. Maintain stable power for a minium 200µs with $\overline{CS}$=high.
3. Issue read operation at least 2 times.



DESIGN ACHIEVES SRAM SPECIFIC OPERATIONS

The UtRAM design works just like an SRAM, with no wait states or other overhead for precharging or refreshing its internal DRAM cells. SAMSUNG Electronics(SAMSUNG) hides these operations with advanced design. Precharging takes place during every access, overlapped with the end of the cycle and the decoding portion of the next cycle.

Hiding refresh is more difficult, Every row in every block must be refreshed at least once during the refresh interval to prevent data loss. SAMSUNG provides a internal refresh controller for devices. When all accesses during a refresh interval are directed to one macro-cell, as can happen in signal processing applications, a more sophisticated approach is required to hide refresh. The pseudo SRAM, sometimes used on these applications, which is required a memory controller that can hold off accesses when a refresh operation is needed. SAMSUNG unique qualitative advantage over these parts(in addition to quantitative improvements in access speed and power consumption) is that the UtRAM never needs to hold off accesses, and indeed it has no hold off signal. The circuitry that gives SAMSUNG this advantage is fairly simple but has not previously been disclosed.

AVOID TIMING

Following figures are show you a abonormal timing which is not supported on UtRAM and their solution.

At read operation, if your system have a timing which sustain invalid states over 4us at read mode like Figure 1. There are some guide line for proper operation of UtRAM.

When your system have multiple invalid address signal shorter than tRC on the timing which showed in Figure 1, UtRAM need a normal read timing during that cycle(Figure 2) or toggle the $\overline{CS}$ to high'about tRC(Figure 3).

Figure 1.

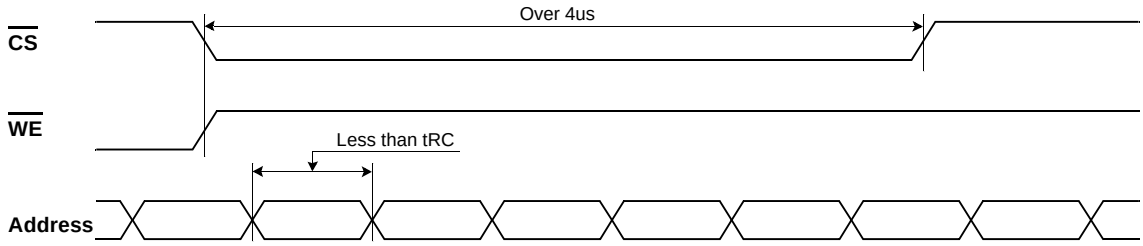


Figure 2.

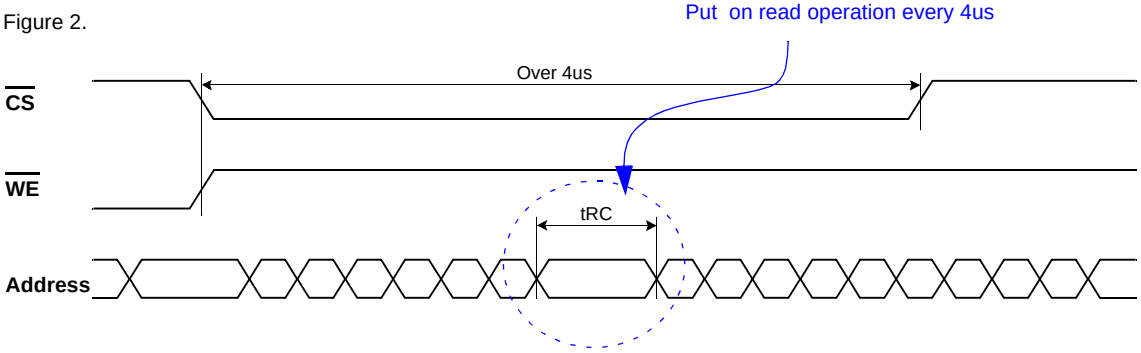
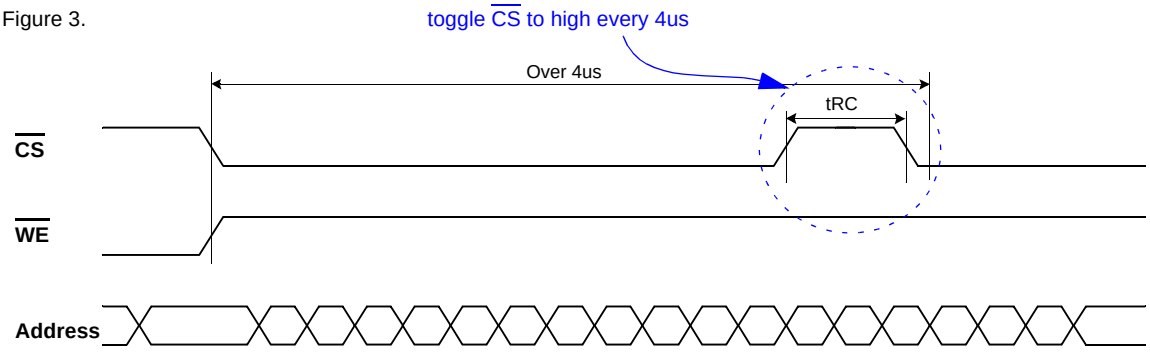


Figure 3.



Write operation have similar restricted operation with Read. If your system have a timing which sustain invalid states over 4us at write mode and system have continuous write signal with Min. tWC over 4us like Figure 4.

You must put read timing on the cycle(Figure 5) or toggle the CS to high about tRC(Figure 6).

Figure 4.

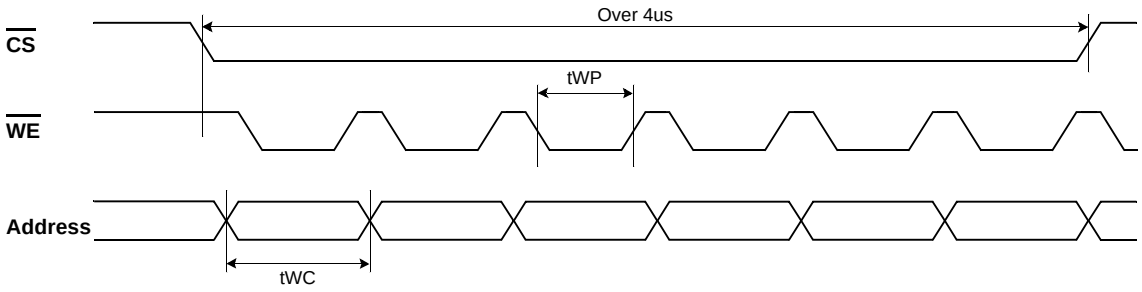


Figure 5.

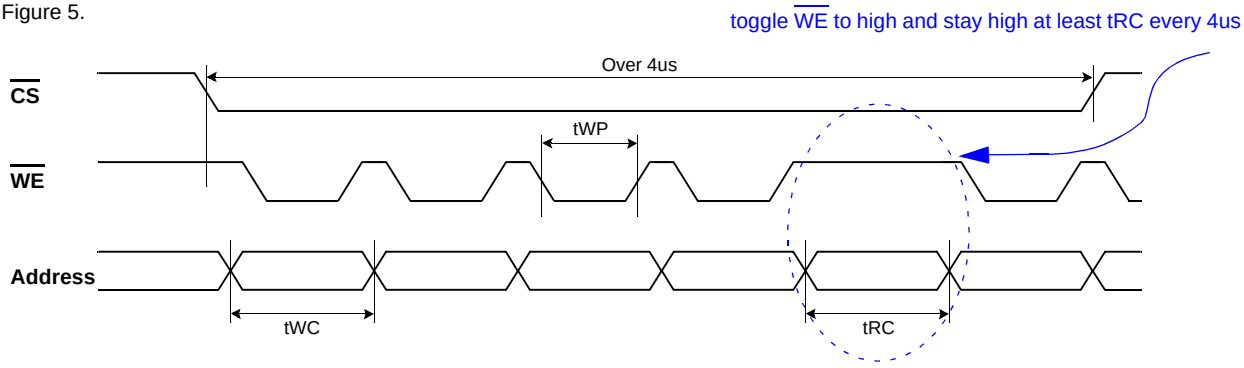


Figure 6.