HYM536410B Series

4M x 36-bit CMOS DRAM MODULE

PRELIMINARY

DESCRIPTION

The HYM536410B is a 4M x 36-bit Fast page mode CMOS DRAM module consisting of nine HY5117400 in 24/28 pin SOJ on a 72 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitor is mounted for each DRAM. The HYM536410BM/BLM are Tin-Lead plated and HYM536410BMG/BLMG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 16M byte memory.

FEATURES

- **Low power dissipation**
  - **Max. battery back-up 24.75mW (L-part)**
  - **Max. CMOS standby 19.80mW (L-part)**
    49.50mW
  - **Max. TTL standby 99.00mW**
  - **Max. operating**

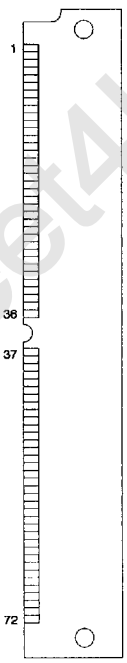
Speed	Power
60	5.94W
70	4.95W
80	4.21W

- **Single power supply of 5V±10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	18ns	45ns
80	80ns	20ns	50ns

- **Fast page mode operation**
- **$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$, $\overline{\text{RAS}}$-only, Hidden refresh**
- **2048 refresh cycles / 256ms (L-part)**
  2048 refresh cycles / 32ms

PIN CONNECTION



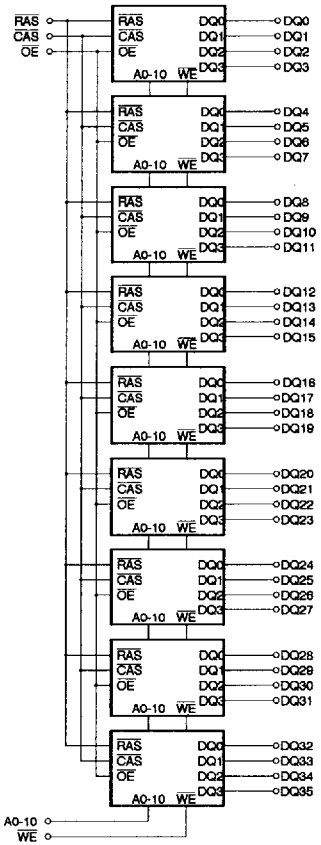
PIN DESCRIPTION

$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
A0-A10	Address Input
DQ0-DQ35	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+5V)
Vss	Ground

PIN NAME

#	NAME	#	NAME
1	Vss	37	DQ19
2	DQ0	38	DQ20
3	DQ1	39	Vss
4	DQ2	40	$\overline{CAS}$
5	DQ3	41	A10
6	DQ4	42	NC
7	DQ5	43	NC
8	DQ6	44	$\overline{RAS}$
9	DQ7	45	NC
10	Vcc	46	DQ21
11	NC	47	$\overline{WE}$
12	A0	48	Vss
13	A1	49	DQ22
14	A2	50	DQ23
15	A3	51	DQ24
16	A4	52	DQ25
17	A5	53	DQ26
18	A6	54	DQ27
19	$\overline{OE}$	55	DQ28
20	DQ8	56	DQ29
21	DQ9	57	DQ30
22	DQ10	58	DQ31
23	DQ11	59	Vcc
24	DQ12	60	DQ32
25	DQ13	61	DQ14
26	DQ14	62	DQ33
27	DQ15	63	DQ15
28	A7	64	DQ34
29	DQ16	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	NC	70	PD4
35	DQ17	71	NC
36	DQ18	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PINS

PIN	-60	-70	-80
PD1	Vss	Vss	Vss
PD2	NC	NC	NC
PD3	NC	Vss	NC
PD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	6.3	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	–1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V±10%, V_{SS} = 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \le V_{IN} \le V_{CC}+1.0$, All other pins not under test = V_{SS}		-90	90	μA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	μA	
I_{CC1}	V_{CC} Supply Current, Operating	t_{RC} = t_{RC} (min.)	60 70 80	- - -	1080 900 765	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs ≥ V_{SS}		-	18	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	t_{RC} = t_{RC} (min.)	60 70 80	- - -	1080 900 765	mA	1,3
I_{CC4}	V_{CC} Supply Current, Fast Page mode	t_{PC} = t_{PC} (min.)	60 70 80	- - -	630 540 450	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ V_{CC}–0.2V	 L-part	- -	9 2.6	mA	 5
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC} = t_{RC} (min.)	60 70 80	- - -	1080 900 765	mA	1,3
I_{CC7}	V_{CC} Supply Current, Battery Back Up (L-part only)	t_{RC} = 125μs, $\overline{CAS}$ = CBR cycling or 0.2V, $\overline{OE}$ & $\overline{WE}$ = V_{CC}–0.2V, A0-A10 = V_{CC}–0.2V or 0.2V, DQ0-DQ35 = V_{CC}–0.2V, 0.2V, or open	t_{RAS} ≤ 300ns t_{RAS} ≤ 1μs	- -	2.7 4.5	mA	1,4,5
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH} = –5mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
4. Only t_{RAS}(max.) = 1μs is applied to refresh of battery backup but t_{RAS}(max.) = 10μs is applied to normal functional operation.
5. I_{CC5}(max.) = 3.6mA and I_{CC7} are applied to L-part only (HYM536410BLM and HYM536410BLMG).

AC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V±10%, V_{SS} = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM536410BM/BLM/MG/BLMG						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	180	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	85	-	95	-	100	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	18	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,9,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	4
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	18	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	400K	70	400K	80	400K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	15	-	18	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	15	10K	18	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	52	20	60	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	50	-	55	-	60	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	45	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	15	-	18	-	20	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	15	-	18	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		L-part	-	256	-	256	-	256	ms	11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM536410BM/BLM/BMG/BLMG						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40	-	45	-	45	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	85	-	95	-	105	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	55	-	60	-	65	-	ns	8
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	15	-	15	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	10	-	15	-	15	-	ns	
49	tOEA	$\overline{OE}$ Access Time	0	15	0	18	0	20	ns	
50	tOED	$\overline{OE}$ to Data Delay	15	-	15	-	15	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	15	0	15	0	15	ns	
52	tOEH	$\overline{OE}$ Command Hold Time	15	-	15	-	15	-	ns	
53	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	60	-	65	-	70	-	ns	8
54	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
55	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initilization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
3. Refer to the HY5117400 data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. t_{REF}(max.) = 256ms is applied to L-part only (HYM536410BLM and HYM536410BLMG).

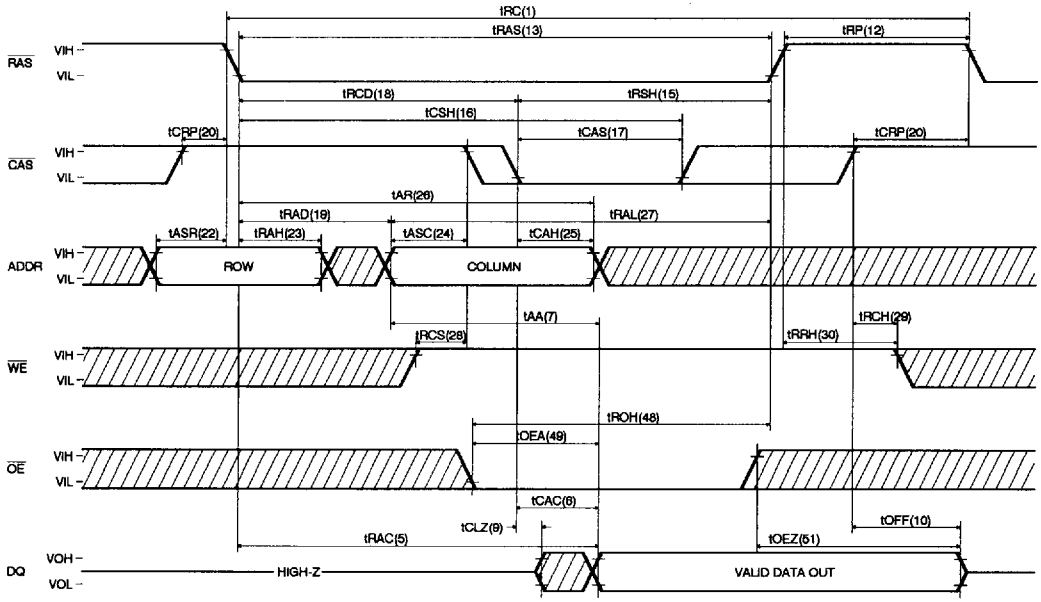
CAPACITANCE

(T_A = 25°C, V_{CC} = 5V±10%, V_{SS} = 0V, f = 1MHz, unless otherwise noted.)

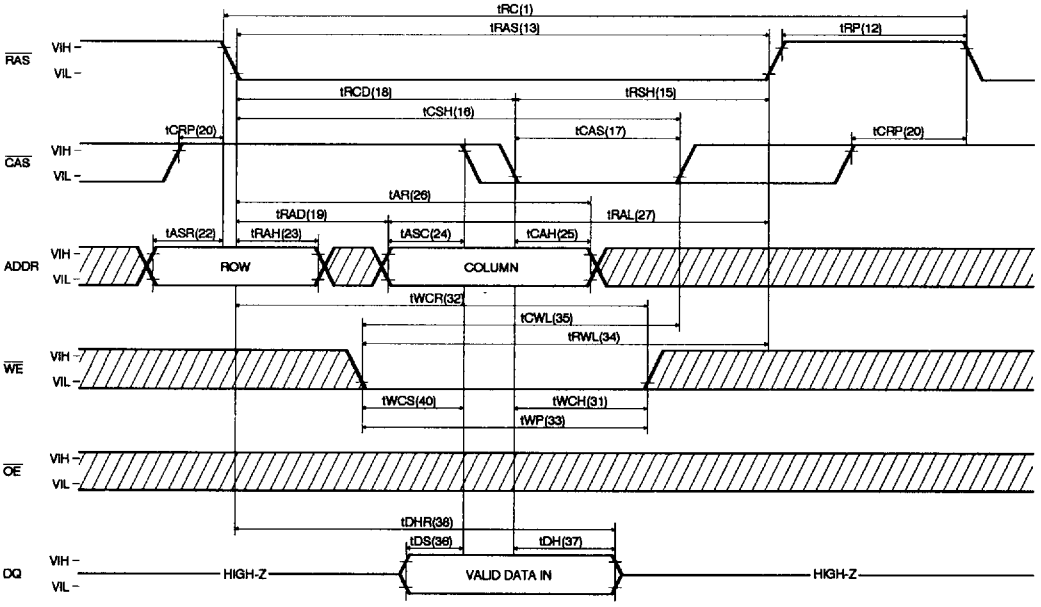
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10)	-	70	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	-	80	pF
C_{DQ}	Data Input/Output Capacitance (DQ0-DQ35)	-	17	pF

TIMING DIAGRAM

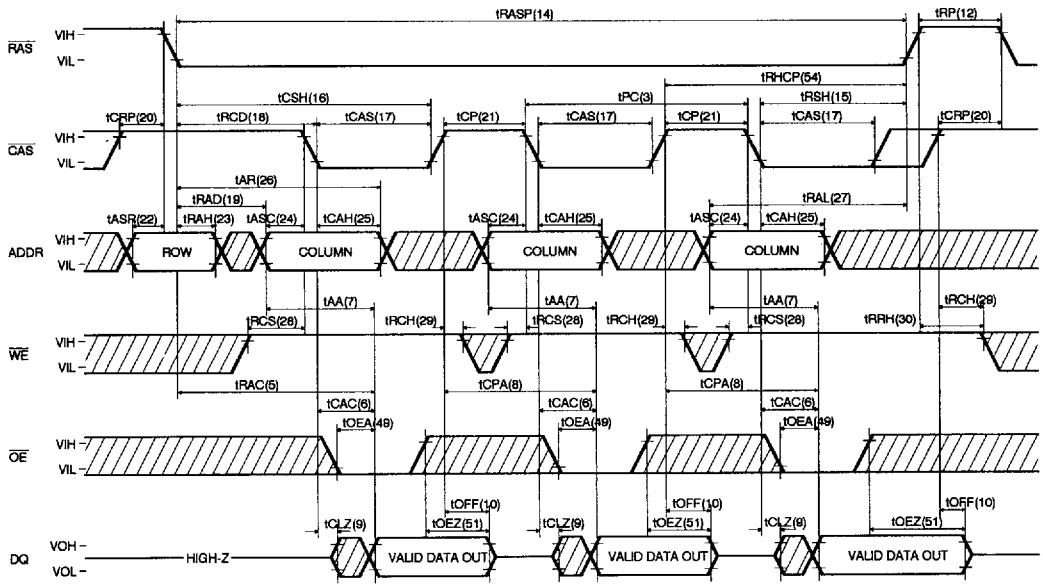
READ CYCLE



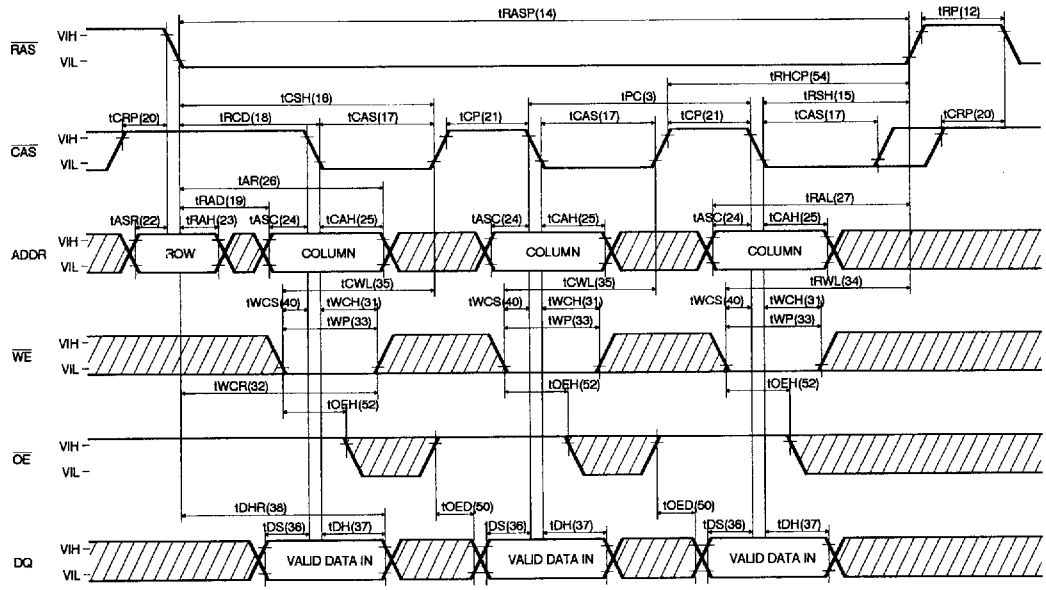
EARLY WRITE CYCLE



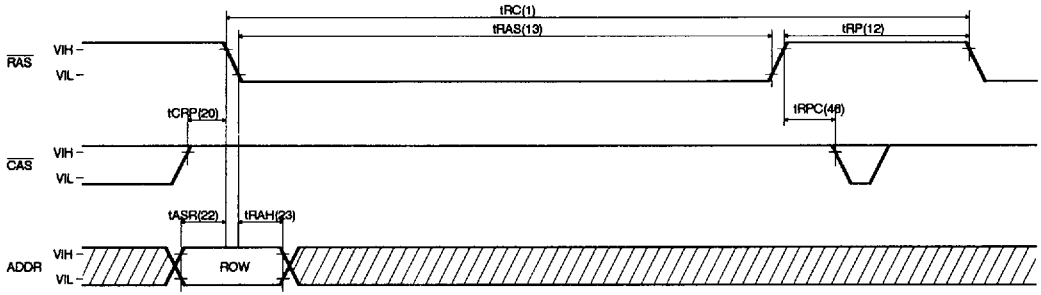
FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE

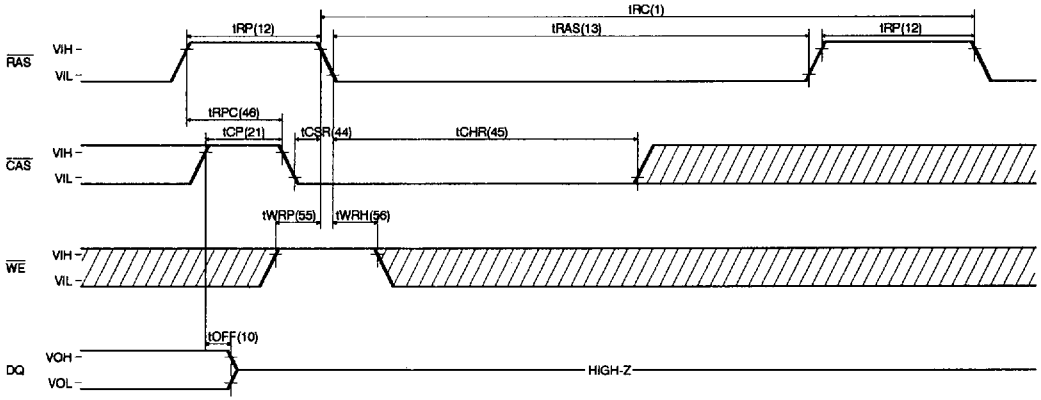


RAS-ONLY REFRESH CYCLE



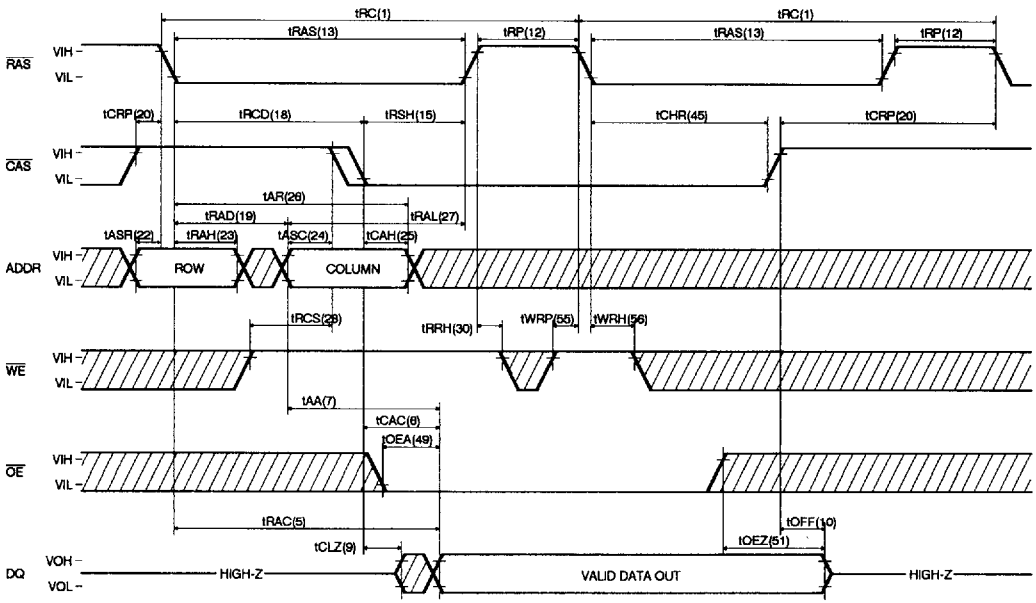
NOTE : $\overline{WE}$ and $\overline{OE}$ = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

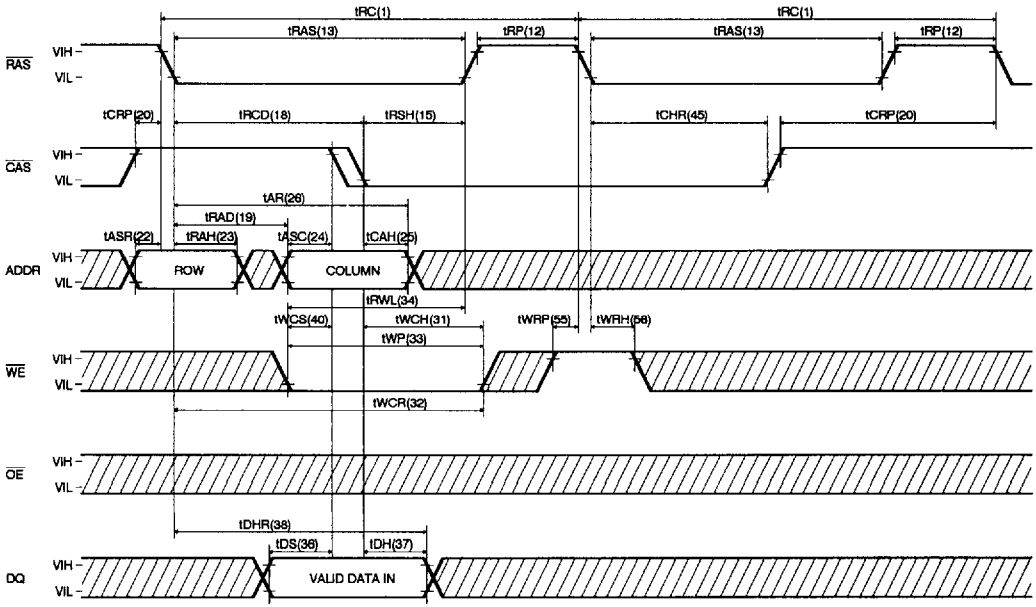


NOTE : ADDR and $\overline{OE}$ = "H" or "L"

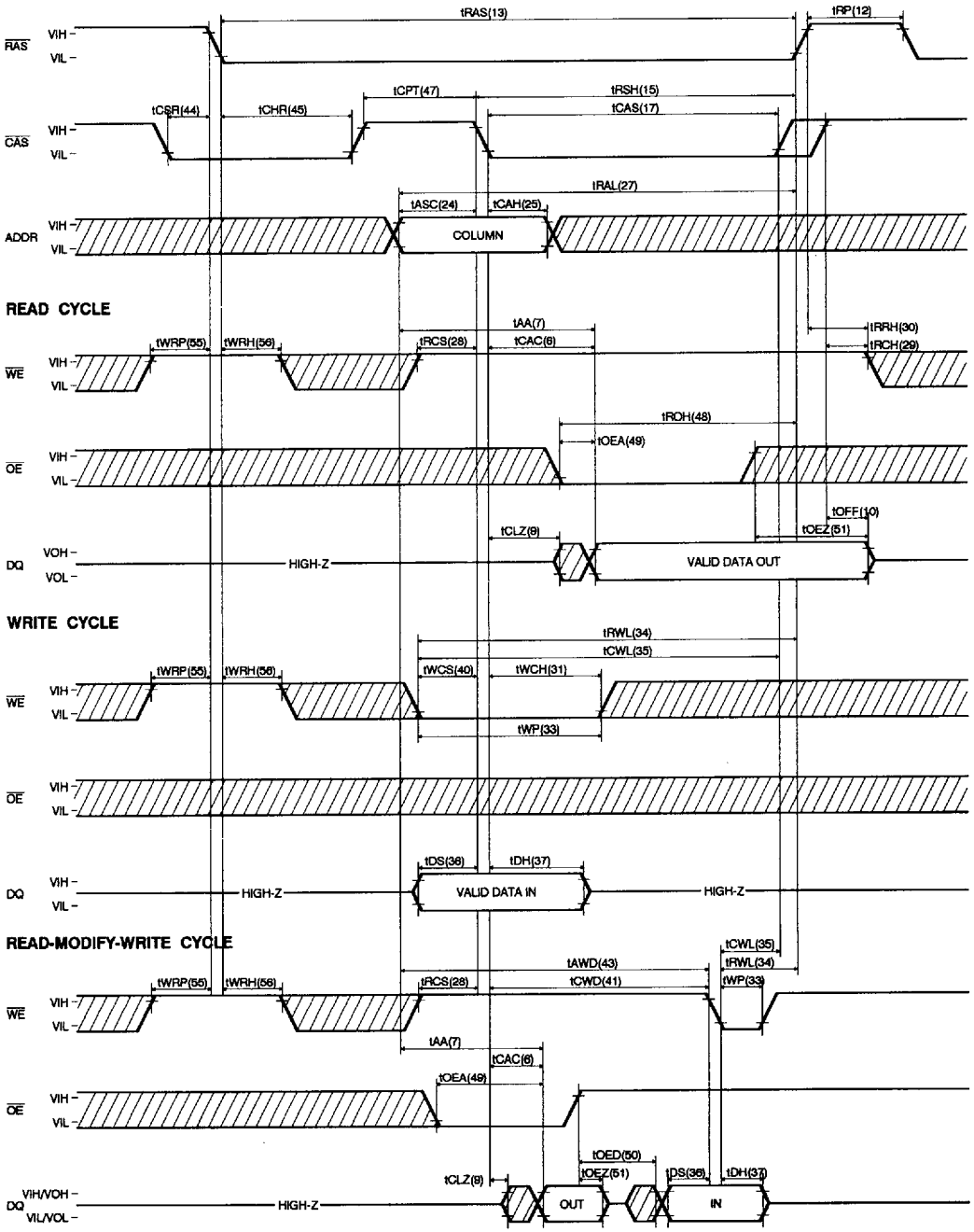
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

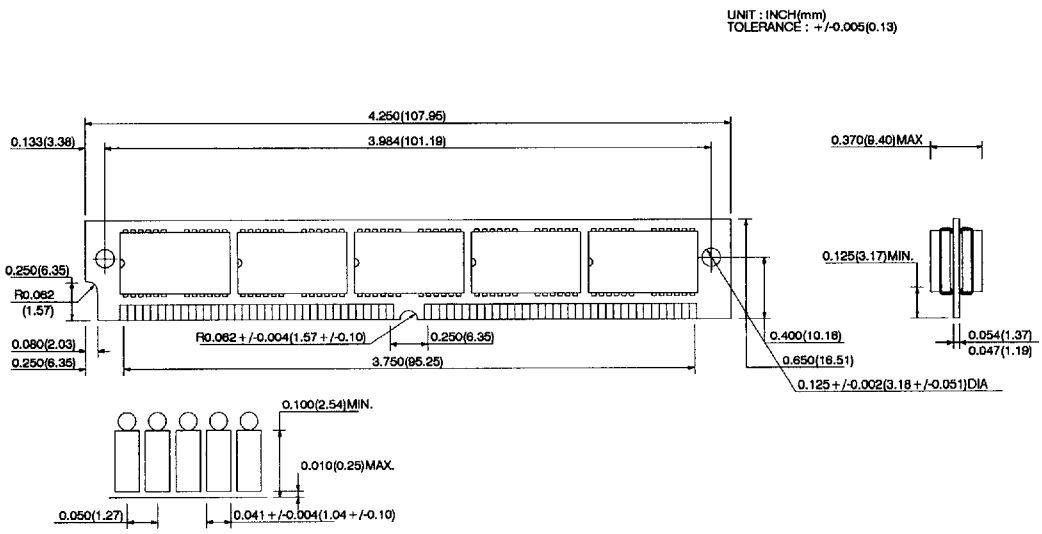


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE INFORMATION

72 pin Single In-line Memory Module (M ; Tin-Lead plated, MG ; Gold plated)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM536410BM	60/70/80		SIMM	Tin-Lead
HYM536410BLM	60/70/80	L-part	SIMM	Tin-Lead
HYM536410BMG	60/70/80		SIMM	Gold
HYM536410BLMG	60/70/80	L-part	SIMM	Gold