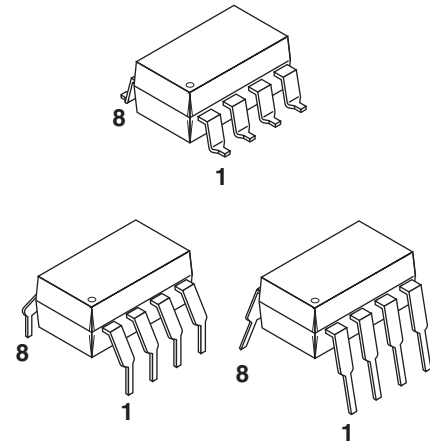


**DESCRIPTION**

The FOD2200 is an optically coupled logic gate that combine an AlGaAs LED and an integrated high gain photo detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter.

The Electrical and Switching Characteristics of the FOD2200 are guaranteed over the temperature range of 0°C to 85°C and a  $V_{CC}$  range of 4.5 volts to 20 volts. Low  $I_F$  and wide  $V_{CC}$  range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a maximum propagation delay of 300 nsec. The FOD2200 is useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

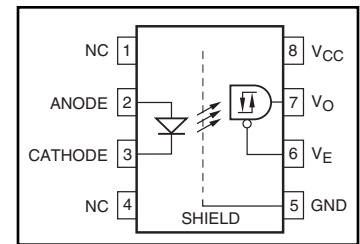


**FEATURES**

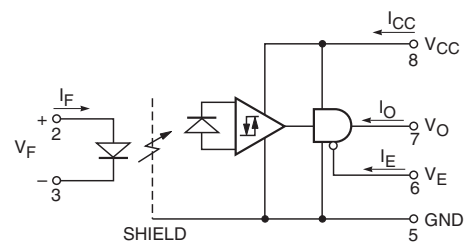
- 1 kV/ $\mu$ s Minimum Common Mode Rejection
- Compatible with LSTTL, TTL, and CMOS Logic
- Wide  $V_{CC}$  Range (4.5 to 20 V)
- 2.5 Mbd Guaranteed over Temperature
- Low Input Current (1.6 mA)
- Three State Output (No Pullup Resistor Required)
- Guaranteed Performance from 0°C to 85°C
- Hysteresis
- Safety Approvals Pending – UL, CSA, VDE
- $V_{ISO} = 5kVRMS$

**APPLICATION**

- Isolation of High Speed Logic Systems
- Computer-Peripheral Interfaces
- Microprocessor System Interfaces
- Ground Loop Elimination
- Pulse Transformer Replacement
- Isolated Bus Driver
- High Speed Line Receiver



**Schematic**



**TRUTH TABLE (Positive Logic)**

LED	Enable	Output
On	H	Z
Off	H	Z
On	L	H
Off	L	L

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise specified)			
Parameter	Symbol	Value	Units
Storage Temperature	$T_{STG}$	-40 to +125	$^\circ\text{C}$
Operating Temperature	$T_{OPR}$	-40 to +85	$^\circ\text{C}$
Lead Solder Temperature (1.6mm below seating plane)	$T_{SOL}$	260 for 10 sec	$^\circ\text{C}$
<b>EMITTER</b>			
Peak Transient Input Current ( $\leq 1\mu\text{s}$ PW, 300 pps)	$I_F(PK)$	1.0	A
Average Forward Input Current	$I_F$	10	mA
Reverse Input Voltage	$V_R$	5.0	V
Output Power Dissipation (No derating required up to $85^\circ\text{C}$ )	$P_D$	45	mW
<b>DETECTOR</b>			
Supply Voltage	$V_{CC}$	0 to 20	V
Average Output Current	$I_O$	25	mA
Three State Enable Voltage	$V_E$	-0.5 to 20	V
Output Voltage	$V_O$	-0.5 to 20	V
Output Power Dissipation (No derating required up to $85^\circ\text{C}$ )	$P_D$	150	mW

<b>RECOMMENDED OPERATING CONDITIONS</b>				
Parameter	Symbol	Min	Max	Units
Forward Input Current	$I_{F(ON)}$	1.6*	5	mA
Forward Input Current	$I_{F(OFF)}$		0.1	mA
Supply Voltage, Output	$V_{CC}$	4.5	20	V
Enable Voltage, Low Level	$V_{EL}$	0	0.8	V
Enable Voltage, High Level	$V_{EH}$	2.0	20	V
Operating Temperature	$T_A$	0	+85	$^\circ\text{C}$
Fan Out (TTL load)	N		4	

\*The initial switching threshold is 1.6mA or less. It is recommended that 2.2 mA be used to permit at least a 20% CTR degradation guardband.

**ELECTRICAL CHARACTERISTICS** ( $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $20\text{V}$ ,  $I_{F(ON)} = 1.6\text{mA}$  to  $5\text{mA}$ ,  $V_{EH} = 2\text{V}$  to  $20\text{V}$ ,  $V_{EL} = 0\text{V}$  to  $0.8\text{V}$ ,  $I_{F(OFF)} = 0\text{mA}$  to  $0.1\text{mA}$  Unless otherwise specified.) See Note 1.

**INDIVIDUAL COMPONENT CHARACTERISTICS**

Parameter	Test Conditions	Symbol	Min	Typ**	Max	Unit	
<b>EMITTER</b>							
Input Forward Voltage	( $I_F = 5\text{mA}$ )	$V_F$			1.75	V	
	$T_A = 25^\circ\text{C}$			1.40	1.7		
Input Reverse Breakdown Voltage	( $I_R = 10\ \mu\text{A}$ )	$B_{VR}$	5.0			V	
Input Capacitance	(Pins 2 & 3) ( $V_F = 0$ , $f = 1\text{MHz}$ )	$C_{IN}$		60		pF	
Input Diode Temperature Coefficient	( $I_F = 5\text{mA}$ )	$\Delta V_F/\Delta T_A$		-1.4		mV/ $^\circ\text{C}$	
<b>DETECTOR</b>							
High Level Supply Current	( $I_F = 5\text{mA}$ ) ( $I_O = \text{Open}$ , $V_E = \text{Don't care}$ )	$I_{CCH}$		$V_{CC} = 5.5\text{V}$	3.5	4.5	mA
				$V_{CC} = 20\text{V}$	4.0	6.0	
Low Level Supply Current	( $I_F = 0$ ) ( $I_O = \text{Open}$ , $V_E = \text{Don't care}$ )	$I_{CCL}$		$V_{CC} = 5.5\text{V}$	4.4	6.0	mA
				$V_{CC} = 20\text{V}$	5.2	7.5	
Low Level Enable Current		$I_{EL}$		-0.1	-0.32	mA	
High Level Enable Current		$I_{EH}$		$V_E = 0.4\text{V}$		20	$\mu\text{A}$
				$V_E = 2.7\text{V}$		100	
				$V_E = 5.5\text{V}$	0.005	250	
				$V_E = 20\text{V}$			
High Level Enable Voltage		$V_{EH}$	2.0			V	
Low Level Enable Voltage		$V_{EL}$			0.8	V	

**SWITCHING CHARACTERISTICS** ( $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $I_{F(ON)} = 1.6\text{mA}$  to  $5\text{mA}$ ,  $I_{F(OFF)} = 0$  to  $0.1\text{mA}$ ,  $V_{CC} = 4.5$  to  $20\text{V}$  Unless otherwise specified.)

AC Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Propagation Delay Time to Output High Level	(Note 2, 4) (Fig. 1) With Peaking Capacitor	$T_{PLH}$		120	300	ns
Propagation Delay Time to Output Low Level	(Note 3, 4) (Fig. 1) With Peaking Capacitor	$T_{PHL}$		180	300	ns
Output Rise Time (10-90%)	(Note 5) (Fig. 1)	$t_r$		80		ns
Output Fall Time (90-10%)	(Note 6) (Fig. 1)	$t_f$		25		ns
Enable Propagation Delay Time to Output High Level	(Fig. 2)	$t_{PZH}$		40		ns
Enable Propagation Delay Time to Output Low Level	(Fig. 2)	$t_{PZL}$		50		ns
Disable Propagation Delay Time from Output High Level	(Fig. 2)	$T_{PHZ}$		95		ns
Disable Propagation Delay Time from Output Low Level	(Fig. 2)	$T_{PLZ}$		80		ns
Common Mode Transient Immunity (at Output High Level)	( $T_A = 25^\circ\text{C}$ ) ( $I_F = 1.6\text{mA}$ , $V_{OH}(\text{Min.}) = 2.0\text{V}$ ) $V_{CC} = 5\text{V}$ (Note 7)(Fig. 3)	$ V_{CM}  = 50\text{V}$	$ICM_H$	1000		V/ $\mu\text{s}$
Common Mode Transient Immunity (at Output Low Level)	( $T_A = 25^\circ\text{C}$ ) ( $I_F = 0\text{mA}$ , $V_{OL}(\text{Max.}) = 0.8\text{V}$ ) $V_{CC} = 5\text{V}$ (Note 8)(Fig. 3)	$ V_{CM}  = 50\text{V}$	$ICM_L$	1000		V/ $\mu\text{s}$

\*\* Typical values at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $I_{F(ON)} = 3\text{mA}$  unless otherwise specified.

**TRANSFER CHARACTERISTICS** ( $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $20\text{V}$ ,  $I_{F(ON)} = 1.6\text{mA}$  to  $5\text{mA}$ ,  $V_{EH} = 2\text{V}$  to  $20\text{V}$ ,  $V_{EL} = 0\text{V}$  to  $0.8\text{V}$ ,  $I_{F(OFF)} = 0\text{mA}$  to  $0.1\text{mA}$  Unless otherwise specified.) See Note 1.

DC Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Output Leakage Current ( $V_{OUT} > V_{CC}$ )	$(V_{CC} = 4.5\text{V}) \frac{V_O = 5.5\text{V}}{(I_F = 5\text{mA}) \quad V_O = 20\text{V}}$	$I_{OHH}$		2.0 2.5	100 500	$\mu\text{A}$
Low Level Output Voltage	$(V_{CC} = 4.5\text{V}, I_F = 0\text{mA})$ $(V_E = 0.4\text{V}, I_{OL} = 6.4\text{mA})$ (Note 2)	$V_{OL}$		0.33	0.5	V
Input Threshold Current	$(V_{CC} = 4.5\text{V}, V_O = 0.5\text{V},$ $V_E = 0.4\text{V}, I_{OL} = 6.4\text{mA})$	$I_{FT}$			1.6	mA
Logic High Output Voltage	$I_{OH} = -2.6\text{mA}$	$V_{OH}$	2.4	$V_{CC}-1.8$		V
High Impedance State Output Current	$V_O = 0.4\text{V}, V_{EN} = 2\text{V}, I_F = 5\text{mA}$	$I_{OZL}$			-20	$\mu\text{A}$
	$V_O = 2.4\text{V}, V_{EN} = 2\text{V}, I_F = 5\text{mA}$	$I_{OZH}$			20	$\mu\text{A}$
	$V_O = 5.5\text{V}, V_{EN} = 2\text{V}, I_F = 5\text{mA}$				100	$\mu\text{A}$
	$V_O = 20\text{V}, V_{EN} = 2\text{V}, I_F = 5\text{mA}$				500	$\mu\text{A}$
Logic Low Short Circuit Output Current Note 10	$V_O = V_{CC} = 5.5\text{V}, I_F = 0\text{mA}$	$I_{OSL}$	25			mA
	$V_O = V_{CC} = 20\text{V}, I_F = 0\text{mA}$		40			mA
Logic High Short Circuit Output Current Note 10	$V_{CC} = 5.5\text{V}, I_F = 5\text{mA}, V_O = \text{GND}$	$I_{OSH}$	-10			mA
	$V_{CC} = 20\text{V}, I_F = 5\text{mA}, V_O = \text{GND}$		-25			mA
Input Current Hysteresis	$V_{CC} = 4.5\text{V}$	$I_{HYS}$		0.03		mA

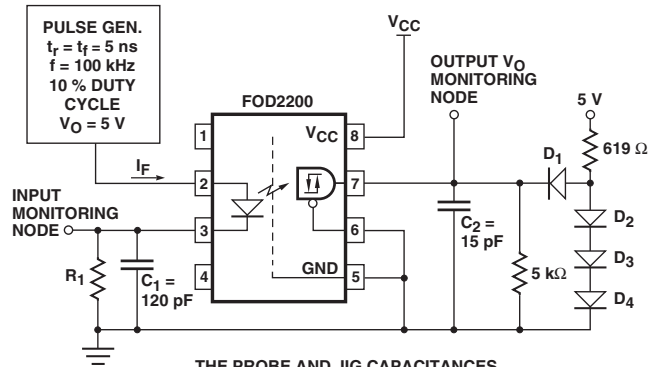
**ISOLATION CHARACTERISTICS** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  Unless otherwise specified.)

Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Withstand Insulation Test Voltage	$(R_H < 50\%, T_A = 25^\circ\text{C})$ $t = 1\text{min}$ (Note 9)	$V_{ISO}$	5000			$V_{RMS}$
Resistance (Input to Output)	$(V_{I-O} = 500\text{VDC})$ (Note 9)	$R_{I-O}$		$10^{12}$		$\Omega$
Capacitance (Input to Output)	$(V_{I-O} = 0\text{V}, f = 1\text{MHz})$ (Note 9)	$C_{I-O}$		0.6		pF

\*\* Typical values at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $I_{F(ON)} = 3\text{mA}$  unless otherwise stated.

**NOTES**

1. The  $V_{CC}$  supply to each optoisolator must be bypassed by a  $0.1\mu\text{F}$  capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package  $V_{CC}$  and GND pins of each device.
2.  $t_{PLH}$  - Propagation delay is measured from the 50% level on the LOW to HIGH transition of the input current pulse to the 1.3V level on the LOW to HIGH transition of the output voltage pulse.
3.  $t_{PHL}$  - Propagation delay is measured from the 50% level on the HIGH to LOW transition of the input current pulse to the 1.3V level on the HIGH to LOW transition of the output voltage pulse.
4. When the peaking capacitor is omitted, propagation delay times may increase by 100 ns.
5.  $t_r$  - Rise time is measured from the 10% to the 90% levels on the LOW to HIGH transition of the output pulse.
6.  $t_f$  - Fall time is measured from the 90% to the 10% levels on the HIGH to LOW transition of the output pulse.
7.  $CM_H$  - The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the high state (i.e.,  $V_{OUT} > 2.0\text{ V}$ ).
8.  $CM_L$  - The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the low state (i.e.,  $V_{OUT} < 0.8\text{ V}$ ).
9. Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together, and Pins 5,6,7 and 8 shorted together.
10. Duration of output short circuit time should not exceed 10 ms.



THE PROBE AND JIG CAPACITANCES ARE INCLUDED IN  $C_1$  AND  $C_2$ .

$R_1$	2.15 k $\Omega$	1.10 k $\Omega$	681 $\Omega$
$I_F$ (ON)	1.6 mA	3 mA	5 mA

ALL DIODES ARE 1N916 OR 1N3064.

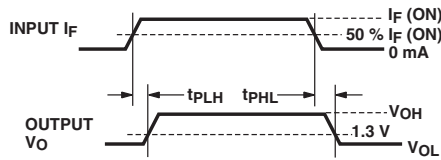
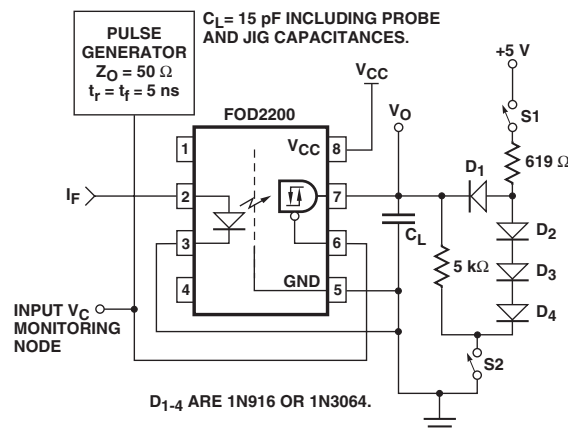


Fig. 1. Test Circuit and Waveforms for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$  and  $t_f$ .



$D_{1-4}$  ARE 1N916 OR 1N3064.

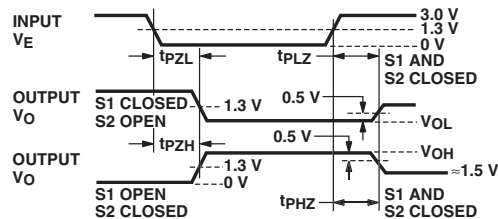
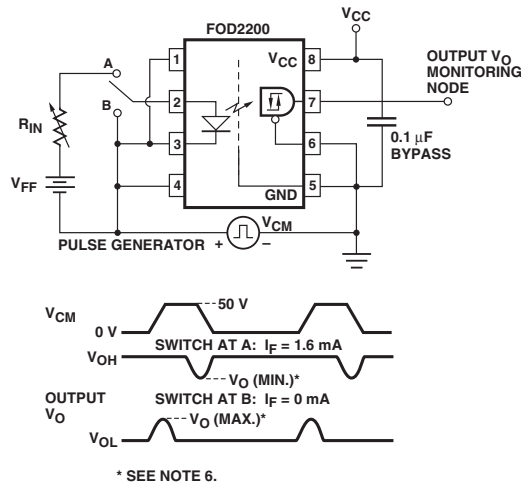
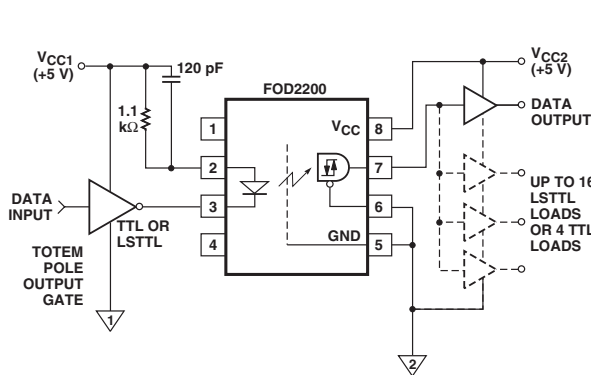


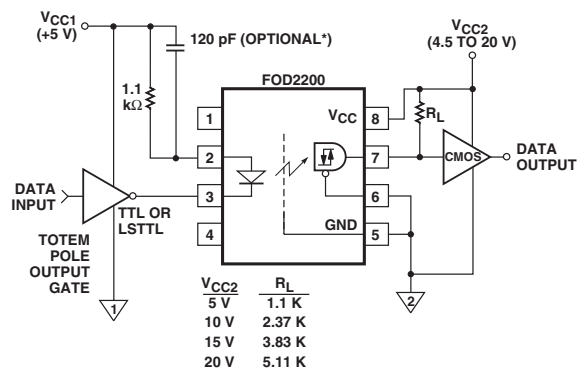
Fig. 2. Test Circuit and Waveforms for  $t_{PHZ}$ ,  $t_{PZH}$ ,  $t_{PLZ}$ , and  $t_{PZL}$ .



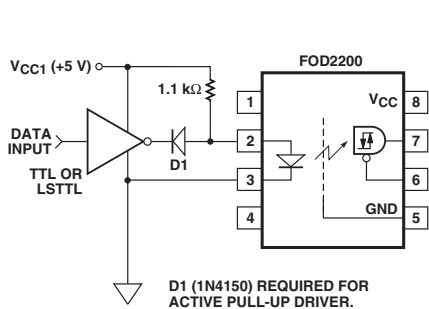
**Fig. 3. Test Circuit and Typical Waveforms for Common Mode Transient Immunity**



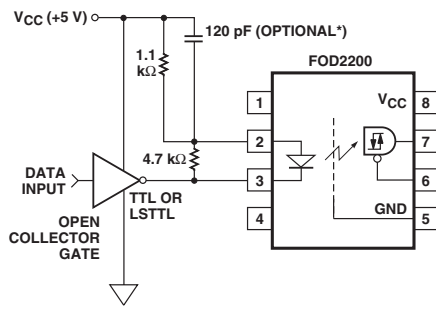
**Figure 4. Recommended LSTTL to LSTTL Circuit.**



**Figure 5. LSTTL to CMOS Interface Circuit.**



**Figure 6. Recommended LED Drive Circuit.**

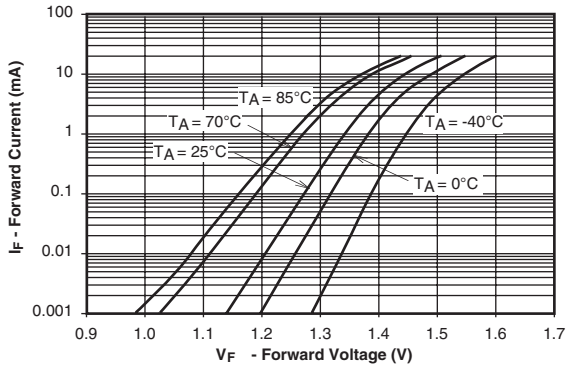


**Figure 7. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I<sub>OH</sub> from the LED).**

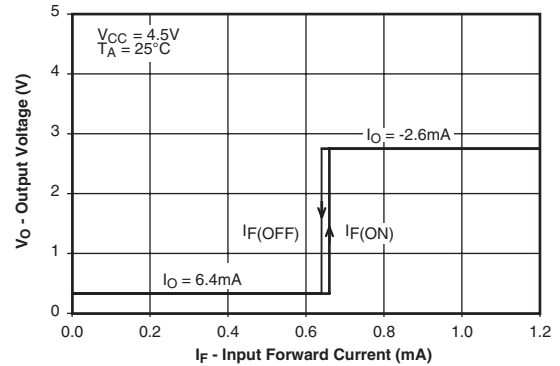
\*The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.

**TYPICAL PERFORMANCE CURVES**

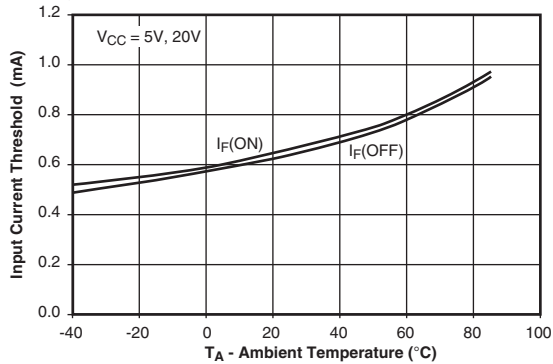
**Figure 8. Input Forward Current vs Forward Voltage**



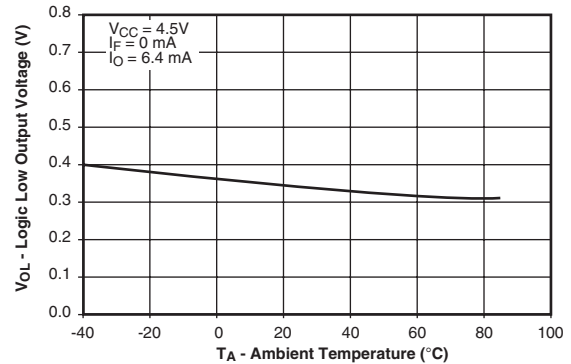
**Figure 9. Output Voltage vs. Input Forward Current**



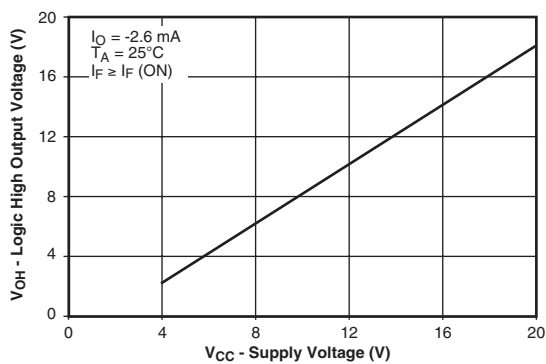
**Figure 10. Input Threshold Current vs. Ambient Temperature**



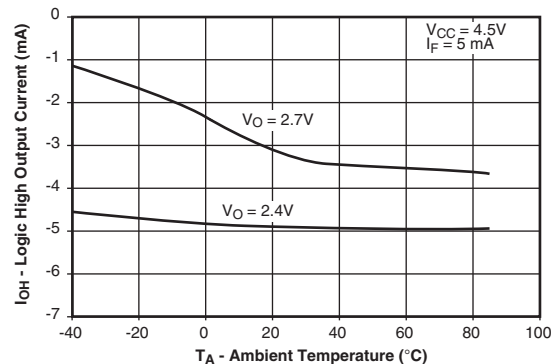
**Figure 11. Logic Low Output Voltage vs. Ambient Temperature**



**Figure 12. Logic High Output Voltage vs. Supply Voltage**



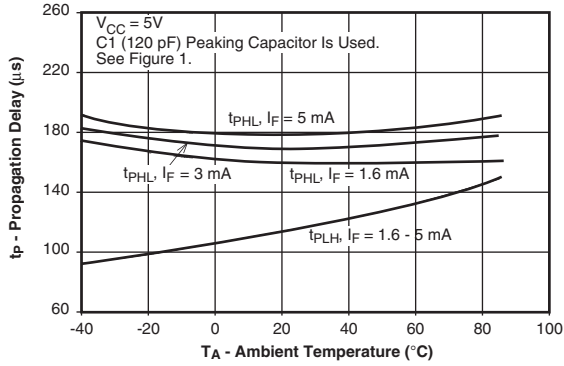
**Figure 13. Logic High Output Current vs. Ambient Temperature**



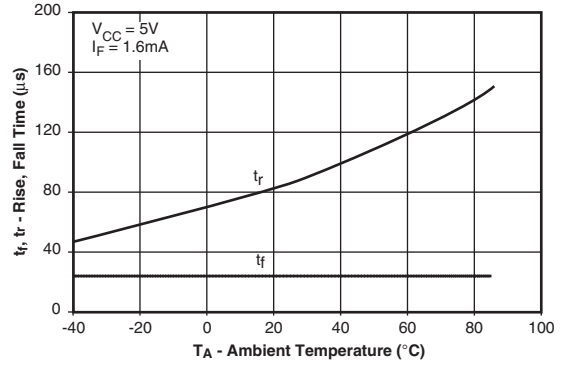


**TYPICAL PERFORMANCE CURVES**

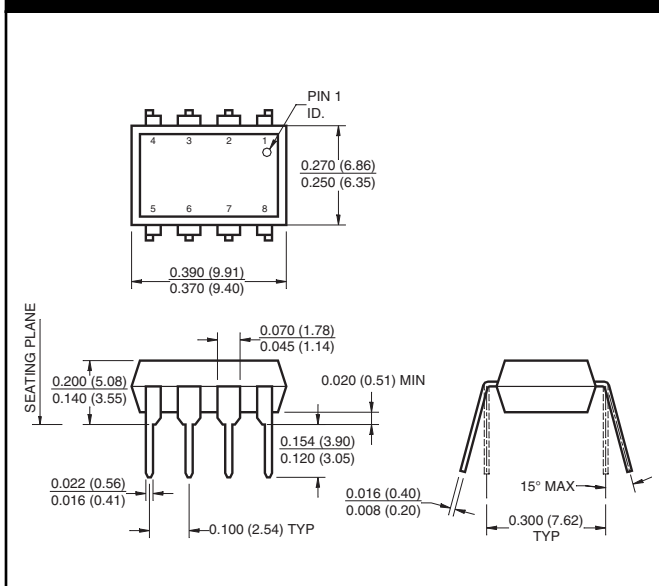
**Figure 14. Propagation Delay vs Ambient Temperature**



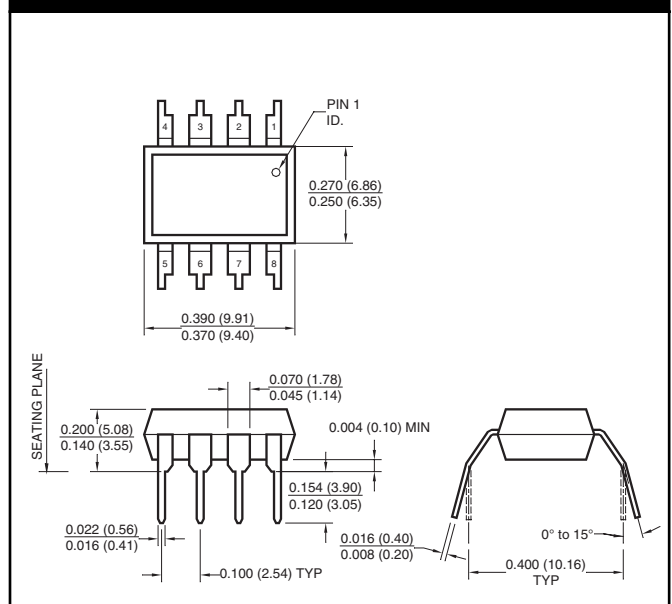
**Figure 15. Rise, Fall Time vs Ambient Temperature**



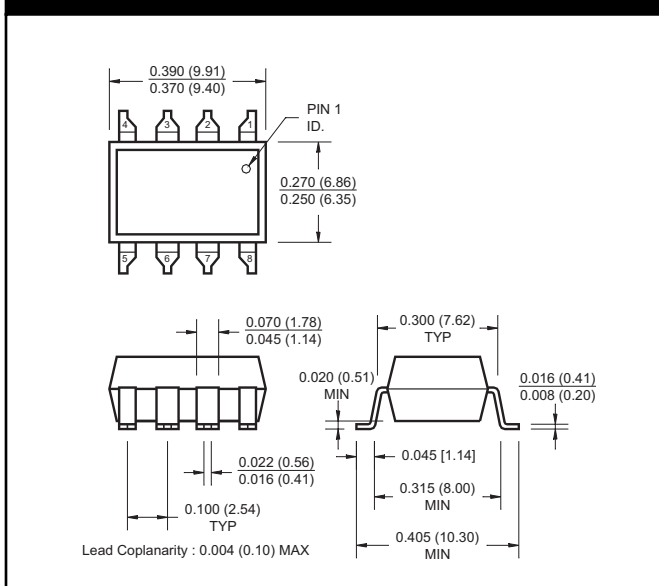
**Package Dimensions (Through Hole)**



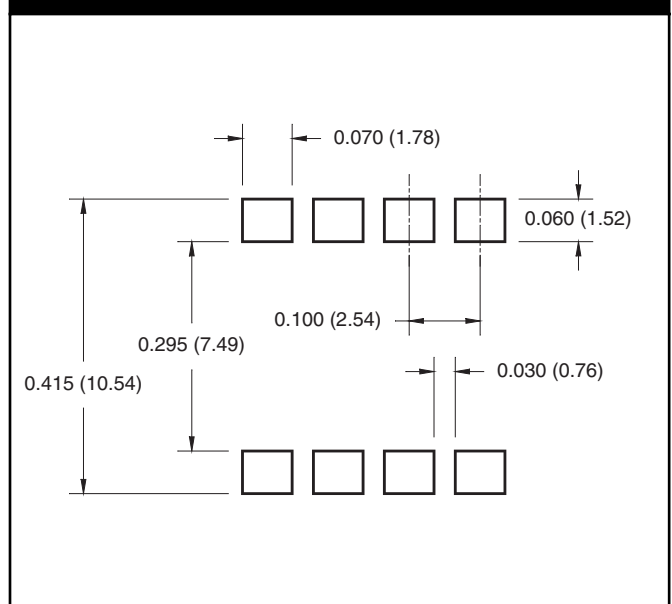
**Package Dimensions (0.4" Lead Spacing)**



**Package Dimensions (Surface Mount)**



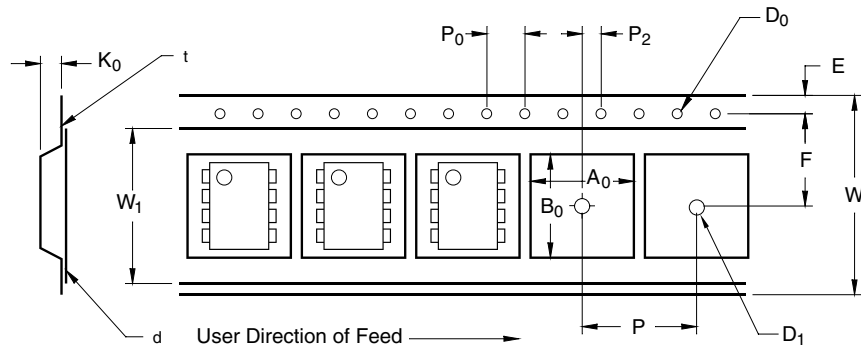
**8 - Pin Dip**



**NOTE**

All dimensions are in inches (millimeters)

**Carrier Tape Specifications**



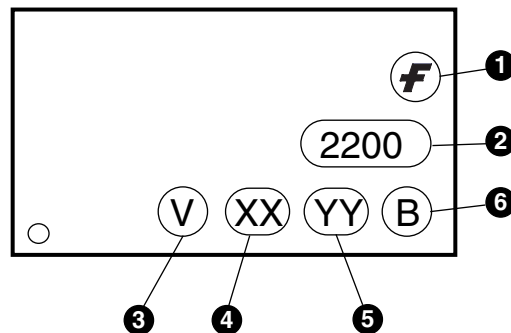
Description	Symbol	Dimension in mm
Tape Width	W	16.0 ± 0.3
Tape Thickness	t	0.30 ± 0.05
Sprocket Hole Pitch	P <sub>0</sub>	4.0 ± 0.1
Sprocket Hole Diameter	D <sub>0</sub>	1.55 ± 0.05
Sprocket Hole Location	E	1.75 ± 0.10
Pocket Location	F	7.5 ± 0.1
	P <sub>2</sub>	4.0 ± 0.1
Pocket Pitch	P	12.0 ± 0.1
Pocket Dimensions	A <sub>0</sub>	10.30 ± 0.20
	B <sub>0</sub>	10.30 ± 0.20
	K <sub>0</sub>	4.90 ± 0.20
Cover Tape Width	W <sub>1</sub>	1.6 ± 0.1
Cover Tape Thickness	d	0.1 max
Max. Component Rotation or Tilt		10°
Min. Bending Radius	R	30

**ORDERING INFORMATION**

Example: FOD2200 X

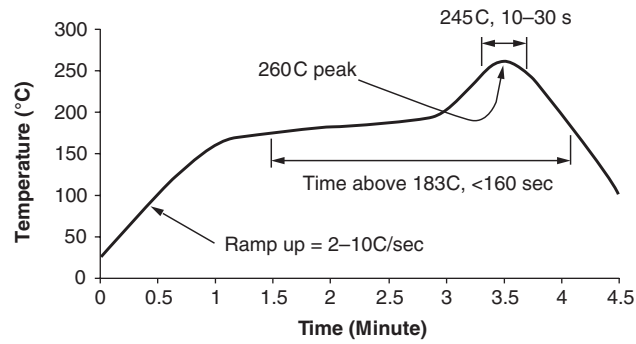
X
<b>Packaging Option</b>
S: Surface Mount Lead Bend
SD: Surface Mount, Tape and Reel
T: 0.4" Lead Spacing
V: VDE 0884
TV: VDE 0884, 0.4" Lead Spacing
SV: VDE 0884, Surface Mount
SDV: VDE 0884, Surface Mount, Tape and Reel

**MARKING INFORMATION**



Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	Two digit year code, e.g., '03'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

**Reflow Profile**



- Peak reflow temperature: 260C (package surface temperature)
- Time of temperature higher than 183C for 160 seconds or less
- One time soldering reflow is recommended

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.