



**8-Mbit (512K x 16) MoBL<sup>®</sup> Static RAM**

**Features**

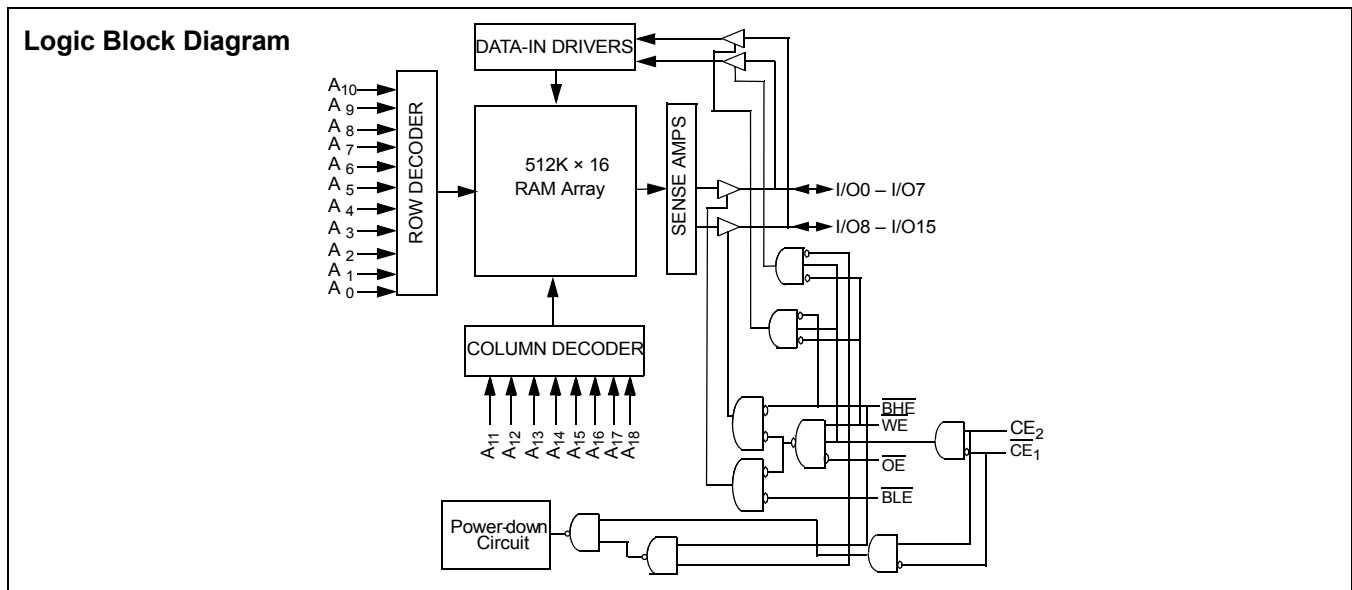
- **Temperature Ranges**
  - Industrial: -40°C to 85°C
  - Automotive: -40°C to 125°C (Preliminary)
- **Very high speed: 45 ns, 55 ns and 70 ns**
- **Wide voltage range: 2.20V – 3.60V**
- **Pin-compatible with CY62157CV25, CY62157CV30, and CY62157CV33**
- **Ultra-low active power**
  - Typical active current: 1.5 mA @ f = 1 MHz
  - Typical active current: 12 mA @ f = f<sub>max</sub>
- **Ultra-low standby power**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered: 48-ball BGA, 48-pin TSOP1, and 44-pin TSOP1I**

**Functional Description<sup>[1]</sup>**

The CY62157DV30 is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode when deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW or both BHE and BLE are HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH and WE LOW).

Writing to the device is accomplished by taking Chip Enables ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

Reading from the device is accomplished by taking Chip Enables ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table for a complete description of read and write modes.

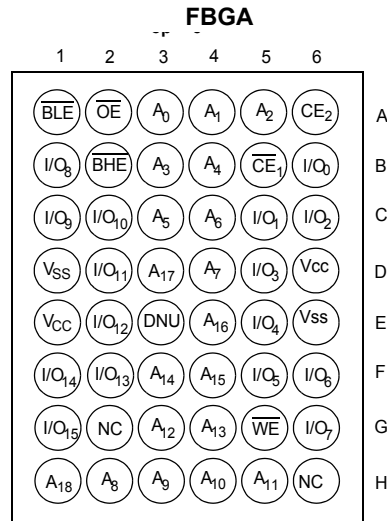


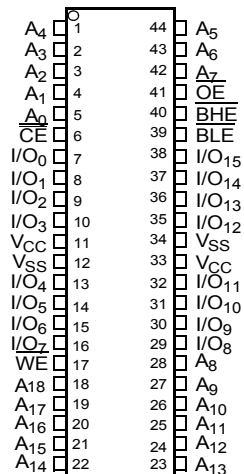
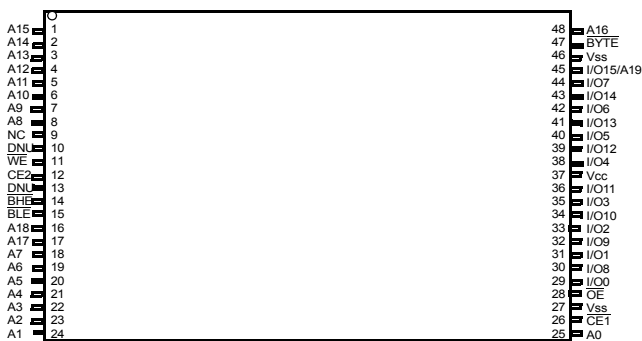
**Notes:**

1. For best practice recommendations, please refer to the Cypress application note entitled *System Design Guidelines*, which is available at <http://www.cypress.com>.

**Product Portfolio**

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
		Min.	Typ. <sup>[2]</sup>	Max.		f = 1MHz		f = f <sub>max</sub>			
						Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.
CY62157DV30L	Industrial	2.2	3.0	3.6	45, 55, 70	1.5	3	12	20	2	20
CY62157DV30LL	Industrial	2.2	3.0	3.6	45, 55, 70	1.5	3	12	15	2	8
CY62157DV30L	Automotive <sup>[3]</sup>	2.2	3.0	3.6	55	1.5	3	12	20	2	50

**Pin Configuration<sup>[4, 5, 6, 7]</sup>**

**48TSOPI**  
 Top View

**44 TSOP II**  
 Top View

**Notes:**

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.
- Automotive data is PRELIMINARY. Shaded areas of the datasheet contain PRELIMINARY information.
- NC pins are not internally connected on the die.
- DNU pins have to be left floating.
- The BYTE pin in the 48-TSOPI package has to be tied HIGH to use the device as a 512K × 16 SRAM. The 48-TSOPI package can also be used as a 1M × 8 SRAM by tying the BYTE signal LOW. For 1M × 8 Functionality, please refer to the CY62158DV30 datasheet. In the 1M × 8 configuration, Pin 45 is A19.
- The 44-TSOPII package device has only one chip enable pin (CE).



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to + 150°C
- Ambient Temperature with Power Applied..... -55°C to + 125°C
- Supply Voltage to Ground Potential ..... -0.3V to + V<sub>CC(max)</sub> + 0.3V
- DC Voltage Applied to Outputs in High-Z State<sup>[8, 9]</sup> ..... -0.3V to V<sub>CC(max)</sub> + 0.3V
- DC Input Voltage<sup>[8, 9]</sup> ..... -0.3V to V<sub>CC(max)</sub> + 0.3V

- Output Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)
- Latch-up Current..... >200 mA

**Operating Range**

Device	Range	Ambient Temperature (T <sub>A</sub> )	V <sub>CC</sub> <sup>[10]</sup>
CY62157DV30L	Industrial	-40°C to +85°C	2.20V to 3.60V
CY62157DV30LL			
CY62157DV30L	Automotive (Preliminary)	-40°C to +125°C	

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	CY62157DV30			Unit	
			Min.	Typ. <sup>[2]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA, V <sub>CC</sub> = 2.20V	2.0			V	
		I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> = 2.70V	2.4			V	
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA, V <sub>CC</sub> = 2.20V			0.4	V	
		I <sub>OL</sub> = 2.1mA, V <sub>CC</sub> = 2.70V			0.4	V	
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.2V to 2.7V	1.8		V <sub>CC</sub> + 0.3V	V	
		V <sub>CC</sub> = 2.7V to 3.6V	2.2		V <sub>CC</sub> + 0.3V	V	
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.2V to 2.7V	-0.3		0.6	V	
		V <sub>CC</sub> = 2.7V to 3.6V	-0.3		0.8	V	
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Industrial	-1	+1	μA	
			Automotive	-4	+4	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	Industrial	-1	+1	μA	
			Automotive	-4	+4	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = V <sub>CCmax</sub> , I <sub>OUT</sub> = 0 mA, CMOS levels	L	12	20	mA
			LL			15	mA
		f = 1 MHz	L	1.5	3	mA	
			LL			3	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V, CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V <sub>CC</sub> = 3.60V	Industrial	L	2	20	μA
			LL		2	8	
			Automotive	L			50
				LL			
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V or CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.60V	Industrial	L	2	20	μA
			LL		2	8	
			Automotive	L			50
				LL			

**Notes:**

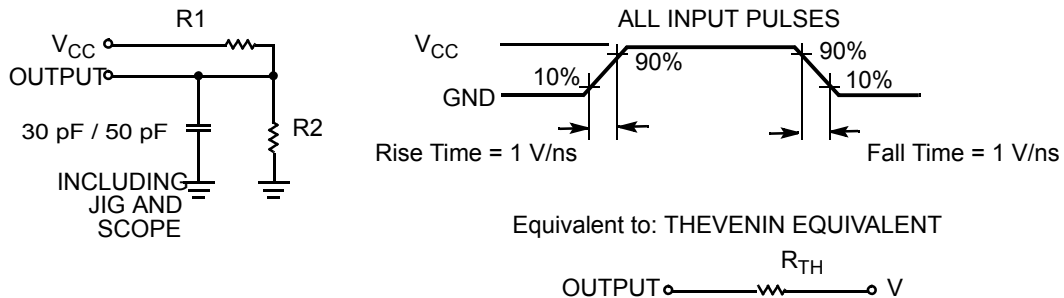
- 8. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
- 9. V<sub>IH(max.)</sub> = V<sub>CC</sub> + 0.75V for pulse duration less than 20 ns.
- 10. Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.

**Capacitance<sup>[11, 12]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(\text{typ})}$	10	pF
$C_{OUT}$	Output Capacitance		10	pF

**Thermal Resistance<sup>[11]</sup>**

Parameter	Description	Test Conditions	BGA	TSOP II	TSOP I	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	72	75.13	74.88	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		8.86	8.95	8.6	$^\circ\text{C/W}$

**AC Test Loads and Waveforms<sup>[13]</sup>**


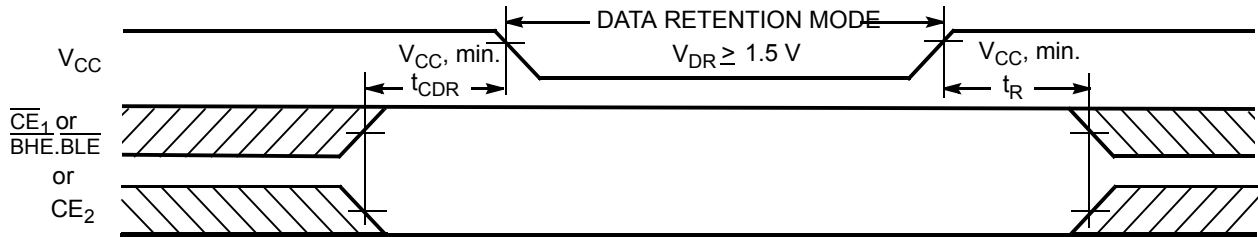
Parameters	2.50V	3.0V	Unit
R1	16667	1103	$\Omega$
R2	15385	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.20	1.75	V

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min.	Typ. <sup>[2]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.5			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.5\text{V}$ $CE_1 \geq V_{CC} - 0.2\text{V}$ , $CE_2 \leq 0.2\text{V}$ , $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	Industrial (L)		10	$\mu\text{A}$
			Industrial (LL)		4	
			Automotive (L)		25	
$t_{CDR}^{[11]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[14]}$	Operation Recovery Time		$t_{RC}$			ns

**Notes:**

11. Tested initially and after any design or process changes that may affect these parameters.
12. The input capacitance on the  $CE_2$  pin of the FBGA and 48TSOPI packages and on the BHE pin of the 44TSOPII package is 15 pF.
13. Test condition for the 45 ns part is a load capacitance of 30 pF.
14. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min.})} \geq 100\text{ us}$  or stable at  $V_{CC(\text{min.})} \geq 100\text{ us}$ .

**Data Retention Waveform<sup>[15]</sup>**

**Switching Characteristics** Over the Operating Range <sup>[16]</sup>

Parameter	Description	45 ns <sup>[13]</sup>		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
t <sub>RC</sub>	Read Cycle Time	45		55		70		ns
t <sub>AA</sub>	Address to Data Valid		45		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		10		ns
t <sub>ACE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Data Valid		45		55		70	ns
t <sub>DOE</sub>	OE LOW to Data Valid		25		25		35	ns
t <sub>LZOE</sub>	OE LOW to Low Z <sup>[17]</sup>	5		5		5		ns
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[17, 18]</sup>		15		20		25	ns
t <sub>LZCE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Low Z <sup>[17]</sup>	10		10		10		ns
t <sub>HZCE</sub>	CE <sub>1</sub> HIGH and CE <sub>2</sub> LOW to High Z <sup>[17, 18]</sup>		20		20		25	ns
t <sub>PU</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Power-Up	0		0		0		ns
t <sub>PD</sub>	CE <sub>1</sub> HIGH and CE <sub>2</sub> LOW to Power-Down		45		55		70	ns
t <sub>DBE</sub>	BLE / BHE LOW to Data Valid		45		55		70	ns
t <sub>LZBE</sub>	BLE / BHE LOW to Low Z <sup>[17]</sup>	10		10		10		ns
t <sub>HZBE</sub>	BLE / BHE HIGH to High Z <sup>[17, 18]</sup>		15		20		25	ns
<b>Write Cycle<sup>[19]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	45		55		70		ns
t <sub>SCE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Write End	40		40		60		ns
t <sub>AW</sub>	Address Set-up to Write End	40		40		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		0		ns
t <sub>PWE</sub>	WE Pulse Width	35		40		45		ns
t <sub>BW</sub>	BLE / BHE LOW to Write End	40		40		60		ns
t <sub>SD</sub>	Data Set-up to Write End	25		25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>HZWE</sub>	WE LOW to High-Z <sup>[17, 18]</sup>		15		20		25	ns
t <sub>LZWE</sub>	WE HIGH to Low-Z <sup>[17]</sup>	10		10		10		ns

**Notes:**

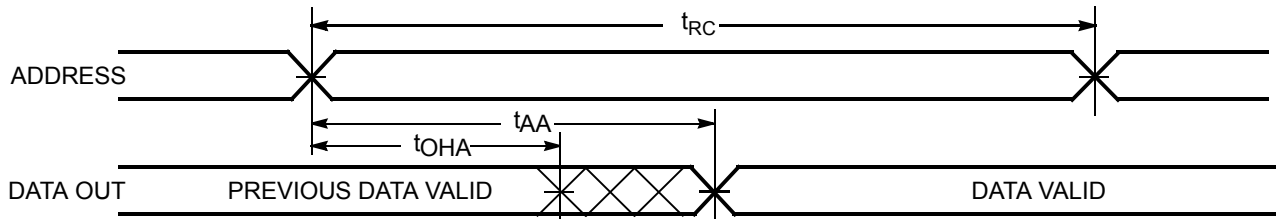
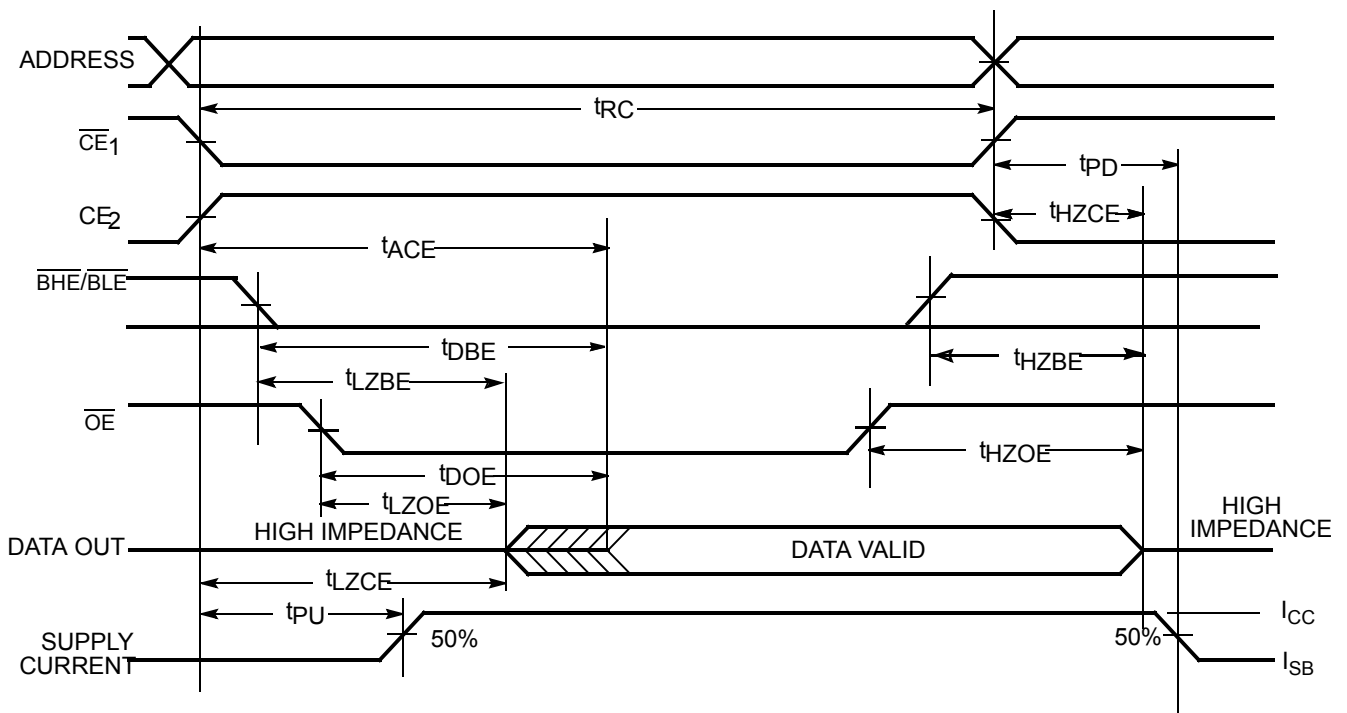
15. BHE, BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

16. Test conditions for all parameters other than three-state parameters assume signal transition time of 3 ns or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.

17. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.

18. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high-impedance state.

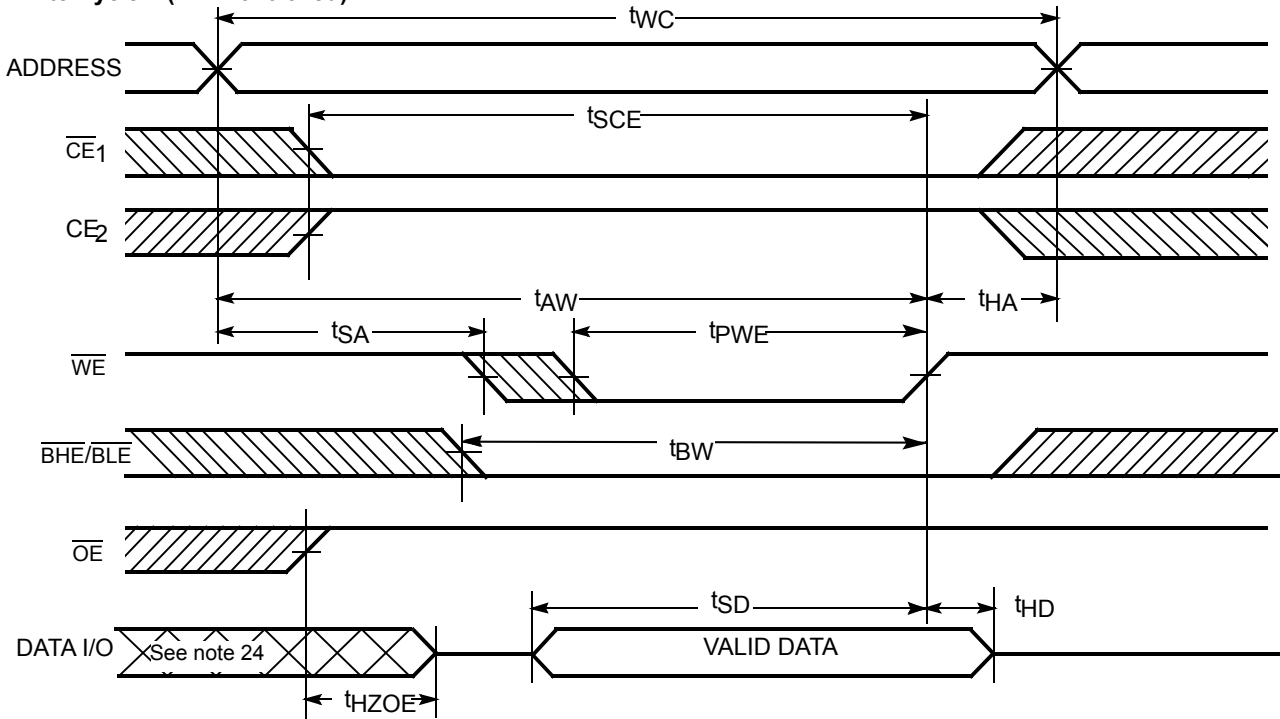
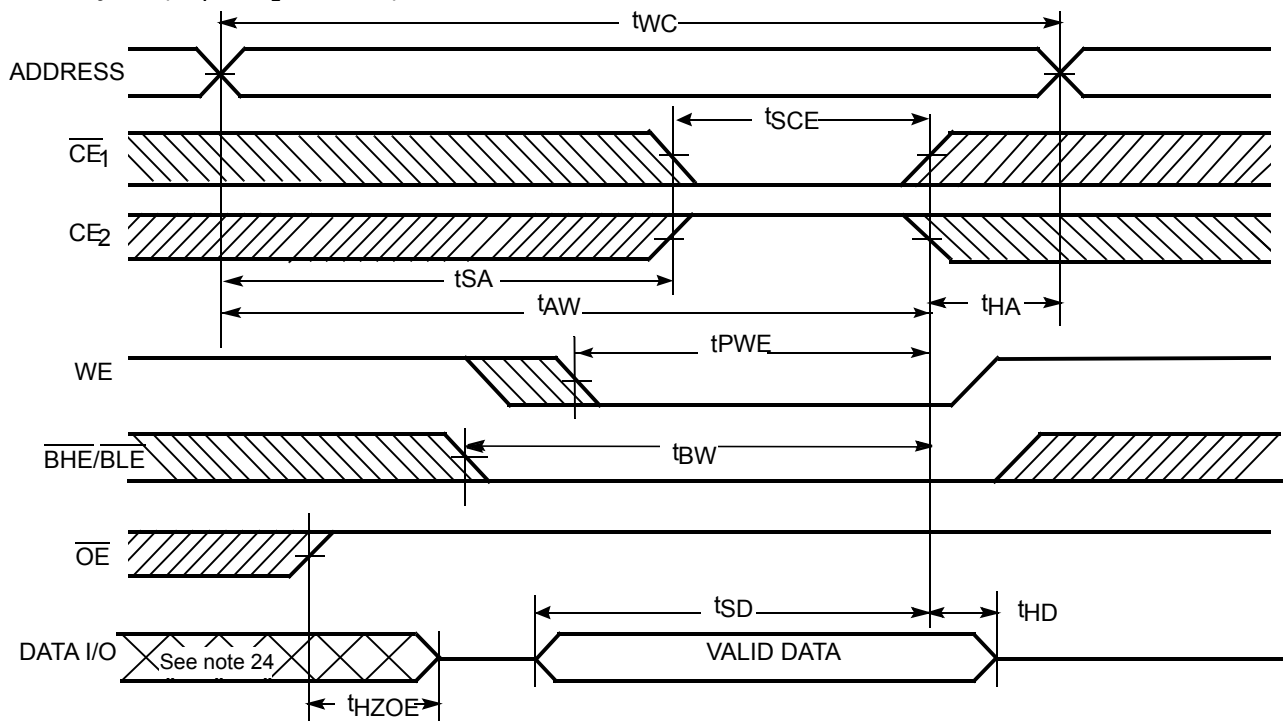
19. The internal Write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE and/or BLE = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

**Switching Waveforms**
**Read Cycle 1 (Address Transition Controlled)<sup>[20, 21]</sup>**

**Read Cycle 2 ( $\overline{OE}$  Controlled)<sup>[21, 22]</sup>**

**Notes:**

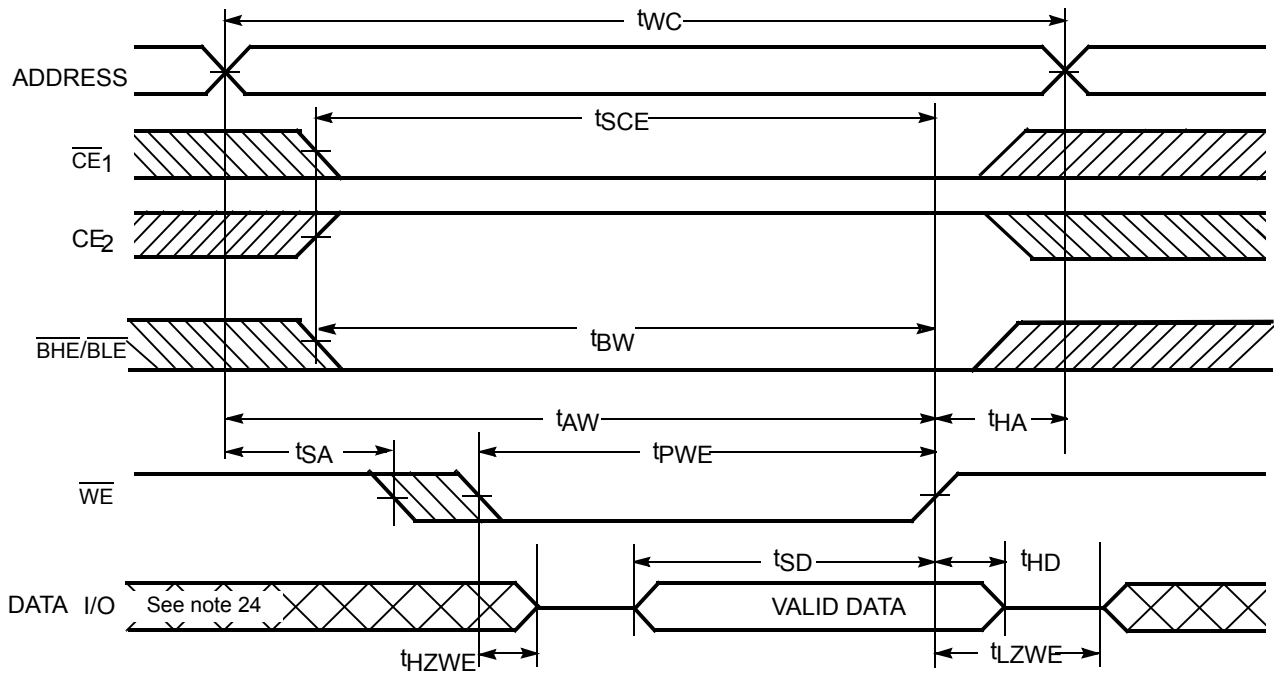
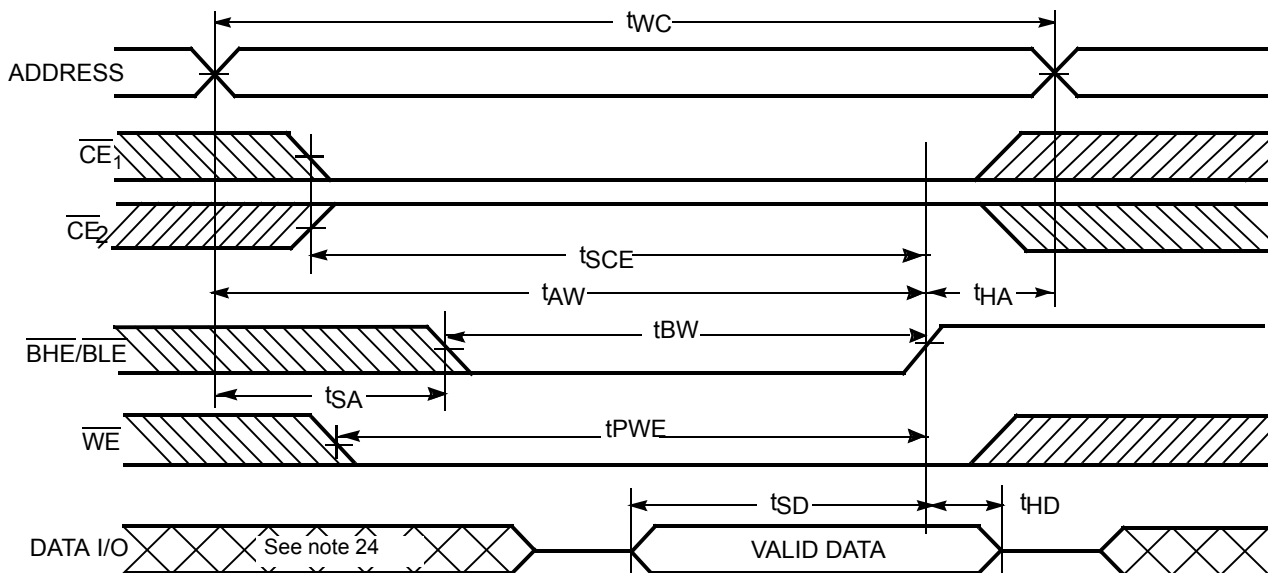
20. The device is continuously selected. OE,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ .

21.  $\overline{WE}$  is HIGH for read cycle.

22. Address valid prior to or coincident with  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms (continued)**
**Write Cycle 1 ( $\overline{WE}$  Controlled)** [19, 23, 24, 25]

**Write Cycle 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled)** [19, 23, 24, 25]

**Notes:**

23. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
24. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high-impedance state.
25. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[24, 25]</sup>**

**Write Cycle 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[24, 25]</sup>**




**Truth Table**

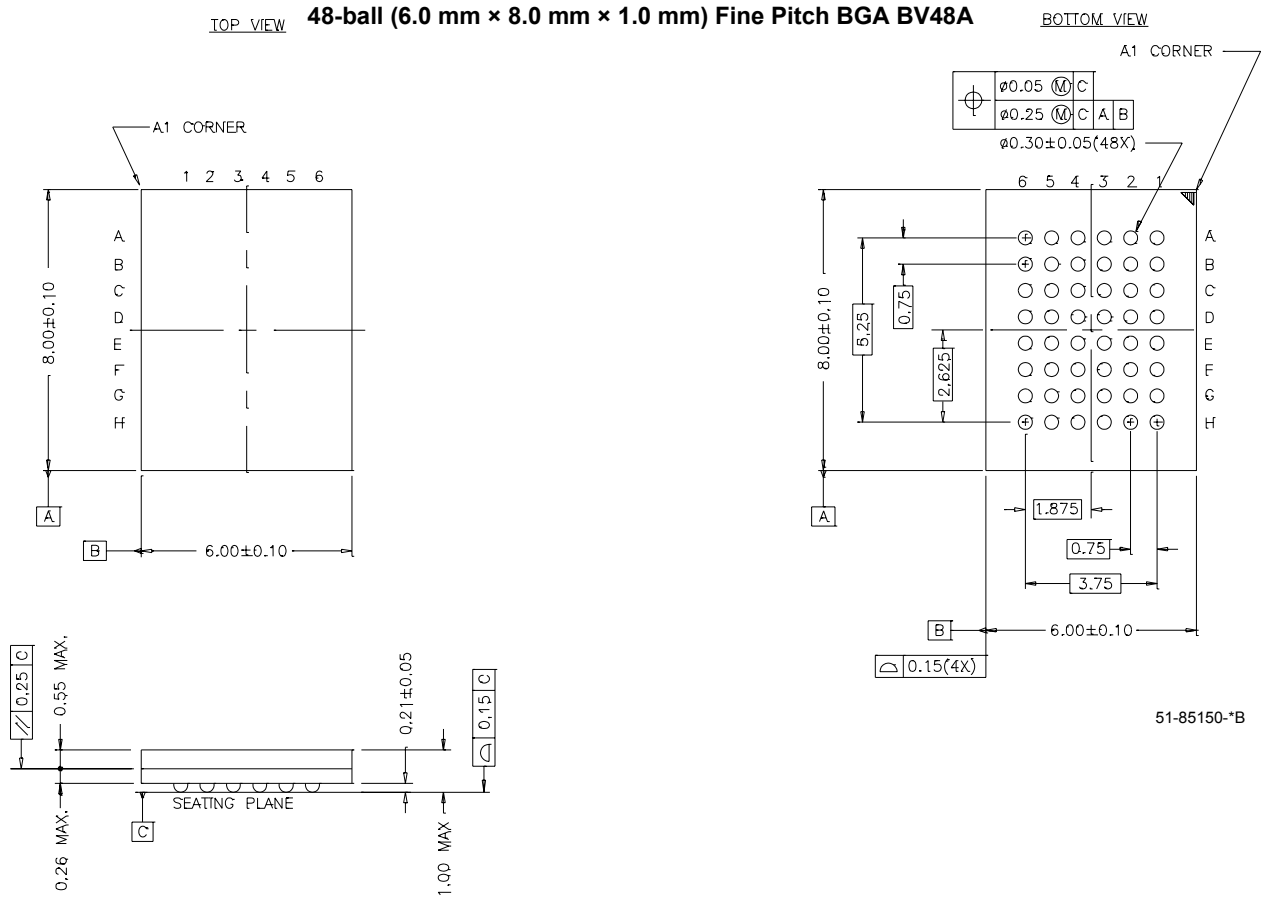
$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out (I/O0 – I/O15)	Read (Upper byte and Lower Byte)	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out (I/O0 – I/O7); High Z (I/O8 – I/O15)	Read (Lower Byte only)	Active ( $I_{CC}$ )
L	H	H	L	L	H	High Z (I/O0 – I/O7); Data Out (I/O8 – I/O15)	Read (Upper Byte only)	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In (I/O0 – I/O15)	Write(Upper byte and Lower Byte)	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In (I/O0 – I/O7); High Z (I/O8 – I/O15)	Write (Lower Byte only)	Active ( $I_{CC}$ )
L	H	L	X	L	H	High Z (I/O0 – I/O7); Data In (I/O8 – I/O15)	Write (Upper Byte only)	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY62157DV30L-45BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm)	Industrial
	CY62157DV30LL-45BVI			
45	CY62157DV30L-45ZXI	Z-48	48-pin TSOP I (Pb-free)	Industrial
	CY62157DV30LL-45ZXI			
45	CY62157DV30L-45ZSXI	ZS-44	44-pin TSOP II (Pb-free)	Industrial
	CY62157DV30LL-45ZSXI			
55	CY62157DV30L-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm)	Industrial
	CY62157DV30LL-55BVI			
55	CY62157DV30L-55BVXI	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm) (Pb-free)	Industrial
	CY62157DV30LL-55BVXI			
55	CY62157DV30L-55BVE	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm)	Automotive
55	CY62157DV30L-55ZXI	Z-48	48-pin TSOP I (Pb-free)	Industrial
	CY62157DV30LL-55ZXI			
55	CY62157DV30L-55ZXE	Z-48	48-pin TSOP I (Pb-free)	Automotive
55	CY62157DV30L-55ZSXI	ZS-44	44-pin TSOP II (Pb-free)	Industrial
	CY62157DV30LL-55ZSXI			
55	CY62157DV30L-55ZSXE	ZS-44	44-pin TSOP II (Pb-free)	Automotive
55	CY62157DV30L-55ZSI	ZS-44	44-pin TSOP II	Industrial
	CY62157DV30LL-55ZSI			
70	CY62157DV30L-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm)	Industrial
	CY62157DV30LL-70BVI			
70	CY62157DV30L-70BVXI	BV48A	48-ball Fine Pitch BGA (6 mm × 8 mm × 1 mm) (Pb-free)	Industrial
	CY62157DV30LL-70BVXI			
70	CY62157DV30L-70ZXI	Z-48	48-pin TSOP I (Pb-free)	Industrial
	CY62157DV30LL-70ZXI			

**Ordering Information** (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62157DV30L-70ZSXI	ZS-44	44-pin TSOP II (Pb-free)	Industrial
	CY62157DV30LL-70ZSXI			
70	CY62157DV30L-70ZSI	ZS-44	44-pin TSOP II	Industrial
	CY62157DV30LL-70ZSI			

**Package Diagrams**


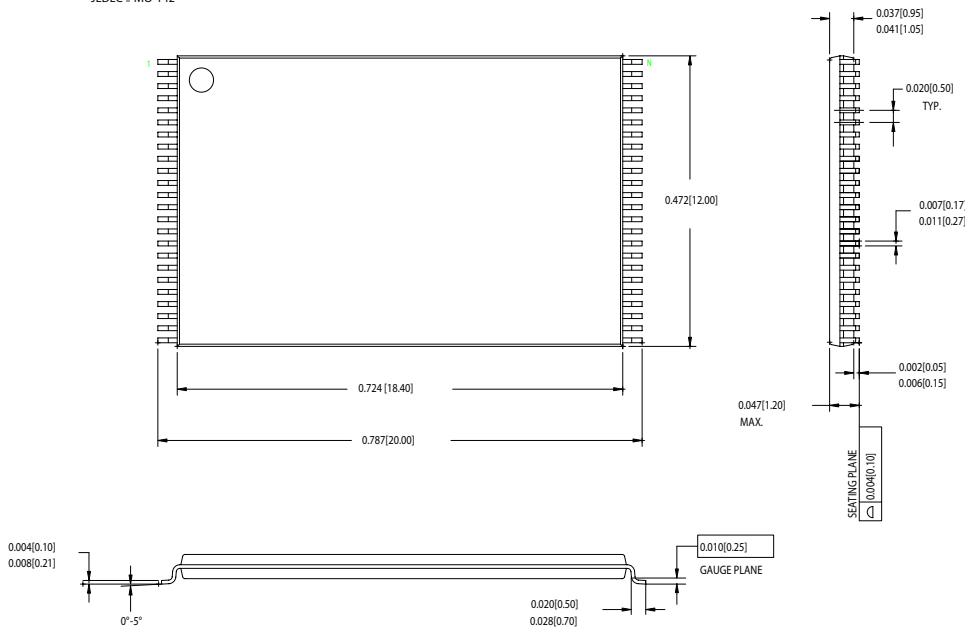
Package Diagrams (continued)

48-Lead TSOP I (12 mm x 18.4 mm x 1.0 mm) Z48A

DIMENSIONS IN INCHES (MM) MIN.

MAX.

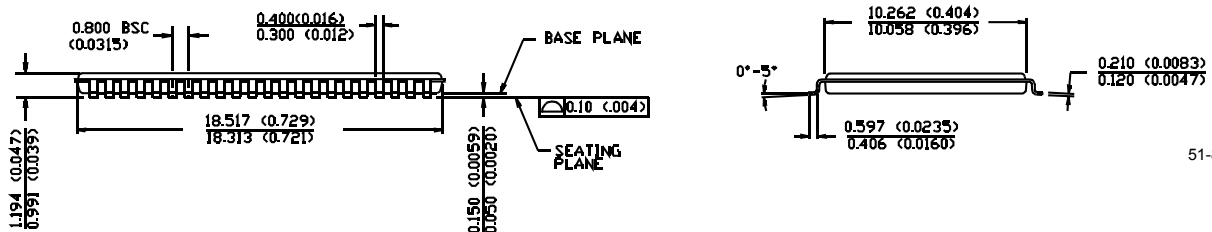
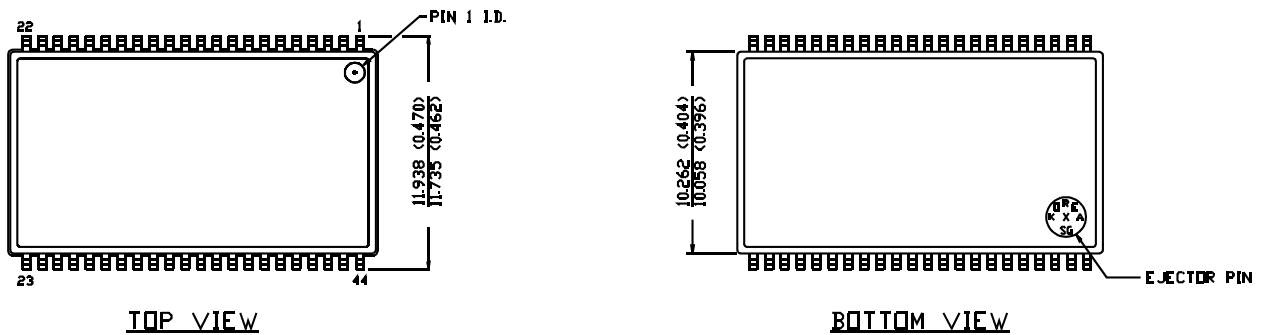
JEDEC # MO-142



51-85183-A

DIMENSION IN MM (INCH)  
MAX  
MIN

44-Pin TSOP II ZS44



51-85087-A

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Document History Page

Document Title:CY62157DV30 MoBL® 8-Mbit (512K x 16) MoBL® Static RAM Document Number: 38-05392				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	126316	05/22/03	HRT	New Data Sheet
*A	131013	11/19/03	CBD/LDZ	Change from Advance to Preliminary
*B	133115	01/24/04	CBD	Minor Change: Change MPN and upload.
*C	211601	See ECN	AJU	Change from Preliminary to Final Changed Marketing part number from CY62157DV to CY62157DV30 in the title and in the Ordering Information table Added footnotes 4, 5 and 11 Modified footnote 8 to include ramp time and wait time Removed MAX value for VDR on Data Retention Characteristics table Changed ordering code for Pb-free parts Modified voltage limits in Maximum Ratings section
*D	236628	See ECN	SYT/AJU	Added 45-ns and 70-ns Speed Bins Added Automotive product information
*E	257349	See ECN	PCI	Added test condition for 45 ns part (footnote #13 on page 4)