CLA60000 Series

Channel less CMOS Gate Arrays

This new family of gate arrays uses many innovative techniques to achieve 110K gates per chip with system clock speeds of up to 70MHz. The combination of high speed, high gate complexity and low power operation places Zarlink Semiconductor at the forefront of ASIC capability.

General Description

The CLA60000 gate array family is Zarlink Semiconductor's fifth-generation CMOS gate array product. These arrays allow even higher integration densities at enhanced system clock rates as need for many of today's system applications.

The largest array in the family at 110K gates offers a tenfold increase in raw gate availability then channelled gate arrays. In addition, many new designs features have been incorporated such as analog functionality, slew rate output control, and intermediate I/O buffering for optimum data transfer through peripheral cells.

Also, the low-power characteristics of Zarlink Semiconductor CMOS processing have been incorporated in these arrays, easing the thermal management problems associated with complex designs of 20,000 gates and above.

Features

- Channel less arrays to 110,000 gates
- 1.4 micron dual layer metal silicon CMOS process
- Typical Gate Delays of 700ps (NAND2)
- Comprehensive cell library including microcells, macrocells, and paracells
- Power distribution optimized for maximum noise immunity
- Slew controlled outputs with up to 24mA drivers
- Fully supported by design software (PDS2) and popular workstations
- Very high latch up immunity

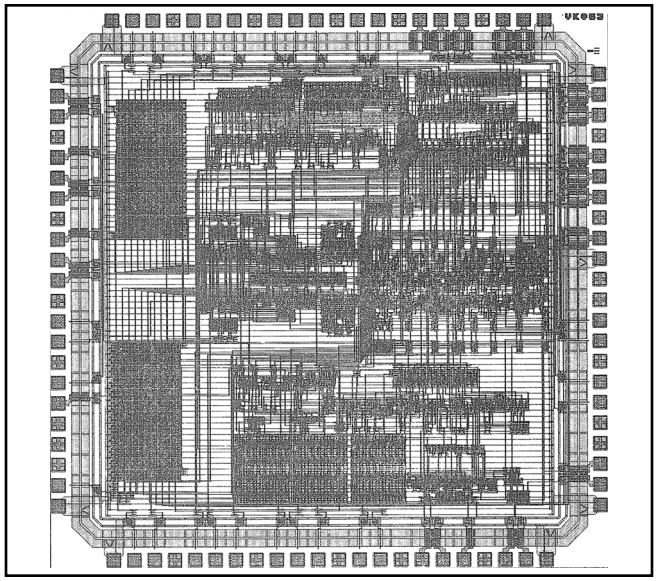


Figure 1 - CLA60000 Chip Microplot

All CLA60000 arrays have the same construction. A core of uncommitted transistors is arranged for optimum connection as logic functions and surrounded by uncommitted peripheral (I/O) circuitry. The channel less array architecture is an important feature - the absence of discrete wiring channels increases flexibility, reduces track capacitance whilst significantly increasing transistor sizes for improved logic performance.

The construction of the basic building blocks have been planned to support basic logic functions, macro functions, and core memory functions (RAM and ROM) with high routability. Logic programmability is given by dual level metal, with interconnecting vias, plus a forth level of programmability (contacts).

The overall architecture of these gate arrays has been designed to exploit many new and emerging developments in CAD tools. Increasing demands are now being made for design tools which are faster, easier to use, and more accurate. The Zarlink Semiconductor Design System (PDS2) allows full control over all aspects of design including logic capture, simulation and layout.

Product Range

The CLA60000 product range is shown below. Actual gate utilization can be typically 40-70% of the uncommitted gate count depending on circuit structure.

Product	Uncommitted Gate Count	Pads Including Power
CLA61XXX	2040	40
CLA62XXX	5488	64
CLA63XXX	10608	88
CLA64XXX	19928	120
CLA65XXX	35784	160
CLA66XXX	55616	200
CLA67XXX	80560	240
CLA68XXX	110112	280

Core Arrangement

A four transistor (2 NMOS and 2 PMOS) groups forms the basis of the core array. This array element is repeated in a regular fashion over the complete core area to give a 'Full Field' (sea-of-gates) array. The unique design of the basic four transistor cells give the Zarlink Semiconductor arrays a major advantage over all competitors. Thesilicon layout has been configured so that the basic logic cells, flip-flops and large hierarchical cells can be interconnected easily with through-cell routing channels. It also ensures that an optimum overall data flow and control signal distribution scheme is possible.

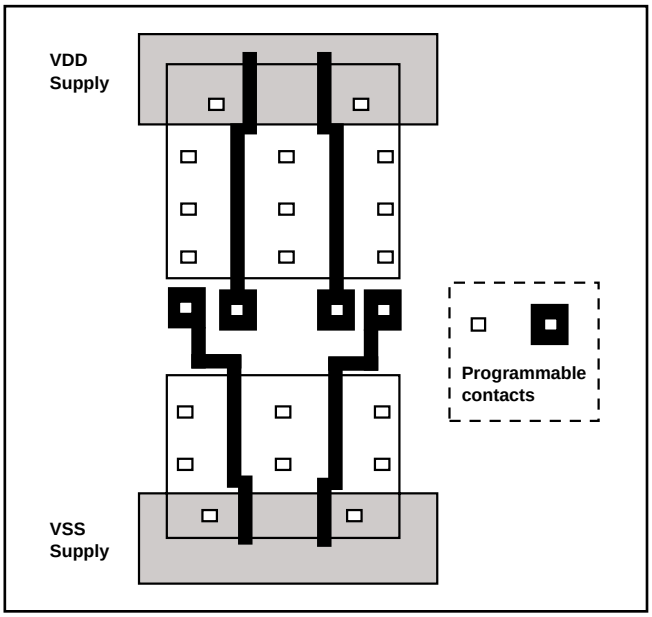


Figure 2 - Array Core Cell

Complete rows of array elements can be used as routing channels to conform to the earlier channeled Zarlink Semiconductor arrays or, if desired, compact hierarchical logic blocks and localized routing areas can be defined like a cell based design layout. The array structure has been designed to be totally flexible in architecture with the distribution of logic blocks and routing channels being definable by the designer.

I/O Buffer Arrangement

The I/O buffers are the interface to external circuitry and are therefore required to be robust and flexible. The inputs and outputs can withstand electro-static discharges, are not susceptible to latch up (an inherent CMOS problem) and provide the designer with multiple interface options.

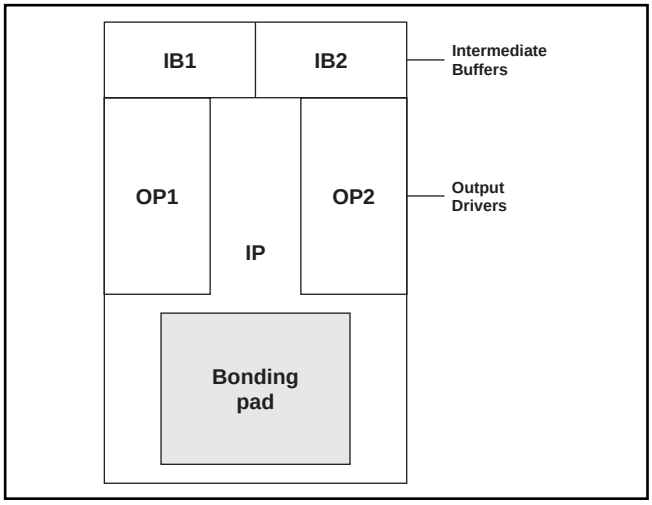
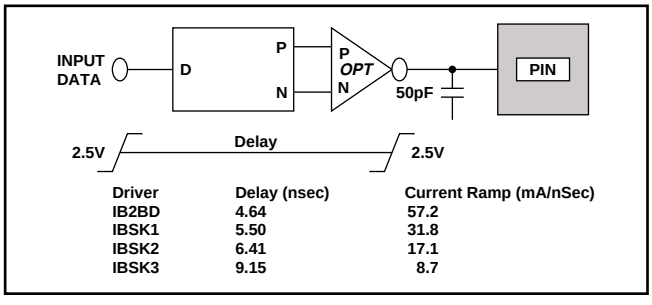


Figure 3 - I/O Block

The CLA60000 I/O buffers contain all the components for static protection, input pull-up and pull down resistors, various output drive currents and input interface signals such as CMOS and TTL. In addition, the I/O buffer contains all the components for intermediate buffering stages including Schmitt triggers, TTL threshold detectors, tristate control, signal re-timing flip-flops and slew rate control for the output drivers. Some analog interface cells can also be implemented using the available components. I/O buffer locations can also be configured as supply pads (VDD and VSS).



Driver	Delay (nsec)	Current Ramp (mA/nSec)
IB2BD	4.64	57.2
IBSK1	5.50	31.8
IBSK2	6.41	17.1
IBSK3	9.15	8.7

Figure 4 - Slew Control

Slew control of output drivers is a useful benefit where outputs are driving large capacitive loads such as busses. Noise transients caused by voltage coupling into peripheral power supplies can give switching problems, resulting in mis-operation. The extent of this voltage disruption is depended on the number of outputs switching, supply pad locations and the inductance of the chip bond wire/package leads. The CLA60000 family uses proprietary design techniques to reduce this phenomenon by offering output switching control (di/dt) as part of the intermediate buffers.

The power distribution scheme for the CLA60000 arrays is very flexible (shown in figure 5): three separate power rings are used, one for the internal core logic, one for the large output driver cells and one for the intermediate buffer regions. Each of the separate power rings isolate any noise generated by the low-impedance output drivers from the core logic and intermediate buffers. The power rings can be connect to separate pad locations or, if required, combined at a single Input or Output pad location. In addition, it is possible to isolate sections of the peripheral supply ring for the implementation of basic analog circuits.

The distribution of the supply rails across the core of the array can be automatically positioned for the interconnect of the base cells and hierarchical blocks. This allows greater design flexibility and provides additional signal routing channels. Supply interconnection is added during autolaying leaving unpopulated areas available for signal routing.

Low core power dissipation is very important for high complexity circuits (see section on Thermal Management).

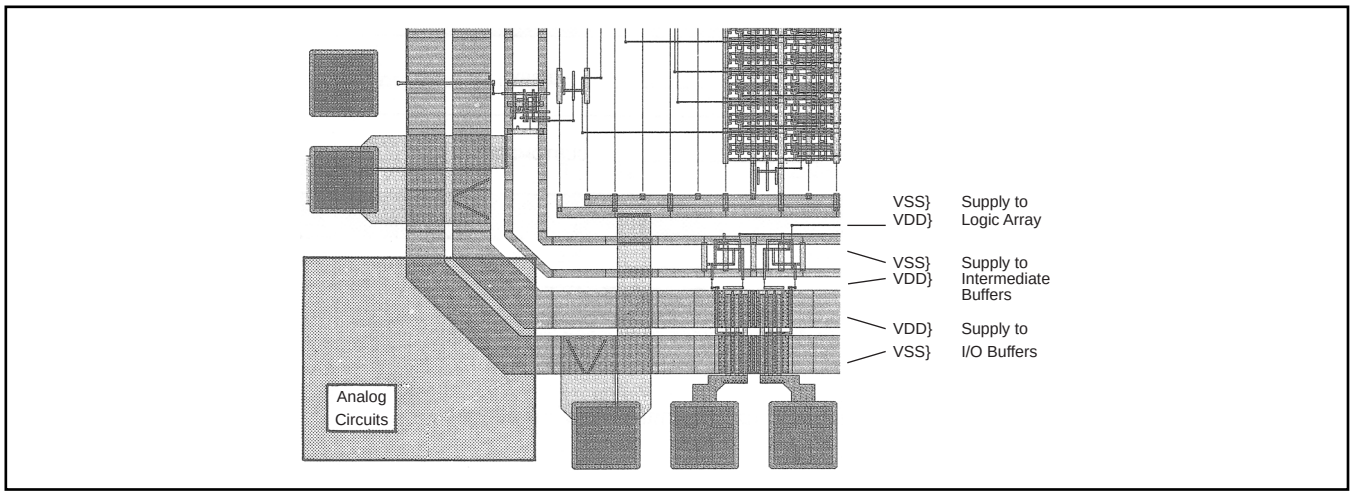


Figure 5 - Power Supply Organization

PDS2 - The Zarlink Semiconductor ASIC Design System

PDS2 is Zarlink Semiconductor's ASIC computer-aided design system. It provides a fully integrated, technology independent VLSI design system for all Zarlink Semiconductor Semi-Custom CMOS products.

PDS2 allows the designer to perform all design activities from schematic entry, circuit debugging, fault grading, through to chip layout and generation of a test program for the production test of the finished ICs.

Logical design of CLA60000 is realized with the same software as is used for the CLA5000 and MVA5000 families of CMOS semi-custom products. PDS2 runs on DEC VEX equipment (under VMS)* and comprise schematic entry, logic and fault simulation, extensive result examination facilities and advanced library and configuration management tools. Layout and routing is also supported on PDS2 along with full back annotation. Hierarchical logical design is possible up to 20 levels.

Supplemented by a three day training course for first-time users, PDS2 may be used either at a Zarlink Semiconductor Design Centre or under licence at the designer's premises.

Design Support and Interfaces

Zarlink Semiconductor offers a variety of design interfaces to customers. For each interface, Zarlink Semiconductor requires a given set of information to be forwarded by the designer which is assessed at Design Reviews (1 to 4). At each stage, the design must be deemed to be acceptable by Zarlink Semiconductor Project Engineers before commencing the next stage of work. Design Reviews may be held in the designer's premises or at a Zarlink Semiconductor Design Centre.

Further information on PDS2 or the interfacing requirements to the Zarlink Semiconductor technologies is available from any Zarlink Semiconductor Sales Office or Design Centre.

* DEC, VAX and VMS are trademarks of Digital Equipment Corporation, USA

Design Interfaces

	PDS2 USED AT Zarlink DESIGN CENTRE		PDS2 USED BY CUSTOMER ON OWN PREMISES			Zarlink COMPLETES DESIGN	
						TURN KEY	WORK STATION
OPTIONS	A	B	C	D	E	F	G
DESIGN REVIEW 1							
LOGICAL DESIGN	CUSTOMER	CUSTOMER	CUSTOMER	CUSTOMER	CUSTOMER	Zarlink	Zarlink
DESIGN REVIEW 2							
PHYSICAL DESIGN	Zarlink	CUSTOMER	Zarlink	CUSTOMER	CUSTOMER (AT DESIGN CENTRE)	Zarlink	Zarlink
DESIGN REVIEW 3							
PROTOTYPE MANUFACTURING				Zarlink			
PROTOTYPE EVALUATION				CUSTOMER			
DESIGN REVIEW 4							
PRODUCTION				Zarlink			

Figure 6 - Access Routes to Zarlink Semi-custom

Zarlink Semiconductor operates a design audit procedure with four formal review meetings:

REVIEW 1:	Checks that the required specification can be met by the CLA60000 gate array.
LOGICAL DESIGN:	Conversion of the logic into hierarchical netlist. Circuit function is simulated for the eventual environmental conditions to be met by the chip, including definition of the test pattern and fault simulation.
REVIEW 2:	Checks that logic simulation results are acceptable to both parties, and finalizes objectives for physical design (package, pinout, etc.)
PHYSICAL DESIGN:	Package and pinout are defined. Cells are placed and routed within the array - using Zarlink Semiconductor's interactive layout package. A final simulation is performed which takes account of real track loads.
REVIEW 3:	Establishes that it is appropriate to proceed with chip manufacture by comparing all PDS2 results with customer's specifications.
PROTOTYPES:	Zarlink Semiconductor manufactures four custom masks develops a test program from the customer' simulation vectors, fabricates wafers and supplies 10 tested, packaged prototypes as standard. Additional prototypes may be supplied at extra cost.
REVIEW 4:	Confirms that the customer has fully examined the prototype and approves the chip design for full-scale production.

The schematic entry and logical design work may be done by Zarlink Semiconductor, or the customer may licence the PDS2 tools with Zarlink Semiconductor providing training to enable the engineer to undertake this phase of development in house. Design rooms and equipment are also available for customer use at any Zarlink Semiconductor design centres at attractive rental rates.

For the physical design phase, customers are encouraged to work with Zarlink Semiconductor layout engineers to ensure the best possible final performance. This can be completed either at a Zarlink Semiconductor design centre or at the customers premises.

Design Thermal Management

As gate integration capacity improves with CMOS process geometry reduction, the ability of silicon to exceed the power capabilities of accepted packaging technology is a very real problem. Semi-Custom designers now have the ability to design circuits of 50,000 gates and over, and chip power consumption is (or should be) a very important concern.

With complexities approaching 100K gates, the core power at gate level becomes increasingly more dominant. It becomes essential to offer ultra low power core logic to maintain an acceptable overall chip power budget (typically 1 Watt for standard surface mount packaging).

The consequences of higher power consumption are elevated chip temperatures and reductions in product reliability, otherwise relatively expensive special packaging has to be considered which is bulkier and more costly.

Zarlink Semiconductor's CLA60000 arrays offer low power factors. At 5mW per gate per MHz gate power and 2mW per gate load, power is lower than most competitive arrays, with lower operating temperatures and higher inherent long term reliability.

CLA60000 Power Dissipation Calculation

CLA60000 series power dissipation for any array can be estimated by following this example (calculated for the CLA68XXX).

Number of available gates	110112
Percent gates used	40%
Number of used gates	44045
Number of gates switching each clock cycle (15%)	6607
Power dissipation/gate/MHz (µW) (gate fanout typically 2 loads)	9
Total core dissipation/MHz (mW)	59.5
Number of available I/O pads	280
Percent of I/O pads used as Outputs	40
Number of I/O pads used as Outputs	112
Number of output buffers switching each clock cycle (20%)	22
Dissipation/output buffers/MHz/pF (µW)	25
Output loading in pF	50
Power/output buffer/MHz (mW)	1.25
Total output buffer dissipation/MHz (mW)	27.5
Total Power dissipation/MHz (mW)	87
Total Power at 10MHz clock rate (W)	0.87
Total Power at 25MHz clock rate (W)	2.18

1.4 Micron CMOS Process

The 1.4 micron CMOS process Zarlink Semiconductor process variant VJ) uses the latest manufacturing techniques at Zarlink Semiconductor's Class 1, 6-inch fabrication facility in Roborough, England. The process can be described as a twin well, self aligned LOCOS isolated technology on an epitaxial substrate giving low defect density and high reliability.

Effective channel length is 1.1 micron. Usable gate packaging density is 600 gates/sq.mm on two levels of metal. Devices will operate up to a maximum junction temperature of 170 Deg.C, and show excellent hardness, ESD, and stable performance.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		MIN	MAX	UNITS
Supply	Voltage	-0.5	7.0	V
Input	Voltage	-0.5	Vdd+0.5	V
Output	Voltage	-0.5	Vdd+0.5	V
Storage	Temperature:			
	Ceramic	-65	150	Deg.C
	Plastic	-40	125	Deg.C

Operation above these absolute maximum ratings may permanently damage device characteristics and may affect reliability.

RECOMMENDED OPERATING LIMITS

PARAMETER	MIN	MAX	UNITS
Supply Voltage	3.0	6.0	V
Input Voltage	Vss	Vdd	V
Output Voltage	Vss	Vdd	V
Current per pad		100	mA
Operating Temperature:			
Commercial Grade	0	70	Deg.C
Industrial Grade	-40	85	Deg.C
Military Grade	-55	125	Deg.C

AC Characteristics for Selected Cells

The CLA60000 technology library contains all the timing information for each cell in the design library. This information is accessible to the simulator, which calculates propagation delays for all signal paths in the circuit design. The PDS2 simulator can automatically derate timings according to the various factors such as:

Supply voltage variation (from nominal 5V)
Chip temperature
Processing tolerance
Gate fanout
Input transition time
Input signal polarity
Interconnecting wiring

For initial assessments of feasibility, worst case estimations of path delays can be done in the following manner, using the dynamic Characteristics table as a guide to the normal propagation delays at 25 Deg. C and 5V supply.

- For temperatures, Zarlink Semiconductor's has derived a derating multipler (Kt) of +0.3% per Deg. C
- For supply voltage derating, a factor of (Kv) - 25% per volt of VDD Change should be used.
- For manufacturing variation (Kp), the tolerance is ±50%
- The maximum variation on typical delays over the Commercial grade product will be at 4.5V and 70 Deg. C ambient temperature.

tpd (max)

= Kp x Kv x Kt x tpd (typ)

= 1.50 x (1+(5.0 - 4.5) 0.25) x (1+(70-25) 0.003) x tpd (typ)

= 1.50 x 1.13 x 1.13 x tpd (typ) = 1.91 x tpd (typ)

The minimum delay, at 5.5V and 0 Deg. C will be:

tpd (min)

= 0.66 x (1-(5.5-5.0) x 0.25) x (1-(25-0)0.003) x tpd (typ)

= 0.66 x 0.87 x 0.93 x tpd (typ)

= 0.53 x tpd (typ)

A similar calculation may be applied for any voltage and temperature relevant to the application. An additional "safety factor" of ±20% may be applied if desired for conservative design. For worst case military grade characteristics, the performance derating multiplier is 2.57 times the commercial typical.

Fanout is in gate load units

INTERNAL CORE CELLS

Name	Cells	Description	Symbol	Typical Propagation Delay (nS) Fanout=2	Worst case Propagation Delay (nS) Commercial Fanout 2	Commercial Fanout 4	Industrial Fanout 2	Industrial Fanout 4
INV2	1	INVERTER DUAL DRIVE	tpLH tpHL	0.64 0.39	1.43 0.87	1.65 1.05	1.50 0.91	1.72 1.10
NAND2	2	2 - INPUT NAND GATE	tpLH tpHL	0.82 0.67	1.83 1.51	2.27 2.01	1.92 1.58	2.38 2.11
NOR 2	2	2 - INPUT NOR GATE	tpLH tpHL	1.11 0.58	2.48 1.30	3.24 1.66	2.60 1.36	3.40 1.74
DF	4	MASTER SLAVE	tpLH tpHL	1.04 0.93	2.32 2.08	2.76 2.44	2.44 2.18	2.90 2.56
DFRS	6	MASTER SLAVE D - TYPE WITH SET AND RESET	tpLH tpHL	1.19 1.12	2.66 2.52	3.10 3.02	2.79 2.65	3.25 3.17

INTERMEDIATE BUFFER CELLS

Name	Cells	Description	Symbol	Typical Propagation Delay (nS) Fanout=2	Worst case Propagation Delay (nS) Commercial Fanout 2	Commercial Fanout 4	Industrial Fanout 2	Industrial Fanout 4
IBGATE	-	LARGE 2 INPUT NAND GATE + 2 INPUT NOR	tpLH tpHL	0.76 0.50	1.69 1.13	2.05 1.40	1.77 1.19	2.15 1.47
IBDF	-	MASTER SLAVE D-TYPE FLIP FLOP	tpLH tpHL	1.04 0.93	2.32 2.08	2.76 2.44	2.44 2.18	2.90 2.56
IBCMOS1	-	CMOS INPUT BUFFER WITH 2 INPUT NAND GATE	tpLH tpHL	1.11 0.72	2.48 1.61	2.88 1.83	2.60 1.69	3.02 1.92

INTERMEDIATE BUFFER CELLS				Typical Propagation Delay (nS)	Worst case Propagation Delay (nS)			
					Commercial		Industrial	
Name	Cells	Description	Symbol	Fanout=2	Fanout		Fanout	
					2	4	2	4
OP 3	-	STANDARD OUTPUT BUFFER	tpLH tpHL	2.83 2.06	2.83 2.06	10.03 5.66	2.79 2.16	10.53 2.27
OP 6	-	MEDIUM OUTPUT BUFFER	tpLH tpHL	0.86 0.70	1.93 1.52	5.53 3.12	2.02 1.59	5.80 3.28
OP 12	-	LARGE OUTPUT BUFFER	tpLH tpHL	0.70 0.56	1.52 1.23	3.12 2.03	1.60 1.29	3.28 2.13

Note:
Commercial Worst case is 4.5V, 70 Deg.C operating, Worst Case processing
Industrial Worst case is 4.5V, 85 Deg.C operating, Worst Case processing
Military worst case is 4.5V, 125 Deg.C operating, Worst Case processing

DC Electrical Characteristics

All characteristics at Commercial Grade voltage and temperature (Note 1)

CHARACTERISTIC	SYM	VALUE			UNIT	CONDITIONS
		Min	Typ	Max		
LOW LEVEL INPUT VOLTAGE	VIL				V	
TLL Inputs (IBTTL1/IBTTL2)				0.8		
CMOS Inputs (IBCMOS1/IBCMOS2)				1.0		
HIGH LEVEL INPUT VOLTAGE	VIH				V	
TLL Inputs (IBTTL1/IBTTL2)		2.0				
CMOS inputs (IBCMOS1/IBCMOS2)		VDD - 1.0				
INPUT HYSTERESIS (IBST1) Rising	VT+		2.75		V	VIL to VIH
Falling	VT-		1.92			VIH to VIL
(IBST2) Rising	VT+		2.20			VIL to VIH
Falling						VIH to VIL
INPUT CURRENT CMOS/TTL INPUTS	IIN	-5		+5	µA	VIN = VDD or VSS
Inputs with 1Kohm Resistors		±0.2	±5	±10	mA	VIN = VDD or VSS
Inputs with 2Kohm Resistors		±0.1	±2.5	±5	mA	VIN = VDD or VSS
Inputs with 4Kohm Resistors		±0.05	±1.2	±2.5	mA	VIN = VDD or VSS
Inputs with 100Kohm Resistors		±10	±50	±200	mA	VIN = VDD or VSS
Resistor values nominal - See note 2						
HIGH LEVEL OUTPUT VOLTAGE	VOH				V	
All outputs		VDD -0.05				IOH=-1µA
Smallest drive cell OP1/OPOS1		VDD-1.0	VDD-0.5			IOH=-1mA
Low drive cell OP2/OPOS2		VDD-1.0	VDD-0.5			IOH=-2mA
Standard drive cell OP3/OPOS3		VDD-1.0	VDD-0.5			IOH=-3mA
Medium drive cell OP6/OPOS6		VDD-1.0	VDD-0.5			IOH=-6mA
Large drive cell OP12/OPOS12		VDD-1.0	VDD-0.5			IOH=-12mA
LOW LEVEL OUTPUT VOLTAGE	VOL				V	
All Outputs				VSS +0.05		IOL=1µA
Smallest Drive Cell OP1/OPOD1			0.2	0.4		IOL=2mA

DC Electrical Characteristics (continued)

All characteristics at Commercial Grade voltage and temperature (Note 1)

CHARACTERISTIC	SYM	VALUE			UNIT	CONDITIONS
		Min	Typ	Max		
Low drive cell OP2/OPOS2			0.2	0.4		IOL=4mA
Standard drive cell OP3/OPOS3			0.2	0.4		IOL=6mA
Medium drive cell OP6/OPOS6			0.2	0.4		IOL=12mA
Large drive cell OP12/OPOS12			0.2	0.4		IOL=24mA
TRISTATE OUTPUT LEAKAGE CURRENT	IOZ				µA	
OUTPUT SHORT CIRCUIT CURRENT	IOS				mA	
STANDBY SUPPLY CURRENT (per gate)	IDDSB		10		nA	

Note 1: Commercial grade is 0-70 deg. C, 5V ±10% power supply voltage

Note 2: Resistor value spreads (Min-Max):

LOW VALUE (Rtyp 1K) 0.5 - 2Kohm LOW VALUE (Rtyp 4K) 2K - 8Kohm

LOW VALUE (Rtyp 2K) 1.0 - 4Kohm HIGH VALUE (Rtyp 100K) 25K - 250Kohm

Note 3: Standard driver output OP3 etc. Short circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.

Note 4: Excluding peripheral buffers.

Note 5: Excludes package leadframe capacitance or bidirectional pins.

Note 6: Excludes package.

Packaging

Production quantities of the CLA60000 family are available in Industry-standard ceramic and plastic packages according to the codes shown below. Prototype samples are normally supplied in ceramic only. Where plastic production packages are requested, Ceramic prototypes will be supplied in the nearest equivalent and tested to the final test specification.

DC	DILMON	Dual in Line, Multilayer ceramic. Brazed leads. Metal sealed lid. Through board.
DG	CERDIP	Dual in Line, Ceramic body. Alloy leadframe. Glass sealed. Through board.
DP	PLASDI	Dual in Line, Copper or Alloy leadframe. Plastic moulded. Through board.
AC	P.G.A.	Pin Grid Array. Multilayer Ceramic. Metal sealed lid. Through board.
MP	SMALL OUTLINE	Dual in Line 'Gullwing' formed leads. Plastic moulded. Surface mount.
LC	LCC	Leadless Chip Carrier. Multilayer ceramic. Metal sealed lid. Surface mount.
HC	LEADED CHIP CARRIER	Quad Multilayer ceramic. Brazed 'J' formed leads. Metal sealed lid. Surface mount.
GC	LEADED CHIP CARRIER	Quad Multilayer ceramic. Brazed 'Gullwing' leads. Metal sealed lid. Surface mount.
HG	QUAD CERPAC	Quad ceramic body. 'J' formed leads. Glass sealed. Surface mount.
GG	QUAD CERPAC	Quad ceramic body. 'Gullwing' formed leads. Glass sealed. Surface mount.
HP	PLCC	Quad Leaded plastic Chip Carrier. 'J' formed leads. Plastic moulded. Surface mount.
GP	PQFP	Quad plastic Flat Pack. 'Gullwing' formed leads. Glass sealed. Surface mount.

Packaging Options

The package style and pin count information is intended only as a guide. Detailed package specifications are available from Zarlink Semiconductor Design Centres on request. Available packages are being continuously updated, so if a particular package is not listed, please enquire through your Zarlink Semiconductor Sales Representative.

	LEADS	STYLE	CLA61	CLA62	CLA63	CLA64	CLA65	CLA66	CLA67	CLA68
DUAL IN LINE	16	DC	X							
	16	DG	X							
	16	DP	X							
	18	DC	X							
	18	DG								
	18	DP	X							
	20	DC	X							
	20	DG	X							
	20	DP	X							
	22	DC	X	X	X					
	22	DG		X						
	22	DP	X	X						
	24	DC	X	X	X	X				
	24	DG	X	X	X					
	24	DP	X	X	X					
	28	DC	X	X	X	X				
	28	DG	X	X	X	X				
	28	DP	X	X	X					
	40	DC	X	X	X	X	X			
	40	DG		X	X					
	40	DP	X	X	X	X				
	48	DC		X	X	X	X			
	48	DG								
	48	DP		X	X	X				
QUAD	16	MP	X							
	18	MP	X	X	X					
	20	MP	X							
	24	MP	X							
	28	MP	X	X						
	28	HP	X	X	X	X				
	28	LC	X	X	X					
	28	HC	X	X	X					
	28	HG	X	X	X					
	44	HP	X	X	X	X	X			
	44	GP	X	X	X					
	44	LC	X	X	X	X				
	44	HC	X	X	X	X				
	44	HG	X	X	X	X				
	48	GP		X	X	X				
	64	GP		X	X	X				
	68	HP		X	X	X	X			
	68	LC		X	X	X	X	X	X	
	68	HC		X	X	X	X			
	68	HG		X	X	X	X			
	80	GP			X	X				
	84	HP			X	X	X			
	84	LC			X	X	X	X		
	84	HC			X	X	X	X		
	84	HG		X	X	X	X	X		
	100	GP			X	X				
	100	GG			X	X				
	120	GP				X	X			X
	132	GC					X	X	X	
	160	GP								X
	172	GC						X	X	X
	196	GC						X		
PGA	68	AC		X	X	X	X			
	84	AC			X	X	X	X	X	
	100	AC			X	X	X			
	120	AC				X	X			
	132	AC					X	X		
	144	AC					X	X		
	180	AC					X	X		

Cell Library

A most comprehensive cell library is available in CLA60000. The implementation of a cell has involved the silicon planning, design rule checking, automatic generation of a SPICE file for performance analysis, SPICE simulation and result extraction, generation of data sheets, generation of the PDS2 simulator library code and verification of cell attributes for layout tools.

The two micron CMOS array (CLA5000) cell library can be converted to equivalent cells on the CLA60000 arrays to allow system upgrades. In addition, many new functions have been made available such as RAMs, ROMs, and DSP Macros. Some macro cells are also available for implementing structured test philosophies. Also separate documentation on build-in test for gate arrays will be available in the near future.

CLA60000 Library (Library version V1R2)

Logic Array:

BUF	Non-inverting Signal Buffer
2INV	Dual Inverter
INV2	Inverter Dual Drive
INV4	Inverter Quad Drive
INV8	Inverter x 8 Drive
NAND2	2-Input Nand Gate
ND3	3-Input Nand Gate
NAND3	3-Input Nand Gate + Inverter
2NAND	3 Dual 3-Input NAND Gate
NAND4	4-Input NAND Gate
NAND5	5-Input NAND Gate
NAND6	6-Input NAND Gate
NAND8	8-Input NAND Gate
NOR2	2-Input NOR Gate
NR3	3-Input NOR Gate
NOR3	3-Input NOR Gate + Inverter
2NOR3	Dual 3-Input NOR Gate
NOR4	4-Input NOR Gate
NOR5	5-Input NOR Gate
NOR 6	6-Input NOR Gate
NOR8	8-Input NOR Gate
A202I	2-Input AND to 2-Input NOR Gate + Inverter
O2A2I	2-Input OR to 2-input NAND Gate + Inverter
2A2O2	Dual 2-Input AND to 2-Input NOR Gate
202A2I	Dual 2-INput OR to 2-Input NAND Gate
2ANOR	2-Input ANDs to 2-Input NOR Gate
2ONAND	2-Input ORs to 2-Input NAND Gate
A2O3I	2-Input AND to 3-Input NOR Gate
O2A3I	2-Input OR to 3-Input NAND Gate
A3O2I	3-Input AND to 2-Input NOR Gate
O3A2I	3-Input OR to 2-Input NAND Gate
A2O4I	Quad 2-Input ANDs to 4-Input NOR Gate
O2A4I	Quad 2-Input ORs to 4-Input NAND Gate
A4O2I	Dual 4-Input ANDs to 2-INPUT NOR Gate
O4A2I	Dual 4-Input ORs to 2-Input NAND Gate
3A2O3I	Triple 2-input ANDs to 3-Input NOR Gate
302A3I	Triple 2-Input ORs to 3-Input NAND Gate
A202A2I	2-Input AND to 2-Input OR to 2-Input NAND
O2A2O2I	2-Input OR to 2-Input AND to 2-Input NOR
GND	GND Cell
VDD	VDD Cell
EXOR	Exclusive OR Gate + NAND Gate + Inverter
EXNOR	Exclusive NOR Gate + NOR Gate + Inverter
EXOR2	2-Input Exclusive OR Gate
EXNOR2	2-Input Exclusive NOR Gate
EXOR 3	3-Input Exclusive OR Gate
EXNOR3	3-Input Exclusive NOR Gate
HADD	Half Adder + Inverter
SUM	Sum Block
CARRY	Carry Block + NOR Gate
FADD	Full Adder + NOR Gate
MUX2TO1	2 to 1 Multiplexor
MUX4TO1	4 to 1 Multiplexor
MUX8TO1	8 to 1 Multiplexor
MUXI2TO1	2 to 1 Inverting Multiplexor
MUXI4TO1	4 to 1 Inverting Multiplexor
MUXI8TO1	8 to 1 Inverting Multiplexor

CLKA	Basic Clock Driver
2CLKA	Dual Basic Clock Driver
CLKAP	Basic Clock Driver + Inverter
CLKAM	Basic Clock Driver + Inverter
CLKB	Large Clock Driver + Inverter
DRV3	Triple Output Internal Driver
DRV6	Hex Output Internal Driver
TM	Buffered Transmission Gate
2TM	Transmission Gate for 2 to 1 Multiplexing
BDR	Bus Driver
DL	Data Latch
DL2	Data Latch
DLRS	Data Latch with Set and Reset
DLARS	Data Latch with Set and Reset
DF	Master-Slave D-Type Flip-Flop
DFRS	Master-Slave D-Type Flip-Flop with Set and Reset
MDF	Multiplexed Master-Slave D-Type Flip-Flop
MDFRS	Multiplexed Master-Slave D-Type Flip-Flop with Set and Reset
M3DF	3 to 1 Multiplexed Master-Slave D-Type Flip-Flop
M3DFRS	3 to 1 Multiplexed Master-Slave D-Type Flip-Flop with Set and Reset
JK	J K Flip-Flop
JKRS	J K Flip-FLop with Set and Reset
JBARK	J K Flip-Flop
JBARKRS	J K Flip-Flop with Set and Reset
BDL	Buffered Data Latch
BDLRS	Buffered Data Latch with Set and Reset
BDLARS	Buffered Data Latch with Set and Reset
BDF	Buffered Master-Slave D-Type Flip-Flop
BDFRS	Buffered Master-Slave D-Type Flip-Flop with Set and Reset
BMDF	Buffered Multiplexed Master-Slave D-Type Flip-Flop
BMDFRS	Buffered Multiplexed Master-Slave D-Type Flip-Flop with Set and Reset
TRID	Tri-State Driver

Intermediate Buffers:

IBST1	Input Buffer with CMOS switching level
IBST2	Input Buffer with 2V switching level
IBSK1	Driver with Lightly Skewed Outputs
IBSK2	Driver with Medium Skewed Outputs
IBSK3	Driver with Heavily Skewed Outputs
IBTRID	Tri-State Driver
IBTRID1	Tri-State Driver with Lightly Skewed Outputs + 2 Inverters
IBTRID2	Tri-State Driver with Medium Skewed Outputs + 2 Inverters
IBTRID3	Tri-State Driver with Heavily Skewed Outputs + 2 Inverters
IBGATE	Large 2-Input NAND Gate + Large 2-Input NOR Gate
IB2D	Dual High Power Inverters
IBCLKB	Large Clock Driver
IBDF	Master-Slave D-Type Flip-Flop
IBDFA	Master-Slave D-Type Flip-Flop
IBCMOS1	CMOS Input Buffer and Large 2-Input NAND Gate
IBCMOS2	CMOS Input Buffer and Data Latch
IBTTL1	TTL Input Buffer and Large 2-Input NAND Gate
IBTTL2	TTL Input Buffer and Data Latch

Input Buffer:

IPNR	Input Cell (with no Pullup or Pulldown resistors)
IPR1P	Input Cell with 1K-Ohm Pull-up Resistor
IPR1M	Input Cell with 1K-Ohm Pull-down Resistor
IPR2P	Input Cell with 2K-Ohm Pull-up Resistor
IPR2M	Input Cell with 2K-Ohm Pull-down Resistor
IPR3P	Input Cell with 4K-Ohm Pull-up Resistor
IPR3M	Input Cell with 4K-Ohm Pull-down Resistor
IPR4P	Input Cell with 100K-Ohm Pull-up Resistor
IPR4M	Input Cell with 100K-Ohm Pull-down Resistor

Output Buffers:

OP1	Smallest Drive Output Buffer
OP2	Small Drive Output Buffer
OP3	Standard Drive Output Buffer
OP6	Medium Drive Output Buffer
OP12	Large Drive Output Buffer
OP5B	Standard Drive Non-Inverting Output Buffer
OP11B	Large Drive Non-Inverting Output Buffer
OPT1	Smallest Drive Tri-State Output Buffer
OPT2	Small Drive Tri-State Output Buffer
OPT3	Standard Drive Tri-State Output Buffer
OPT6	Medium Drive Tri-State Output Buffer

OPT12	Large Drive Tri-State Output Buffer
OPT4B	Standard Drive Non-Inverting Tri-State Output Buffer
OPT10B	Large Drive Non-Inverting Tri-State Output Buffer
OPOD1	Smallest Drive Open-Drain Output Buffer
OPOD2	Small Drive Open-Drain Output Buffer
OPOD3	Standard Drive Open-Drain Output Buffer
OPOD6	Medium Drive Open-Drain Output Buffer
OPOD12	Large Drive Open-Drain Output Buffer
OPOD5B	Standard Drive Non-Inverting Open Drain Output Buffer
OPOD11B	Large Drive Non-Inverting Open Drain Output Buffer
OPOS1	Smallest Drive Open-Source Output Buffer
OPOS2	Small Drive Open-Source Output Buffer
OPOS3	Standard Drive Open-Source Output Buffer
OPOS6	Medium Drive Open-Source Output Buffer
OPOS12	Large Drive Open-Source Output Buffer
OPOS5B	Standard Drive Non-Inverting Open-Source Output Buffer
OPOS11B	Large Drive Non-Inverting Open-Source Output Buffer

Supply Pads:

OPVP	VDD Power Pad (Outputs)
OPVM	GND Power Pad (Outputs)
OPVPB	VDD Power Pad (Outputs):Break in VDD
OPVMB	GND Power Pad (Outputs):Break in GND
OPVPBB	VDD Power Pad (Outputs):Break in VDD and GND
OPVMBB	GND Power Pad (Outputs):Break in GND and VDD
IBVP	VDD Power Pad (Buffers)
IBVM	GND Power Pad (Buffers)
IBVPB	VDD Power Pad (Buffers):Break in VDD
IBVMB	GND Power Pad (Buffers):Break in GND
IBVPBB	VDD Power Pad (Buffers):Break in VDD and GND
IBVMBB	GND Power Pad (Buffers):Break in GND and VDD
LAVP1	Power Pad for Logic Array
LAVP2	Power Pad for Logic Array
LAVP3	Power Pad for Logic Array
LAVP4	Power Pad for Logic Array
LAVP5	Power Pad for Logic Array
LAVM1	Power Pad for Logic Array
LAVM2	Power Pad for Logic Array
LAVM3	Power Pad for Logic Array
LAVM4	Power Pad for Logic Array
LAVM5	Power Pad for Logic Array
LAGND	Power Pad for Logic Array
LAVDD	Power Pad for Logic Array

Analogue Cells:

OSC1	Crystal Oscillator Peripheral Cell
ANIPCMP1	Comparator - Standard
ANIPCMP2	Comparator - Low Power
ANADC4	Four Bit Analogue To Digital Converter
ANDAC4	Four Bit Digital To Analogue Converter
ANVREFGN	Reference Generator/Power On Reset
ANVREFSH	Shunt Regulator/Power On Reset

a) Memory Cells

RAM2	2 bit memory
RAM4	4 bit memory
RAM8	8 bit memory
RAM16	16 bit memory
RAM32	32 bit memory
RAM64	64 bit memory

b) Single port decoder cells

RAD2S	2 words (1-16 bits RAM)
RAD2SL	2 words (17-64 bits RAM)
RAD4S	4 words (1-16 bits RAM)
RAD4SL	4 words (17-64 bits RAM)
RAD8S	8 words (1-16 bits RAM)
RAD8SL	8 words (17-64 bits RAM)
RAD16S	16 words (1-16 bits RAM)
RAD16SL	16 words (17-64 bits RAM)
RAD32S	32 words (1-16 bits RAM)
RAD32SL	32 words (17-64 bits RAM)
RAD64S	64 words (1-16 bits RAM)
RAD64SL	64 words (17-64 bits RAM)

c) Dual port decoder cells

RAD2D	2 words (1-16 bits RAM)
RAD2DL	2 words (17-64 bits RAM)
RAD4D	4 words (1-16 bits RAM)
RAD4DL	4 words (17-64 bits RAM)
RAD8D	8 words (1-16 bits RAM)
RAD8DL	8 words (17-64 bits RAM)
RAD16D	16 words (1-16 bits RAM)
RAD16DL	16 words (17-64 bits RAM)
RAD32D	32 words (1-16 bits RAM)
RAD32DL	32 words (17-64 bits RAM)
RAD64D	64 words (1-16 bits RAM)
RAD64DL	64 words (17-64 bits RAM)

Macro Cells:

a) Adders

ADA4	4 bit binary full adders with fast carry
ADG4	Look ahead carry generator

b) Counters

CNA4	BCD counter/4 bit latch BCD decoder/ driver
CNB4	4 bit counter latch
CNC4	4 bit synchronous counter
CND4	4 bit synchronous binary up/down counter
CND4A	4 bit synchronous binary up/down counter with reset
CNE4	4 bit decade counter
CNF4	4 bit synchronous binary counter
CNG4	4 bit synchronous binary counter with enable

c) Decoders

DRA3T8	3 line to 8 line decoder/demultiplexer
DRA4T16	4 line to 16 line decoder/demultiplexer
DRA4T16A	4 line to 16 line decoder/demultiplexer with no enable
DRB3T8	3 line to 8 line decoder/demultiplexer with address registers
DRC3T8	3 line to 8 line decoder/demultiplexer with address latches
DRD2T4	2 line to 4 line decoder/demultiplexer
DRF4T101	4 line to 10 line BCD decoder
DRG4T10	4 line to 10 line Excess 3 to decimal decoder
DRH4T10	4 line to 10 line Excess Gray to decimal decoder
DRI10	BCD to decimnal decoder/driver
DRJ7	BCD to 7-Segment decoder/driver
DRK7	BCD to 7-Segment decoder/driver

d) Encoders

ENA8T3	8 line to 3 line priority encoder
ENB10T4	10 line to 4 line priority encoder

e) Flip-Flops

FFA8	8 bit bistable latches
FFB6	6 bit D-type flip-flops with clear
FFC4	4 bit D-type flip-flops with clear and complementary outputs
FFD8	Octal D-type flip-flops with clear

f) ALU/Function generator

FGA4 Arithmetic logic unit/function generator

g) Magnitude comparator

MCA4	4 bit magnitude comparators

h) Multipliers

MLA10	Decade rate multiplier
MLB4X4	4 bit binary multiplier with tristate outputs
MLW7	7 bit slice Wallace tree with tristate outputs

i) Multiplexors

MXA8T1	8 line to 1 line data selector/multiplexer
MXB4T1	4 line to 1 line data selector/multiplexer with tristate outputs
MXB4T1A	4 line to 1 line data selector/multiplexer with inverted tristate outputs
MXC2T1	Quad 2 line to 1 line data selector/ multiplexer
MXC2T1A	Quad 2 line to 1 line data selector/ multiplexer with inverted outputs
MXD4T1	4 line to 1 line data selector/multiplexer
MXE4T1	Dual 4 line to 1 line data selector/ multiplexer
MXF2T1	Quad 2 line to 1 line multiplexer with storage

j) Parity generators

PGA	9 bit odd/even generator/check

k) Shift registers

SRA2	2 bit parallel out serial shift registers with clear
SRA4	4 bit parallel out serial shift registers with clear
SRA8	8 bit parallel out serial shift registers with clear
SRA8A	8 bit parallel out serial shift registers with no clear
SRB2	2 bit parallel in serial shift registers with clear
SRB4	4 bit parallel in serial shift registers with clear
SRB8	8 bit parallel in serial out shift registers with clear
SRB8A	8 bit parallel in serial out shift registers with no clear
SRC8	8 bit parallel in serial out shift registers
SRD4	4 bit parallel in serial out shift registers
SRE4	4 bit parallel in serial out shift registers
SRE4	4 bit parallel in serial out shift registers with J.KBAR input
SRF8	8 bit shift and store register with tristate outputs
SRG4	4 bit bidirectional universal shift registers
SRJ4	4 bit parallel access shift registers
SRK5	5 bit shift register

i) Monitor

PERF	Performance monitor for CLA60000

m) Built in Test

RGBIT	User Bit for use in BIST circuit
RGCTL	Control unit for use in BIST circuits
RGDIAG	Diagnostic unit for use in BIST circuits
RGHOLD	Hold Bit for use in BIST circuit
RGTBIT	Test Bit for use in BIST circuit

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