

Input selector for high resolution displays

BH7659S / BH7659FS

The BH7659S / BH7659FS are input signal switching ICs developed for high resolution displays that have three $f_c = 250\text{MHz}$ wide-band video switching circuits for RGB video signal switching and four CMOS analog switching circuits for switching between H_b and V_b signals as well as I²C bus signals (SDA and SCL).

●Applications

High-resolution displays and high-definition TVs

●Features

- 1) Operates with a 5V power supply voltage.
- 2) Built-in, wide-band switching circuit for RGB switching ($f_c = 250\text{MHz}$).
- 3) SDA and SCL as well as H_b and V_b signal switching is possible.
- 4) Built-in power save function.

●Absolute maximum ratings ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{cc}	8.0	V
Power dissipation	Pd	1300*1 (SDIP32)	mW
		800*2 (SSOP-A32)	
Operating temperature	T_{opr}	- 25 ~ + 75	°C
Storage temperature	T_{stg}	- 55 ~ + 125	°C

*1 Reduced by 13mW for each increase in T_a of 1°C over 25°C.

*2 Reduced by 8.0mW for each increase in T_a of 1°C over 25°C.

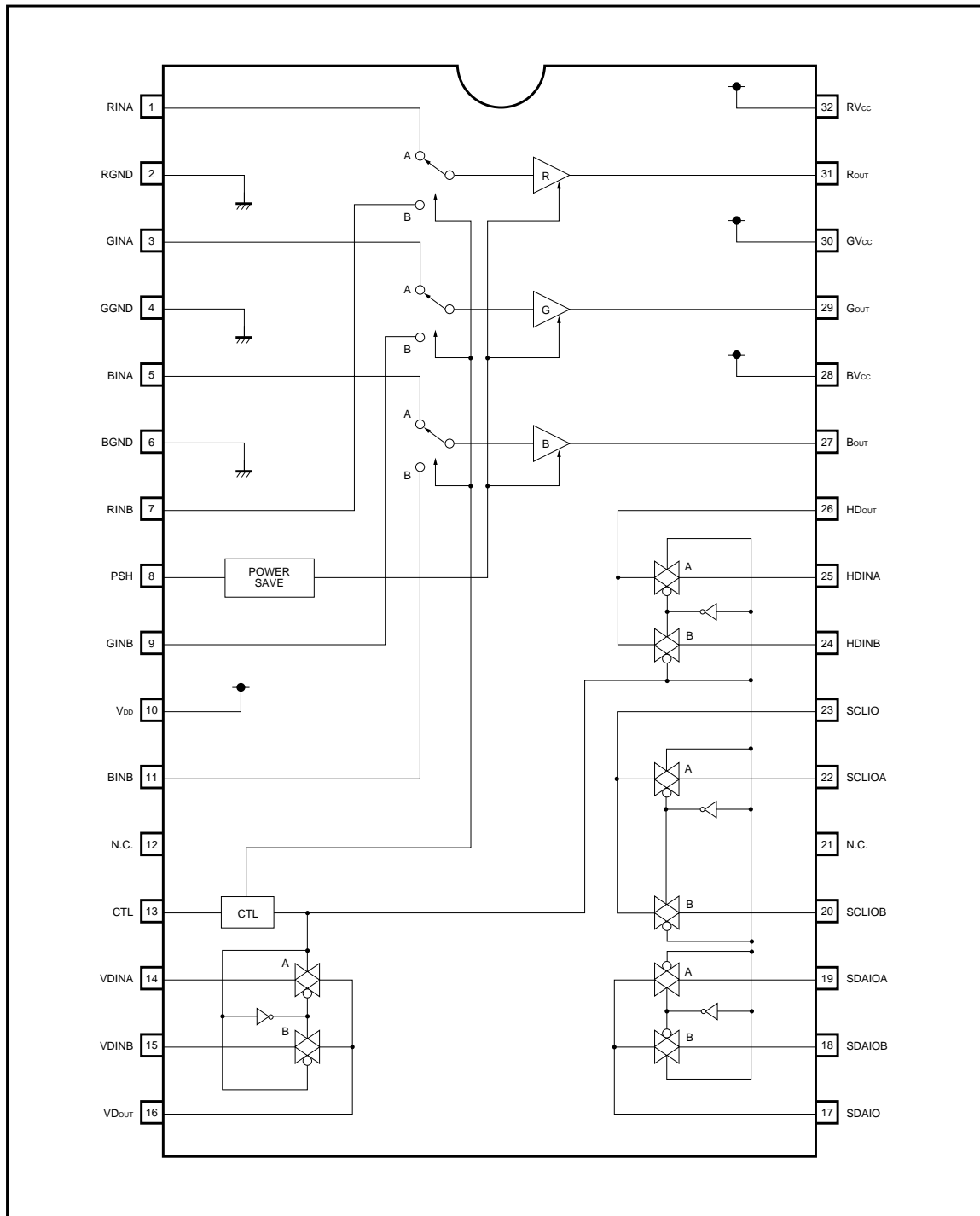
●Recommended operating conditions ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating power supply voltage	V_{cc}	4.5	5.0	5.5	V

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●Block diagram



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●Input / Output equivalent circuits

Pin No.	Pin description (pin name)	Reference potential	Input / output circuit	Function
1 3 5 7 9 11	Red signal input A (RINA) Green signal input A (GINA) Blue signal input A (BINA) Red signal input B (RINB) Green signal input B (GINB) Blue signal input B (BINB)	3.5V when selected 0V when not selected ⁸		Switches between the two RGB signaling systems. Input B is selected by setting the CTL pin to high and input A to low.
27 29 31	Blue signal output (BOUT) Green signal output (GOUT) Red signal output (ROUT)	1.85V		Power save activates by setting the PSH pin to high.
8 9	Power save input (PSH) Control input (CTL)	0V		PSH Power save off $\leq 1.5V$ Power save on $\geq 3.5V$ CTL Input A $\geq 3.5V$ Input B $\leq 1.5V$

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Pin No.	Pin description (pin name)	Reference potential	Input / output circuit	Function
14	VD signal input A (VDINA)			<p>Switches between the two VD, HD, SDA, and SCL signaling systems.</p> <p>Input B is selected by setting the CTL pin to high and input A to low.</p> <p>Bi-directional I / O is possible with CMOS analog switch</p>
15	VD signal input B (VDINB)			
16	VD signal output (VDOUT)			
17	SDA signal I / O (SDAIO)			
18	SDA signal I / O B (SDAIOB)			
19	SDA signal I / O A (SDAIOA)			
20	SCL signal I / O B (SCLIOB)			
22	SCL signal I / O A (SCLIOA)			
24	SCL signal I / O (SCLIO)			
25	HD signal input B (HDINB)			
26	HD signal input A (HDINA)			
27	HD signal output (HDOUT)			
2	Red ground (RGND)	0V		
4	Green ground (GGND)	0V	—	Green video SW block GND
6	Blue ground (BGND)	0V	—	Blue video SW block and CMOS SW block GND
10	CMOS power supply voltage (V _{DD})	5V	—	CMOS SW block V _{DD}
28	Blue power supply voltage (BV _{CC})	5V	—	Blue video SW block V _{CC}
30	Green power supply voltage (GV _{CC})	5V	—	Green video SW block V _{CC}
32	Red power supply voltage (RV _{CC})	5V	—	Red video SW block V _{CC}

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● **Electrical characteristics** (unless otherwise noted, $V_{CC}=5.0V$, $T_a = 25^\circ C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
(Overall device)						
Circuit current	I_{CC}	15	25	35	mA	—
Circuit current during power save	I_{PSV}	7	14	22	mA	PS = "H"
(R, G, and B video switches)						
Voltage gain	G_V	- 1.0	- 0.5	0	dB	$f = 10MHz$
Interchannel relative gain	ΔG_{VC}	- 0.5	0	0.5	dB	$f = 10MHz$
Interblock relative gain	ΔG_{VB}	- 0.5	0	0.5	dB	$f = 10MHz$
Output dynamic range	V_{OM}	2.6	—	—	V_{P-P}	$f = 1kHz$
(CMOS analog switch)						
On-resistance	R_{ON}	—	200	400	Ω	$V_{IN} = 2.5V$
Interchannel on-resistance difference	ΔR_{ON}	—	20	40	Ω	$V_{IN} = 2.5V$
Interchannel crosstalk	CT	—	- 70	- 55	dB	$f = 150kHz$
Transmission delay time	t_D	—	20	—	ns	$R_L = 10\Omega$, $C_L = 50pF$
(Control block)						
High level voltage	V_H	3.5	—	—	V	—
Low level voltage	V_L	—	—	1.5	V	—

● **Guaranteed design parameters** (unless otherwise noted, $V_{CC}=5.0V$, $T_a = 25^\circ C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
(R, G, and B video switches)						
Frequency characteristics 1	f_1	- 3.0	0	+ 1.0	dB	$f = 50MHz$
Frequency characteristics 2	f_2	- 6.0	- 3	- 1.0	dB	$f = 250MHz$
Interchannel relative frequency characteristics	Δf_C	- 0.5	0	0.5	dB	$f = 50MHz$
Interblock relative frequency characteristics	Δf_B	- 0.5	0	0.5	dB	$f = 50MHz$
Interchannel crosstalk 1	CT_{C1}	—	- 50	- 35	dB	$f = 50MHz$
Interchannel crosstalk 2	CT_{C2}	—	- 30	- 15	dB	$f = 250MHz$
Interblock crosstalk 1	CT_{B1}	—	- 50	- 35	dB	$f = 50MHz$
Interblock crosstalk 2	CT_{B2}	—	- 30	- 15	dB	$f = 250MHz$

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● Measurement circuit 1

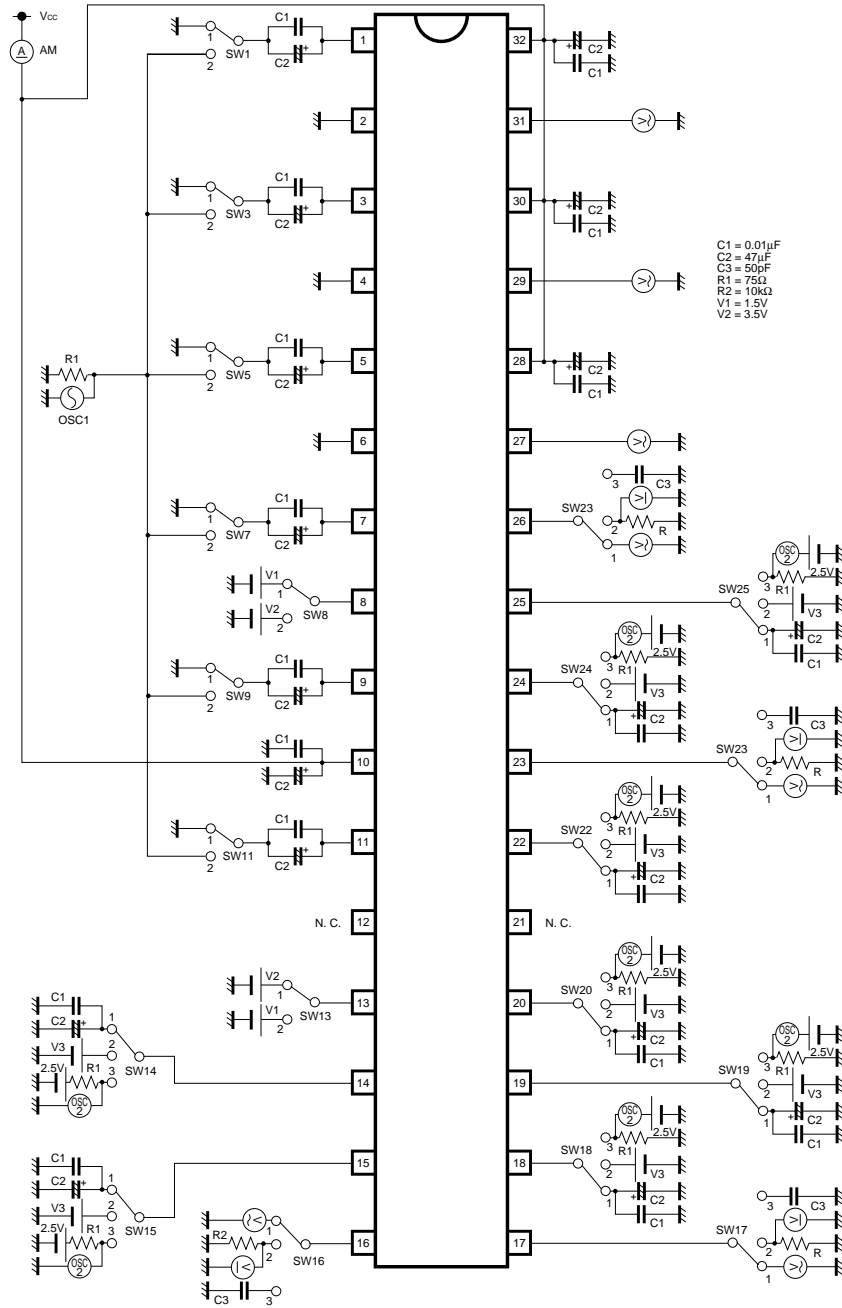


Fig.1

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● Measurement circuit 2

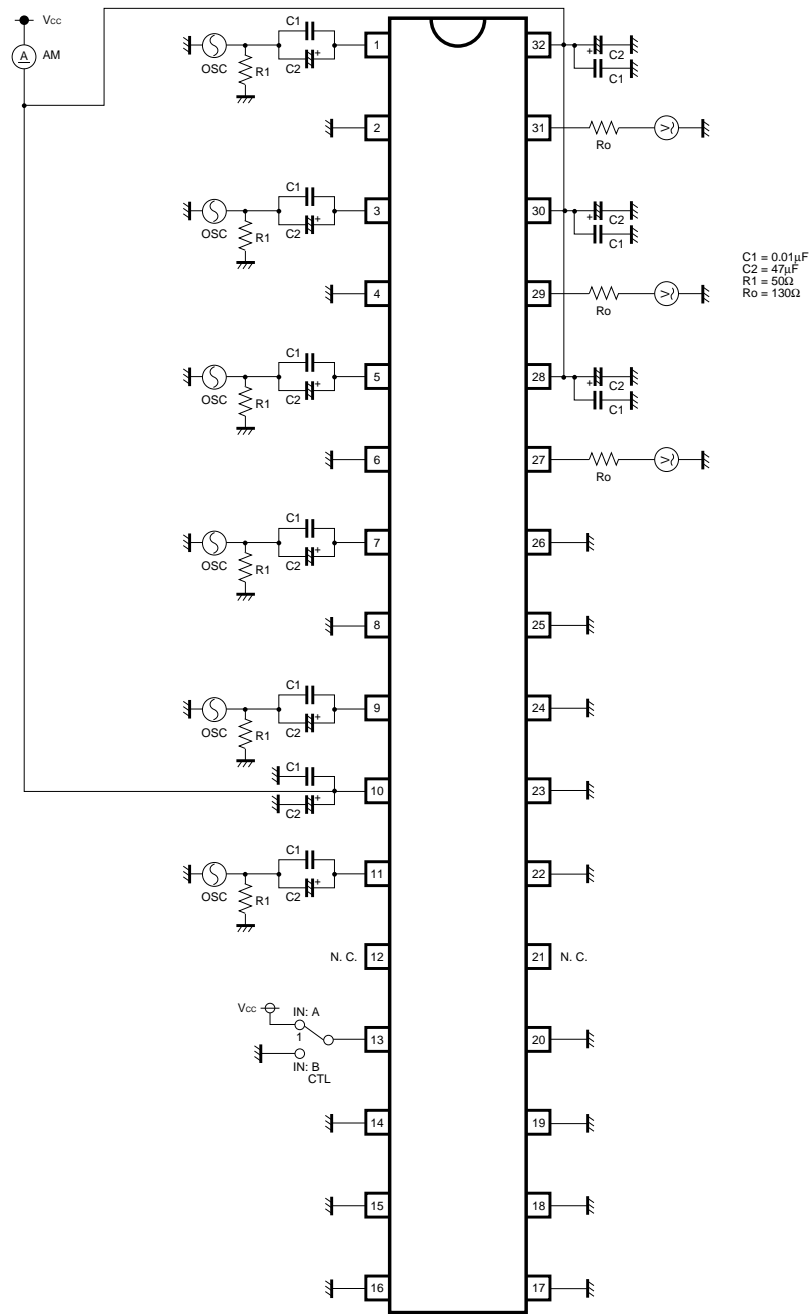


Fig.2

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● Measurement conditions

<Overall device> measurement circuit 1

Parameter	Switch conditions		Notes
	8	Others	
Circuit current	1	1	(1)
Circuit during power save	2	1	(2)

<R, G, and B video switches> measurement circuit 2

Parameter		Input pin: (OSC)						Switch conditions	Notes
		1	7	3	9	5	11	CTL	
Voltage gain (G_v)	RinA	○	—	—	—	—	—	IN: A	(3)
Output dynamic range (V_{OM})	RinB	—	○	—	—	—	—	IN: B	(6)
Frequency characteristics 1 (f_1)	GinA	—	—	○	—	—	—	IN: A	(7)
	GinB	—	—	—	○	—	—	IN: B	
Frequency characteristics 2 (f_2)	BinA	—	—	—	—	○	—	IN: A	(8)
	BinB	—	—	—	—	—	○	IN: B	
Interchannel crosstalk 1 (CT_{C1})	RinA→B	○	—	—	—	—	—	IN: B	(11)
	RinB→A	—	○	—	—	—	—	IN: A	
	GinA→B	—	—	○	—	—	—	IN: B	
Interchannel crosstalk 2 (CT_{C2})	GinB→A	—	—	—	○	—	—	IN: A	(12)
	BinA→B	—	—	—	—	○	—	IN: B	
	BinB→A	—	—	—	—	—	○	IN: A	
Interblock crosstalk 1 (CT_{B1})	G→RinA	—	—	○	—	—	—	IN: A	(13)
	B→RinA	—	—	—	—	○	—	IN: A	
	R→GinA	○	—	—	—	—	—	IN: A	
Interblock crosstalk 2 (CT_{B2})	B→GinA	—	—	—	—	○	—	IN: A	(14)
	R→BinA	○	—	—	—	—	—	IN: A	
	G→BinA	—	—	○	—	—	—	IN: A	
Interchannel relative gain: ΔG_{vc}									(4)
Interblock relative gain: ΔG_{vB}									(5)
Interchannel relative frequency characteristics: Δf_c									(9)
Interblock relative frequency characteristics: Δf_B									(10)

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<C-ROM analog switch> measurement circuit 1

Parameter		Switch conditions														Notes
		13	14	15	16	17	18	19	20	22	23	24	25	26	others	
On-resistance (R_{ON})	VDinA	1	2	1	2	1	1	1	1	1	1	1	1	1	1	(15)
	VDinB	2	1	2	2	1	1	1	1	1	1	1	1	1	1	
	SDinA	1	1	1	1	2	1	2	1	1	1	1	1	1	1	
	SDinB	2	1	1	1	2	2	1	1	1	1	1	1	1	1	
	SCinA	1	1	1	1	1	1	1	1	2	2	1	1	1	1	
	SCinB	2	1	1	1	1	1	1	2	1	2	1	1	1	1	
	HDinA	1	1	1	1	1	1	1	1	1	1	1	2	2	1	
	HDinB	2	1	1	1	1	1	1	1	1	1	2	1	2	1	
Interchannel crosstalk (CT)	VDinA→B	1	3	1	1	1	1	1	1	1	1	1	1	1	1	(17)
	VDinB→A	2	1	3	1	1	1	1	1	1	1	1	1	1	1	
	SDinA→B	1	1	1	1	1	1	3	1	1	1	1	1	1	1	
	SDinB→A	2	1	1	1	1	3	1	1	1	1	1	1	1	1	
	SCinA→B	1	1	1	1	1	1	1	1	3	1	1	1	1	1	
	SCinB→A	2	1	1	1	1	1	1	3	1	1	1	1	1	1	
	HDinA→B	1	1	1	1	1	1	1	1	1	1	1	3	1	1	
	HDinB→A	2	1	1	1	1	1	1	1	1	1	3	1	1	1	
Transmission delay time (t_D)	VDinA	1	3	1	3	1	1	1	1	1	1	1	1	1	1	(18)
	VDinB	2	1	3	3	1	1	1	1	1	1	1	1	1	1	
	SDinA	1	1	1	1	3	1	3	1	1	1	1	1	1	1	
	SDinB	2	1	1	1	3	3	1	1	1	1	1	1	1	1	
	SCinA	1	1	1	1	1	1	1	1	3	3	1	1	1	1	
	SCinB	2	1	1	1	1	1	1	3	1	3	1	1	1	1	
	HDinA	1	1	1	1	1	1	1	1	1	1	1	3	3	1	
	HDinB	2	1	1	1	1	1	1	1	1	1	3	1	3	1	
Interchannel on-resistance difference (ΔR_{ON})															(16)	

Notes:

- (1) Circuit current : I_{CC} ; measurement of the circuit current.
(2) Circuit current during power save : I_{PSV} ; measurement of the circuit current during power save.
(3) Voltage gain : G_V

$V_{IN} = 1.0V_{P-P}$, $f = 10MHz$ sine wave input from the OSC

$$G_V = 20 \log (V_{OUT} / V_{IN}) \text{ [dB]}$$

- (4) Interchannel relative gain : ΔG_{VC}

$$\Delta G_{VC} = G_V R_a - G_V R_b, G_V G_a - G_V G_b, G_V B_a - G_V B_b \text{ [dB]}$$

- (5) Interblock relative gain : ΔG_{VB}

$$\Delta G_{VB} = G_V R_a - G_V G_a, G_V R_a - G_V G_b, G_V R_a - G_V B_a, G_V R_a - G_V B_b \text{ [dB]}$$

$$\Delta G_{VB} = G_V G_a - G_V R_a, G_V G_a - G_V R_b, G_V G_a - G_V B_a, G_V G_a - G_V B_b \text{ [dB]}$$

$$\Delta G_{VB} = G_V B_a - G_V R_a, G_V B_a - G_V R_b, G_V B_a - G_V G_a, G_V B_a - G_V B_b \text{ [dB]}$$

- (6) Output dynamic range : V_{OM}

Connect a distortion meter to the output. After adding a $f = 1kHz$ sine wave input from the OSC, adjust the input level so that the output distortion is 1.0%.

The output voltage at that time is V_{OM} [V_{P-P}].

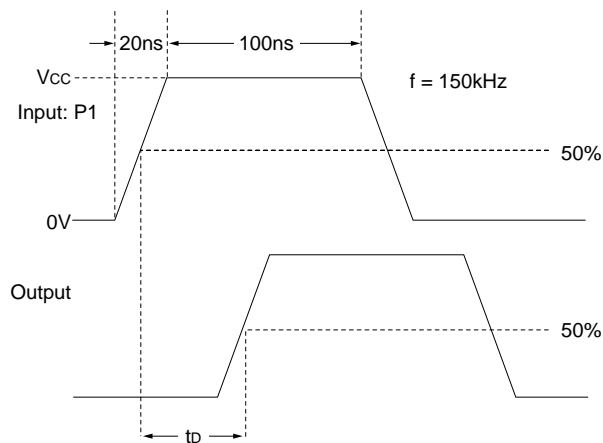
- (7) Frequency characteristics 1 : f_1

Apply to the input pin a $V_{IN} = 1.0V_{P-P}$, $f = 10MHz$ and $50MHz$ sine wave input from the OSC.

$$f_1 = G_V (50MHz) - G_V (10MHz) \text{ [dB]}$$

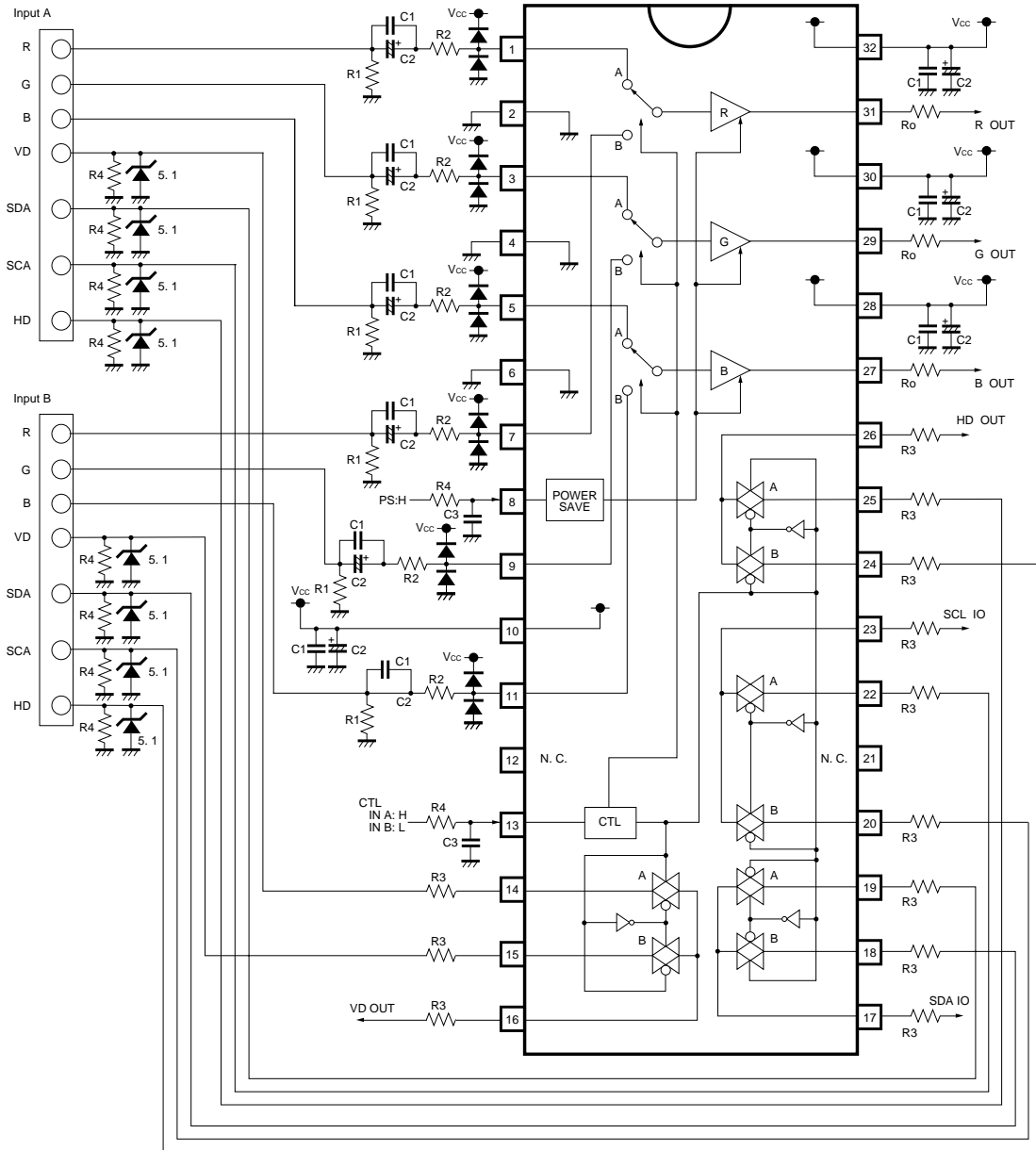
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- (8) Frequency characteristics 2 : f_2
 Apply to the input pin a $V_{IN} = 1.0V_{P-P}$, $f = 10MHz$ and $250MHz$ sine wave input from the OSC.
 $f_2 = G_V(250MHz) - G_V(10MHz)$ [dB]
- (9) Interchannel relative frequency characteristics : Δf_c
 $\Delta f_c = f_1(INA) - f_1(INB)$ [dB]
- (10) Interblock relative frequency characteristics : Δf_b
 $\Delta f_b = f_1(RINA) - f_1(GINA), f_1(GINA) - f_1(BINA), f_1(BINA) - f_1(RINA)$ [dB]
 $= f_1(RINB) - f_1(GINB), f_1(GINB) - f_1(BINB), f_1(BINB) - f_1(RINB)$ [dB]
- (11) Interchannel crosstalk 1 : CT_{C1}
 Apply to the input pin a $V_{IN} = 1.0V_{P-P}$, $f = 50MHz$ sine wave input from the OSC.
 $CT_{C1} = 20\log(V_{OUT} / V_{IN})$ [dB]
- (12) Interchannel crosstalk 2 : CT_{C2}
 Apply to the input pin a $V_{IN} = 1.0V_{P-P}$, $f = 250MHz$ sine wave input from the OSC.
 $CT_{C2} = 20\log(V_{OUT} / V_{IN})$ [dB]
- (13) Interblock crosstalk 1 : CT_{B1}
 Apply to the input pin a $V_{IN} = 1.0V_{P-P}$, $f = 50MHz$ sine wave input from the OSC.
 $CT_{B1} = 20\log(V_{OUT} / V_{IN})$ [dB]
- (14) Interblock crosstalk 2 : CT_{B2}
 Apply to the input pin a $V_{IN} = 1.0V_{P-P}$, $f = 250MHz$ sine wave input from the OSC.
 $CT_{B2} = 20\log(V_{OUT} / V_{IN})$ [dB]
- (15) On-resistance : R_{ON}
 $\Delta R_{ON} = (V_{OUT} / V_{IN} - 1) \times 10^4$ [Ω]
- (16) Interchannel on-resistance difference : ΔR_{ON}
 $\Delta R_{ON} = R_{ON}(INA) - R_{ON}(INB)$
- (17) Interchannel crosstalk : CT
 Apply to the input pin a $V_{IN} = 1.0V_{P-P}$, $f = 150MHz$ sine wave input from the OSC2.
 $CT = 20\log(V_{OUT} / V_{IN})$ [dB]
- (18) Transmission delay time : t_d
 Apply to the input pin the rectangular wave of P1 from the OSC2.



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●Application example



Note: The R_o value differs depending on the load capacitance.

Set so that the frequency characteristics are flat.

$R_1 = 75\Omega$ $C_1 = 0.01\mu F$

$R_2 = 47\Omega$ $C_1 = 47\mu F$

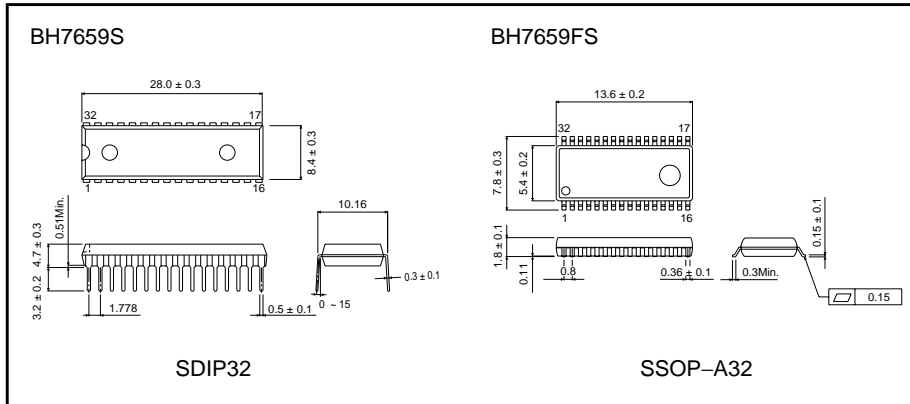
$R_3 = 100\Omega$ $C_1 = 0.1\mu F$

$R_4 = 1.2k\Omega$

Fig.3

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●External dimensions (Units : mm)



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