SIEMENS

Microcontrollers

ApNote   AP163702

Reset and System Startup Configuration via PORT0

This application note presents an overview about the different reset types and the behaviour concerning the system startup configuration via PORT0. The calculation for the Pull-up/down resistors at PORT0 is also included.

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1   Overview about the different Reset Sources

During reset, the device executes a special internal sequence in order to set inside signals and the special function registers to their specified default values. The contents of some special function registers are controlled during system startup configuration via PORT0.

The system startup configuration is sampled upon different reset events. See table 1:
- Hardware Reset: - Power-on Reset
                           - Short Hardware Reset (Warm Reset)
                           - Long Hardware Reset (Power Down Wakeup Reset)

- Software Reset
- Watchdog Timer Reset

Reset Source	Short-cut	Condition
Power-on Reset	PONR	Power-on
Short Hardware Reset	SHWR	$4 \text{ TCL} < t_{RSTIN} \leq 1024 \text{ TCL}$
Long Hardware Reset	LHWR	$t_{RSTIN} > 1024 \text{ TCL}$
Watchdog Timer Reset	WDTR	WDT overflow
Software Reset	SWR	SRST command

Table 1:
Reset Sources and Reset Conditions

1.1   Hardware Reset

A hardware reset is triggered when the reset input signal $\overline{\text{RSTIN}}$ is latched low. To ensure the recognition of the $\overline{\text{RSTIN}}$ signal (latching), it must be held low for at least 2 CPU clock cycles (4 TCL = 100 nsec @ 20 MHz CPU Clock). Also shorter $\overline{\text{RSTIN}}$ pulses may trigger a hardware reset, if they coincide with the latch's sample point. However, for microcontrollers with an on-chip PLL it is recommended to keep $\overline{\text{RSTIN}}$ low for ca. 1 msec to guarantee that the PLL is locked. After the reset sequence has been completed, the $\overline{\text{RSTIN}}$ input is sampled. When the reset input signal is active at that time the internal reset condition is prolonged until $\overline{\text{RSTIN}}$ gets inactive.
The input $\overline{\text{RSTIN}}$ provides an internal pullup device equalling a resistor of 50 KΩ to 150 KΩ (the minimum reset time must be determined by the lowest value). Simply connecting an external capacitor is sufficient for an automatic power-on reset. $\overline{\text{RSTIN}}$ may also be connected to the output of other logic gates.

Three different kinds of external hardware resets have to be considered:

a) Power-on Reset
   A complete power-on reset requires an active $\overline{\text{RSTIN}}$ time of two reset sequences (2 * 1024 TCL = 51.2 μsec @ 20 MHz CPU Clock) after a stable clock signal is available.

Depending on the oscillation frequency the on-chip oscillator needs about 2...50 ms to stabilize.

b) Long Hardware Reset

A long hardware reset requires an active $\overline{\text{RSTIN}}$ time longer than the duration of the internal reset sequence. The duration of the internal reset sequence is 1024 TCL (1024 TCL = 25.6 µsec @ 20 MHz CPU Clock). The long hardware reset is also named power down wakeup reset.

c) Short Hardware Reset

The active $\overline{\text{RSTIN}}$ time of a short hardware reset is between 4 TCL and 1024 TCL. If the $\overline{\text{RSTIN}}$ signal is active for at least 4 TCL clock cycles (100 nsec @ 20 MHz CPU Clock) the internal reset sequence is started (1024 TCL, 25.6 µsec @ 20 MHz CPU Clock). After the internal reset sequence has been completed, the $\overline{\text{RSTIN}}$ input is sampled. When the reset input is still active at that time the internal reset condition is prolonged until $\overline{\text{RSTIN}}$ gets inactive. If the $\overline{\text{RSTIN}}$ signal is active for more then 1024 TCL then the behaviour of the PORT0 latch mechanism is equal to a long hardware reset.

1.2 Software Reset

The reset sequence can be triggered at any time via the protected instruction SRST (Software Reset). This instruction can be executed deliberately within a program, e.g. to leave bootstrap loader mode, or upon a hardware trap that reveals a system failure.

1.3 Watchdog Timer Reset

When the watchdog timer is not disabled during the initialization or serviced regularly during program execution it will overflow and trigger the reset sequence. The watchdog timer reset releases automatically a software reset. Other than a hardware reset the watchdog timer reset completes a running external bus cycle if this bus cycle either does not use $\overline{\text{READY}}$ at all, or if $\overline{\text{READY}}$ is sampled active (low) after the programmed waitstates. When $\overline{\text{READY}}$ is sampled inactive (high) after the programmed waitstates the running external bus cycle is aborted. Then the internal reset sequence is started.

Note: The watchdog timer reset cannot occur while the device is in bootstrap loader mode!

1.4 Bidirectional Reset

The bidirectional reset is a new feature and implemented since the devices and steps listed below. The steps in parentheses do only reflect a software- or watchdog timer Reset to $\overline{\text{RSTIN}}$ but not a short hardware reset as shown in figure 7.

C161RI	AA	- Step	C161CI	AA	- Step
C164CI-8EM	AA	- Step	C167CS-32FM	AA	- Step
C167CR-LM	(CA), CB	- Step	C167S-4RM	(BA), BB	- Step
C167CR-4RM	(AB), AC	- Step			

In bidirectional reset mode the device's line $\overline{\text{RSTIN}}$ (normally an input) may be driven active by the chip logic e.g. in order to support external equipment which is required for startup (e.g. flash memory).
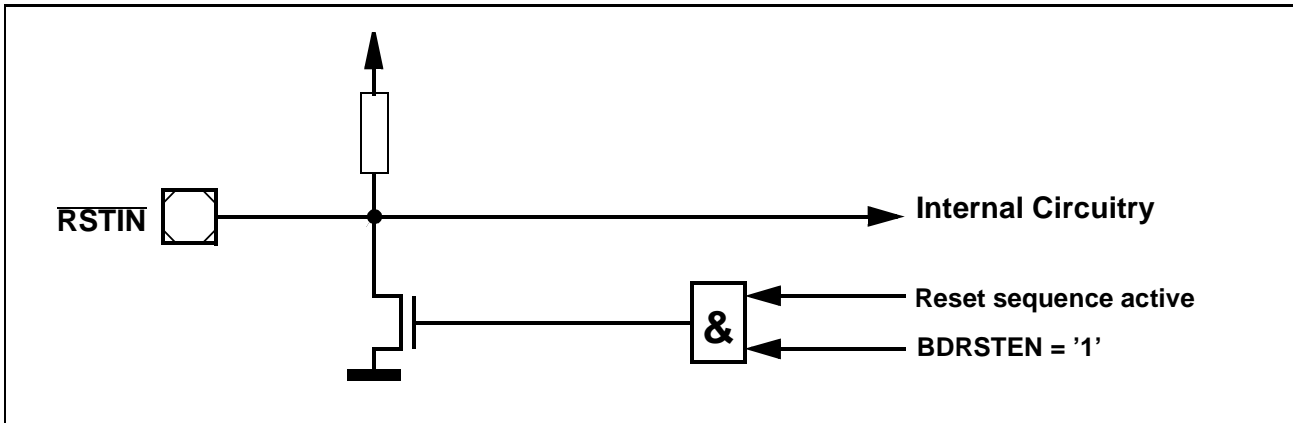
Figure 1 :
Bidirectional Reset Operation

Bidirectional reset reflects internal reset sources (software, watchdog) also to the $\overline{\text{RSTIN}}$ pin and converts short hardware reset pulses to a minimum duration of the internal reset sequence. Bidirectional reset is enabled by setting bit BDRSTEN in register SYSCON (SYSCON.3) and changes $\overline{\text{RSTIN}}$ from a pure input to an open drain IO line with an integrated pull-up resistor. When an internal reset is triggered by the SRST instruction or by a watchdog timer overflow or a low level is applied to the $\overline{\text{RSTIN}}$ line, an internal driver pulls it low for the duration of the internal reset sequence. After that it is released and is then controlled by the external circuitry alone.

The bidirectional reset function is useful in applications where external devices require a defined reset signal but cannot be connected to the device's $\overline{\text{RSTOUT}}$ signal, e.g. an external flash memory which must come out of reset and deliver code well before $\overline{\text{RSTOUT}}$ can be deactivated via EINIT.

The following behaviour differences must be observed when using the bidirectional reset feature in an application:

• Bit BDRSTEN in register SYSCON cannot be changed after EINIT.
• After a reset bit BDRSTEN is cleared (bidirectional reset is disabled).
• Bit WDTR will always be '0', even after a watchdog timer reset.
• The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap
  loader maybe activated when P0L.4 is low.
• Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.

2 System Startup Configuration

Some system features have to be selected before the first program execution is performed. These selections are made during reset via the Pins of PORT0, which are latched at the end of reset.

2.1 Overview about PORT0 Configuration during Reset

PORT0 startup configuration is sampled either with the end of the internal reset sequence or with the end of the external hardware reset. If the external $\overline{\text{RSTIN}}$ signal is deactivated before the end of the internal reset sequence (short hardware reset) then an internal reset signal (IRS) of the device is used to latch the system startup configuration at PORT0, else (power-on reset or long hardware reset) PORT0 is latched after the rising edge of $\overline{\text{RSTIN}}$ with the IRS. The sampling point of PORT0 is 7 TCL (prescaler enabled) or 10 TCL (direct drive or PLL) after the rising edge of $\overline{\text{RSTIN}}$ as shown in the PORT0 sample timing (see figures below).

The duration of one internal reset sequence is 1024 TCL for initializing the internal special function registers plus 10 TCL for the jump to address 00'0000$_H$ after the internal reset sequence.

As already mentioned the bidirectional reset feature converts software reset, WDT reset or short hardware reset to an externally visible hardware reset with a duration of 1024 TCL. This feature is disabled after hardware reset and can be enabled via software.

X : Pin is sampled -: Pin is not transparent and not sampled	BDRST	PORT0: Clock options			Segm.	Addr. Lines	Chip Selects	WR Config.	Bus Type		Reserved	BSL	Reserved	Reserved	Adapt Mode	Emu Mode	Invert P0H.7	Ext. Access Enable	(OWD disable)
Sample event	-	P0H.7	P0H.6	P0H.5	P0H.4	P0H.3	P0H.2	P0H.1	P0H.0	P0L.7	P0L.6	P0L.5	P0L.4	P0L.3	P0L.2	P0L.1	P0L.0	$\overline{\text{EA}}$	$\overline{\text{RD}}$
PONR	OFF	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
LHWR	ON/OFF	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SHWR	OFF	-	-	-	X	X	X	X	X	X	X	X	X	X	X	X	-	X	X
WDTR/SWR	OFF	-	-	-	X	X	X	X	X	X	-	-	-	-	-	-	-	X	X
SHWR	ON	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
WDTR/SWR	ON	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 2:
System Startup Configuration via PORT0

2.2 PORT0 Sample Timing for the different Reset Types

The different reset sources and timing relations at PORT0 during and at the end of reset are shown below. If a reset event occurs then PORT0 is switched to input mode and the internal pull-ups are active. During that time it is possible that the desired input voltage levels at PORT0 (V_{IH} and V_{IL} forced by the internal/external pull-ups and pull-downs for the startup configuration) are not reached. Therefore PORT0 is **not** transparent for 1024TCL (power-on reset for 2048 TCL) to prevent unexpected behaviour to the system. After that time a part of PORT0 becomes transparent and at the end of reset these pins are sampled with the IRS signal.

Depending on the reset type some PORT0 pins are not transparent, e.g. P0L.1 and P0L.0 which control Adapt Mode and Emulation Mode. Noise on these lines during reset would force the microcontroller to Adapt Mode or Emulation Mode. Therefore both pins are not transparent until the sample point IRS at the end of the reset condition.

The PORT0 sample timings shown below are based on the following conditions:

t_{P0fix}: During t_{P0fix} PORT0 has to be constant so the System Startup Configuration is latched correctly.

t_{SHR}: Duration of a short hardware reset. 4 TCL < t_{SHR} ≤ 1024 TCL

IRS: Internal Reset Signal: Sampling point of PORT0 configuration bits is 7 TCL (prescaler enabled) or 10 TCL (direct drive or PLL) after the rising edge of $\overline{\text{RSTIN}}$ or after the end of the internal reset sequence.
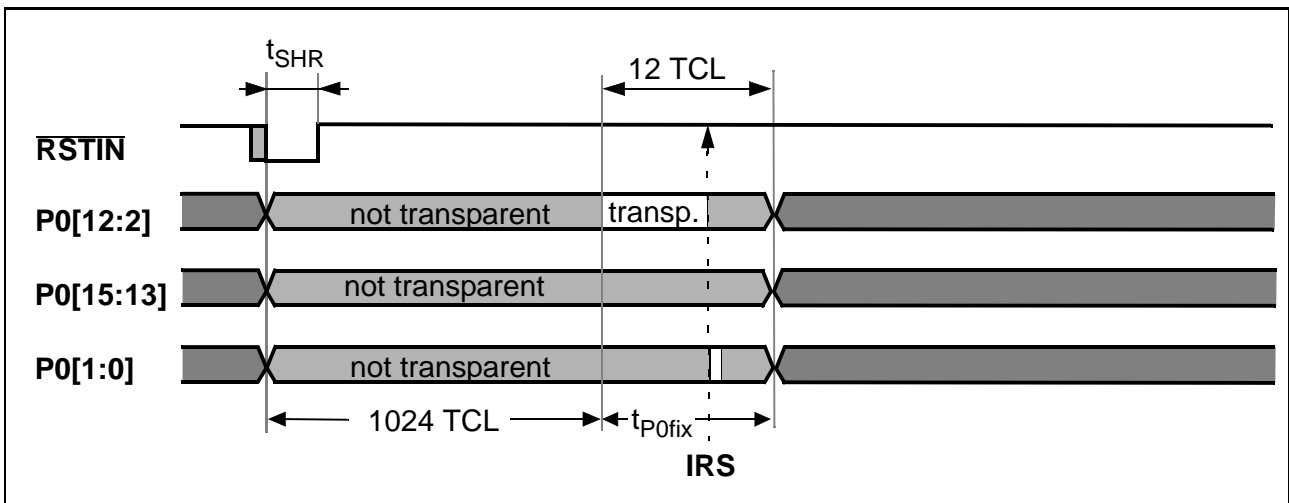
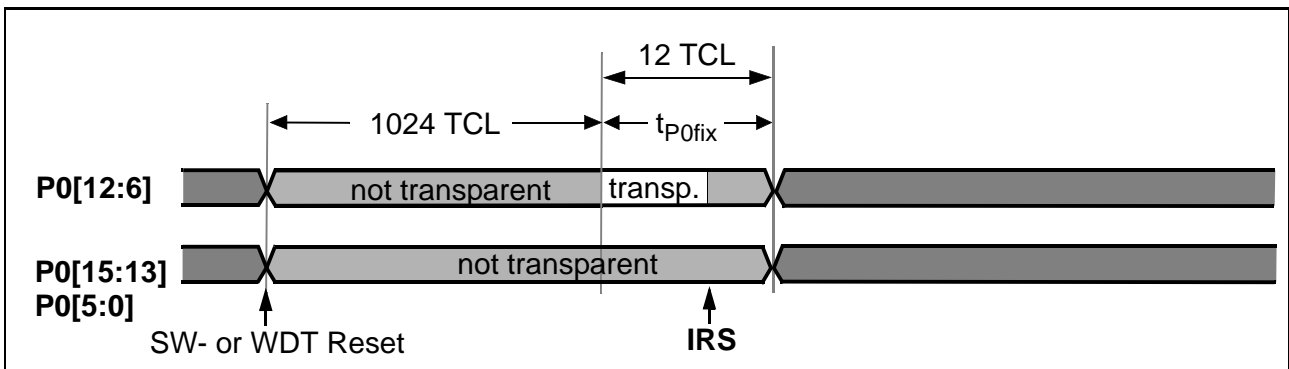TCL: 1 TCL = 1 / (2 *f_{CPU}), 1 TCL = 25 nsec @ 20 MHz CPU Clock
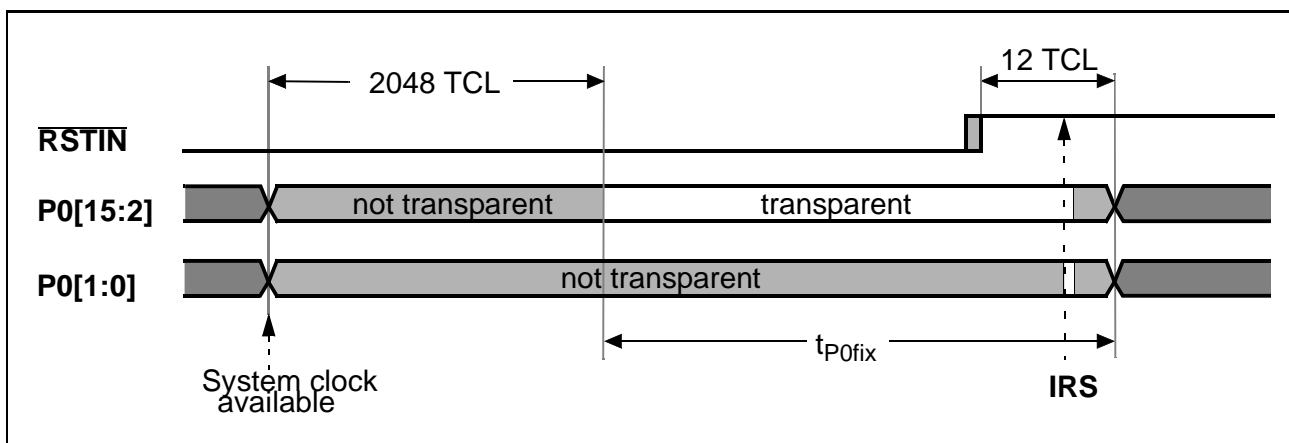
Figure 2 :
PORT0 sample Timing: Power-on Reset
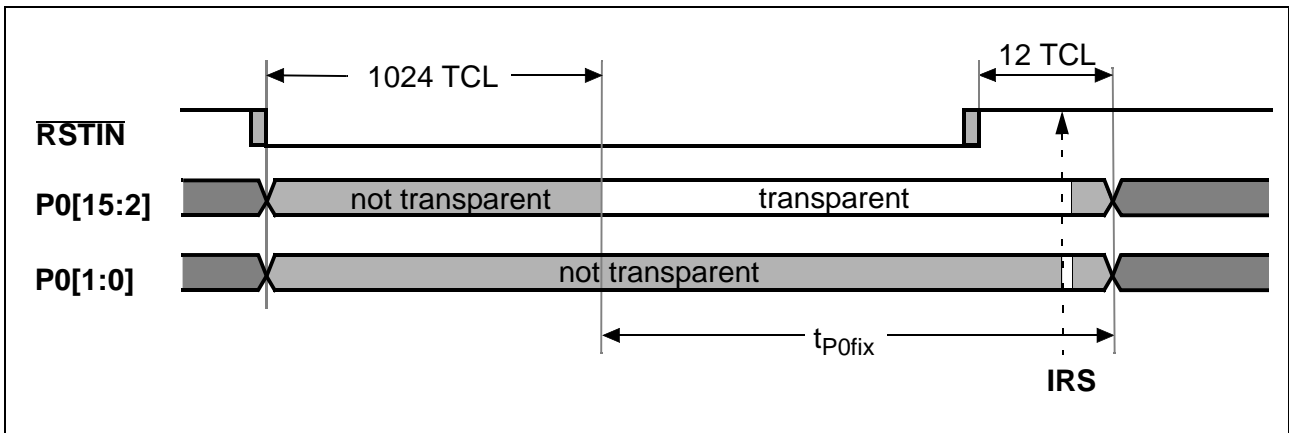
Figure 3 :
PORT0 sample Timing: Long Hardware Reset, Bidirectional Reset <u>enabled</u> or <u>disabled</u>
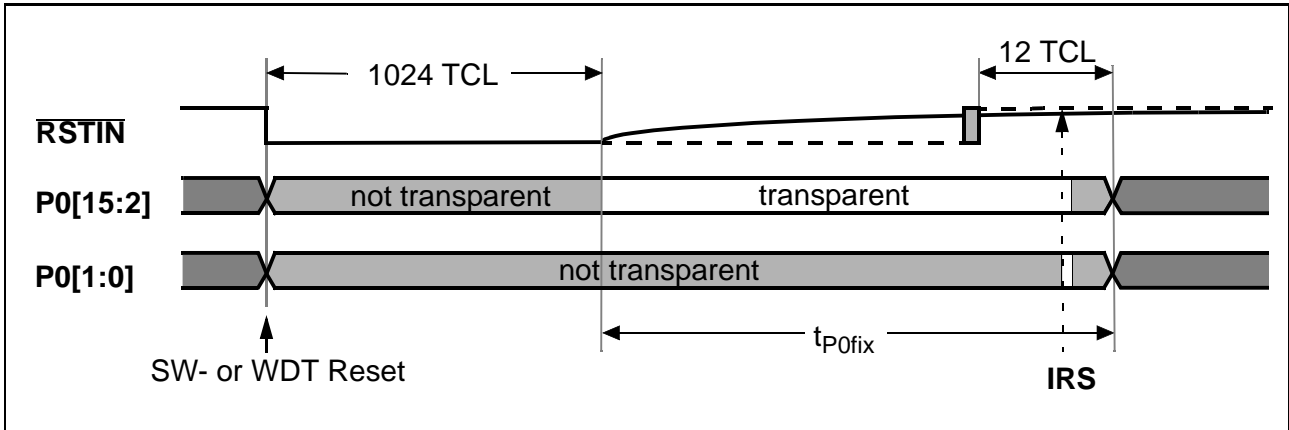

Figure 4 :
PORT0 sample Timing: Short Hardware Reset, Bidirectional Reset <u>disabled</u>
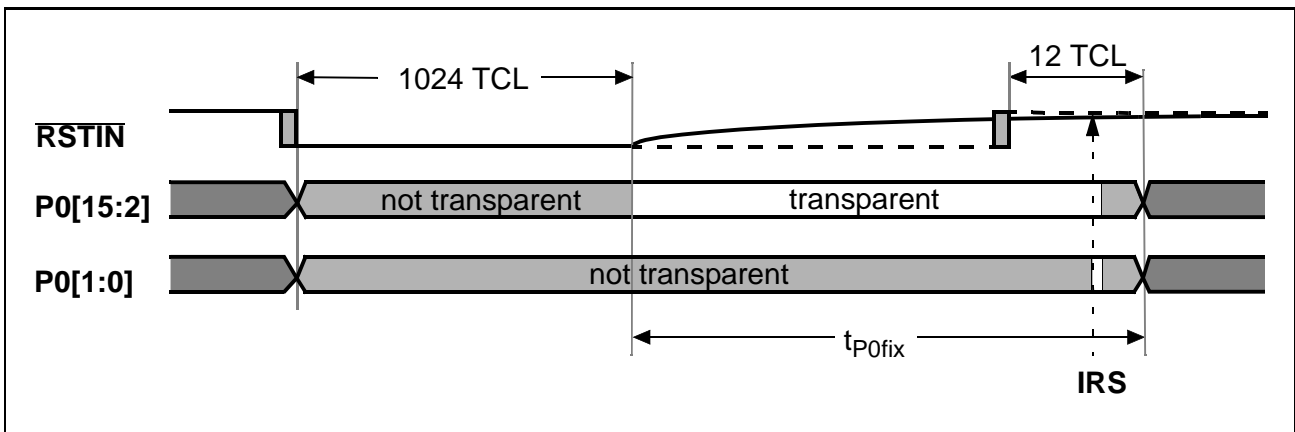

Figure 5 :
PORT0 sample Timing: Software Reset or WDT Reset, Bidirectional Reset <u>disabled</u>

Figure 6 :
PORT0 sample Timing: Software Reset and WDT Reset, Bidirectional Reset <u>enabled</u>

Figure 7 :
**PORT0 sample Timing: Short Hardware Reset, Bidirectional Reset <u>enabled</u>**

3 Calculation of the Pull-up/down Resistors at PORT0 for Startup Configuration

The specification in the Data Sheet includes the values of the PORT0 configuration currents I_{P0L} and I_{P0H}.

3.1 Pull-down Calculation

I_{P0L} is the base for the calculation of the Pull-down resistors for PORT0 startup configuration. $I_{P0Lmin} = -100 \, \mu A \ @ \, V_{IN} = V_{ILmax}$. That means that the port configuration current has to be more or equal than 100 µA to get an input voltage V_{IN} lower or equal to V_{ILmax}. The system current I_{SYSL} has a direct influence on the value of the needed pull-down resistor. The relation between the different parameters and the calculation with an example are shown below.

Note: All currents flowing into the microcontroller are defined as positive and all currents flowing out of it are defined as negative. Because of the internal pull-up transistor the direction of I_{P0L} and I_{P0H} is out of the device and therefore the sign in the current specification is negative.
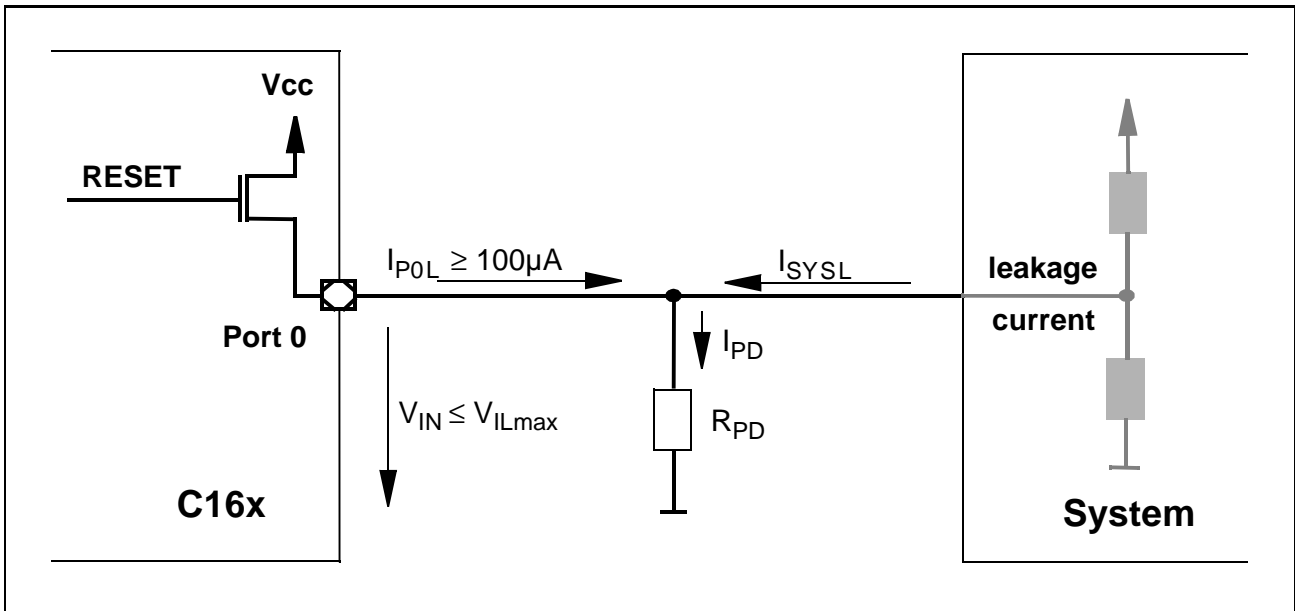
Figure 8 :
System Environment and Pull-down Resistor for Startup

Current Specification in the Data Sheet:

Vcc	= 5V ± 10%	⇒	4.5V	≤	Vcc	≤ 5.5V
V_{ILmax}	= 0.2Vcc - 0.1V	⇒	0.8V	≤	V_{ILmax}	≤ 1.0V
I_{P0Lmin}	= -100µA	⇒	I_{P0L}	≥	|-100µA|	

Pull-down resistor calculation:

$$R_{PD} < \frac{V_{ILmax}}{I_{PD}} = \frac{V_{ILmax}}{I_{P0L} + I_{SYSL}}$$

Example **without** system current:
($I_{SYSL} = 0$ A)

$$R_{PD} < \frac{V_{ILmax}}{I_{PD}} = \frac{0.8\ V}{100\mu A}$$

The recommended maximum value: $R_{PD} = 8\ k\Omega$

3.2   Pull-up Calculation

I_{P0H} is the base for the calculation of the pull-up resistors for PORT0 startup configuration.
$I_{P0Hmax} = -10\ \mu A$ @ $V_{IN} = V_{IHmin}$. As already mentioned PORT0 supplies internal pull-up resistors which are only active during Reset, or during Hold-or Adapt-mode. For normal systems this internal pull-up resistors are sufficient to reach the input high voltages at the PORT0 pins. This situation changes when the system current I_{SYSH} exceeds 10 μA. Then additional external pull-up resistors are mandatory. For example system flash memory with a high leakage current can cause an increased I_{SYSH}. The calculation and an example are shown below.
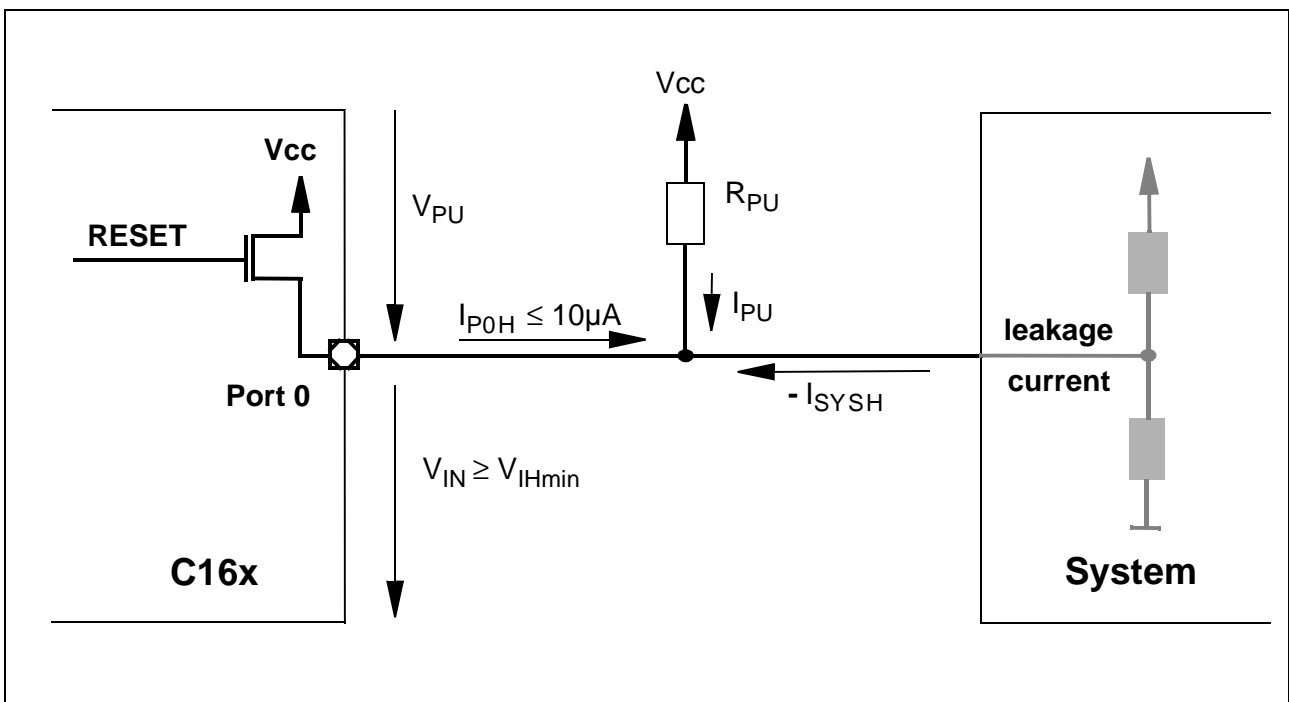
Figure 9 :
System Environment and Pull-up Resistor for Startup

Current Specification in the Data Sheet:

V_{cc} = 5 V ± 10 % ⇒ 4.5 V ≤ V_{cc} ≤ 5.5 V

V_{IHmin} = 0.2 V_{cc} + 0.9 V ⇒ 1.8 V ≤ V_{IHmin} ≤ 2.0 V

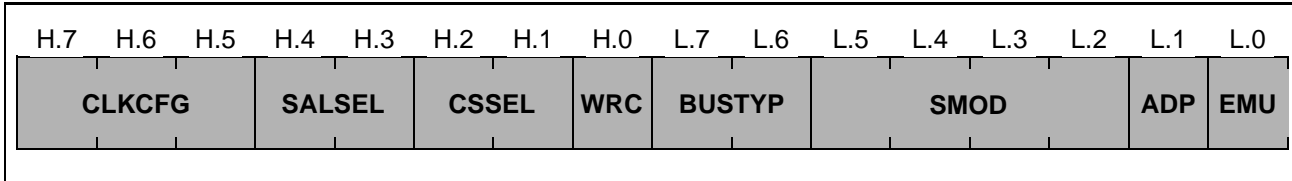I_{P0Hmax} = -10 µA ⇒ I_{P0H} ≤ |-10 µA|

Pull-up resistor calculation:

$$R_{PU} < \frac{V_{PU}}{I_{PU}} = \frac{V_{CCmin} - V_{IHmin}}{I_{SYSH} - I_{P0H}}$$

Example: I_{SYSH} = 50µA:

$$R_{PU} < \frac{4.5\,V - 1.8\,V}{50µA - 10µA} = 67.5\,k\Omega$$

The recommended maximum value: R_{PU} = 67.5 kΩ

4 Appendix
A PORT0 Configuration during Reset

H.7	H.6	H.5	H.4	H.3	H.2	H.1	H.0	L.7	L.6	L.5	L.4	L.3	L.2	L.1	L.0
CLKCFG			SALSEL		CSSEL		WRC	BUSTYP		SMOD				ADP	EMU

Pin	Mode	Comment
EMU	**Emulation Mode**	**Condition for EHM and Quality of P0H.7 is inverted**
ADP	**Adapt Mode**	
SMOD (P0L.5:2)	**Special Modes**	
0 0 0 0	Reserved	Do not use this combination
0 0 0 1	Reserved	Do not use this combination
0 0 1 0	Reserved	Do not use this combination
0 0 1 1	Reserved	Do not use this combination
0 1 0 0	Reserved	Do not use this combination
0 1 0 1	Reserved	Do not use this combination
0 1 1 0	Reserved	Do not use this combination
0 1 1 1	**External Host Mode (EHM)[1]**	**Requires Emulation Mode**
1 0 0 0	Reserved	Do not use this combination
1 0 0 1	Reserved	Do not use this combination
1 0 1 0	**Bootstrap Loader + CPU Host Mode[1]**	**Serial OTP programming via BSL**
1 0 1 1	**Bootstrap Loader**	**Start from internal boot ROM**
1 1 0 0	Reserved	Do not use this combination
1 1 0 1	Reserved	Do not use this combination
1 1 1 0	**CPU Host Mode (CHM)[1]**	**CPU programming mode for OTP**
1 1 1 1	**Normal Start**	**Normal start as defined by $\overline{EA}$ pin**

BUSTYP (P0L.7:6)	External Data Bus Width	External Address Bus Mode
0 0	8-bit Data	Demultiplexed Addresses
0 1	8-bit Data	Multiplexed Addresses
1 0	16-bit Data	Demultiplexed Addresses
1 1	16-bit Data	Multiplexed Addresses
WRC	**Write Configuration**	
CSSEL (P0H.2:1)	**Chip Select Lines**	
1 1	Max: $\overline{CSx}...\overline{CS0}$	Default without pull-downs
1 0	None	Port 6 pins free for IO
0 1	Two: $\overline{CS1}...\overline{CS0}$	
0 0	Three: $\overline{CS2}...\overline{CS0}$	
SALSEL (P0H.4:3)	**Segment Address Lines**	**Directly accessible Address Space**
1 1	Two: A17...A16	256 KByte (Default, without pull-downs)
1 0	Axx...A16	(Maximum)
0 1	None	64 KByte (Minimum)
0 0	Four: A19...A16	1 MByte
CLKCFG (P0H.7-5)	**CPU Frequency $f_{CPU} = f_{XTAL} * F$**	**Notes[2]**
1 1 1	$f_{XTAL} * 4$	Default configuration
1 1 0	$f_{XTAL} * 3$	
1 0 1	$f_{XTAL} * 2$	
1 0 0	$f_{XTAL} * 5$	
0 1 1	$f_{XTAL} * 1$	Direct drive
0 1 0	$f_{XTAL} * 1.5$	
0 0 1	$f_{XTAL} / 2$	Prescaler
0 0 0	$f_{XTAL} * 2.5$	

[1] This modes are only valid for C161CI, C164CI and C167CS

[2] The clock configuration bits are not fully decoded in all devices and steps. Please use Appendix B and the User's Manuals for detailed information.

B   Clock Options and Steps

Device	Step[1]	OWD[2]	PM[3]	Clock Options [4]	PLL Factors (F)
SAx-C161V / K / O	AA	==	no	0.5 / 1	no
SAx-C161RI	AA, BA, BB	==	yes	0.5 / 1	no
SAx-C161SI / CI	AA	$\overline{RD}$	yes	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
SAx-C163	AA, AB, BA, BB	V_{PP}/OWE	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
SAx-C163-16F	AA, AB	V_{PP}/OWE	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
SAx-C163-16F x	BA, BB	==	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
SAx-C164CI	AA	$\overline{RD}$	yes	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
SAx-C165	BB	==	no	0.5	no
SAx-C165	CA	==	no	0.5 / 1	no
SAx-C167-LM	BA, BB, CA, CB, BE	==	no	0.5	no
SAx-C167SR-LM	AB	==	no	1 / PLL	4
SAx-C167SR-LM	BA	==	no	1 / PLL	2/3/4/5
SAx-C167SR-LM		==	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
SAx-C167CR-LM	AB	==	no	1 / PLL	4
SAx-C167CR-LM	BA, BB, CA, CB, BE	==	no	1 / PLL	2/3/4/5
SAx-C167S-4RM	AA,BA, BB	V_{PP}	no	1 / PLL	2/3/4/5
SAx-C167CR-4RM	AA, AB, AC	V_{PP}	no	0.5 / 1 / PLL	1.5/2/2.5/3/4/5
SAx-C167CR-16RM	AA	==	no	1 / PLL	2/3/4/5
SAx-C167CR-16FM	AC	==	no	1 / PLL	4
SAx-C167CS-32FM	AA	$\overline{RD}$	yes	0.5 / 1 / PLL	1.5/2/2.5/3/4/5

[1] The described options are implemented since the steps listed below.

[2] The Oscillator Watchdog (OWD) can be disabled in different kinds.

==   : No OWD implemented.

V_{PP}/OWE   : A low level on pin V_{PP}/OWE disables the OWD.

$\overline{RD}$: A low level on pin $\overline{RD}$ at the end of any type of reset disables the OWD.
               The level of $\overline{RD}$ is latched with the IRS. See figure 2 to figure 7.

V_{PP} : A low level on pin V_{PP} disables the OWD.

[3] Besides other features the Power Management (PM) includes the Slow Down Devider. A separate clock path can be selected for Slow Down operation bypassing the basic clock path used for standard operation. The programmable Slow Down Devider devides the oscillator frequency by a factor of 1 ... 32.

[4] Prescaler option   : 0.5
   Direct drive option   : 1
   The PLL clock is not used for prescaler option $(f_{CPU} = f_{OSC} * 0.5)$
   and direct drive option $(f_{CPU} = f_{OSC} * 1.0).$