

DATA SHEET

74ALS620A/74ALS620A-1
74ALS623A/74ALS623A-1
Transceivers

Product specification
IC05 Data Handbook

1991 Feb 08

Transceivers

74ALS620A/74ALS620A-1 74ALS623A/74ALS623A-1

74ALS620A/74ALS620A-1 Octal bus transceiver, inverting (3-State)
74ALS623A/74ALS623A-1 Octal bus transceiver, non-inverting (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs sink 24mA and source 15mA
- The -1 version sinks 48mA I_{OL} within the +5% V_{CC} range

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS620A/620A-1	4.0ns	33mA
74ALS623A/623A-1	4.0ns	38mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$	
20-pin plastic DIP	74ALS620AN, 74ALS620A-1N 74ALS623AN, 74ALS623A-1N	SOT146-1
20-pin plastic SOL	74ALS620AD, 74ALS620A-1D 74ALS623AD, 74ALS623A-1D	SOT163-1

DESCRIPTION

The 74ALS620A and 74ALS623A are octal transceiver featuring 3-State bus compatible outputs in both transmit and receive directions. The 74ALS620A is an inverting version of the 74ALS623A. The outputs are capable of sinking 24mA and sourcing up to 15mA, providing very good capacitive drive characteristics.

The outputs for the 74ALS620A-1 and 74ALS623A are capable of sinking up to 48mA when within the $\pm 5\%$ V_{CC} range.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

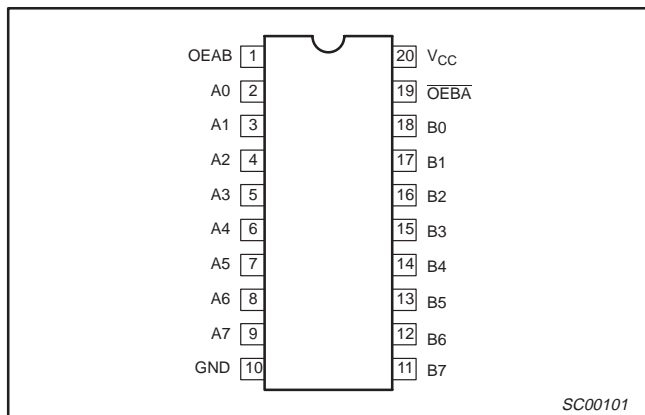
These devices allow data transmission from the A bus to the B bus or from B bus to A bus, depending on the logic levels at the enable inputs (\overline{OEBA} and OEAB). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the 74ALS620A and 74ALS623A the capability to store data by the simultaneous enabling of \overline{OEBA} and OEAB. Each output reinforces its input in this transceiver configuration. Thus when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of the bus lines (16 in all) will remain at their last states.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

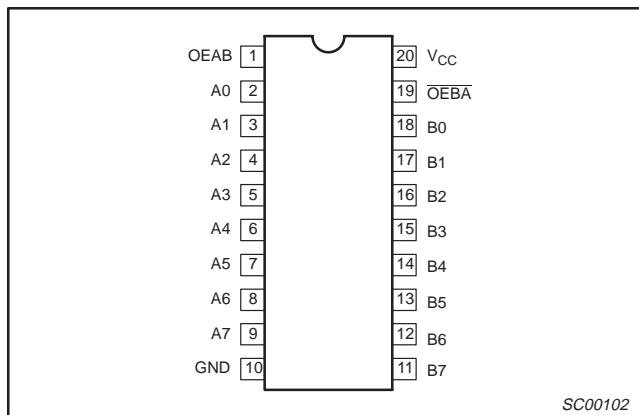
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7, B0 – B7	Data inputs	1.0/1.0	20 μ A/0.1mA
\overline{OEBA} , OEAB	Output Enable inputs	1.0/1.0	20 μ A/0.1mA
A0 – A7, B0 – B7	Data outputs	750/240	15mA/24mA
A0 – A7, B0 – B7	Data outputs (-1 version)	750/480	15mA/48mA

NOTE: One (1.0) ALS unit load is defined as: 20 μ A in the High state and 0.1mA in the Low state.

PIN CONFIGURATION – 74ALS620A/74ALS620A-1



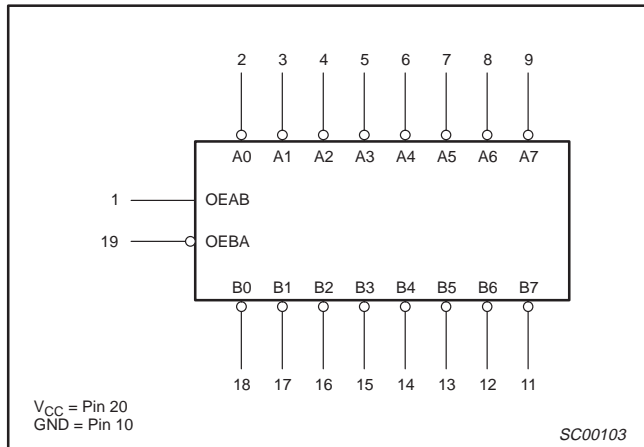
PIN CONFIGURATION – 74ALS623A/74ALS623A-1



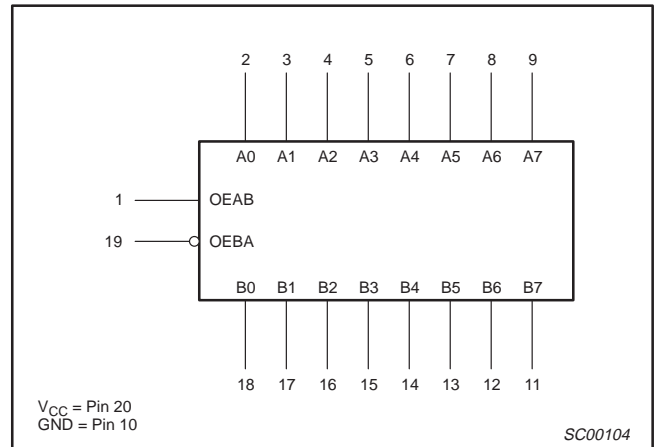
Transceivers

74ALS620A/74ALS620A-1 74ALS623A/74ALS623A-1

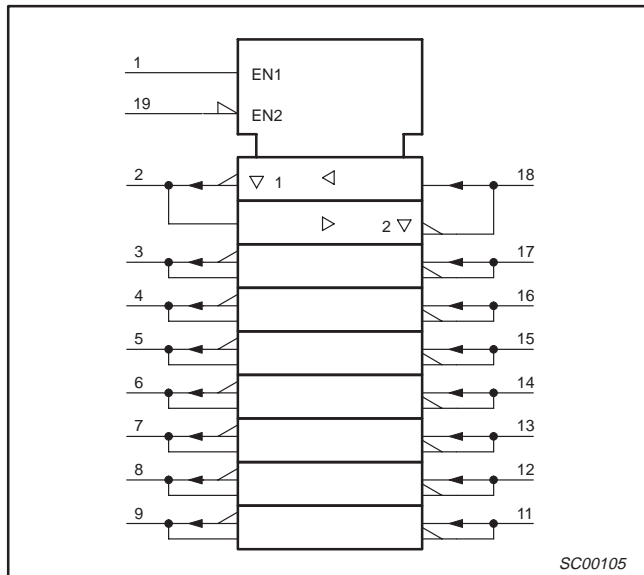
LOGIC SYMBOL – 74ALS620A/74ALS620A-1



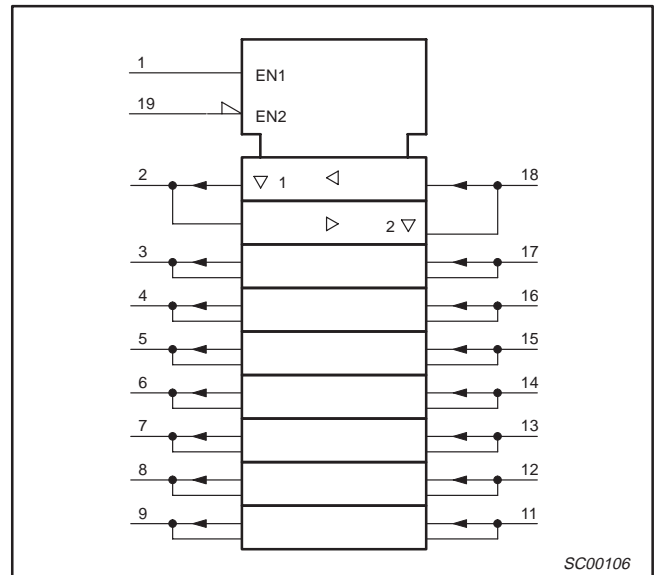
LOGIC SYMBOL – 74ALS623A/74ALS623A-1



IEC/IEEE SYMBOL – 74ALS620A/74ALS620A-1



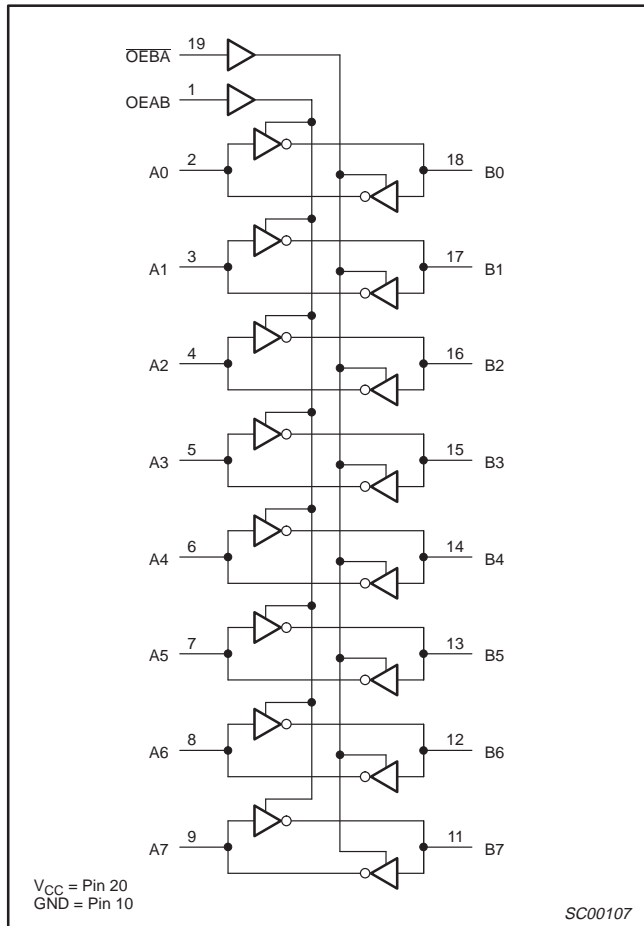
IEC/IEEE SYMBOL – 74ALS623A/74ALS623A-1



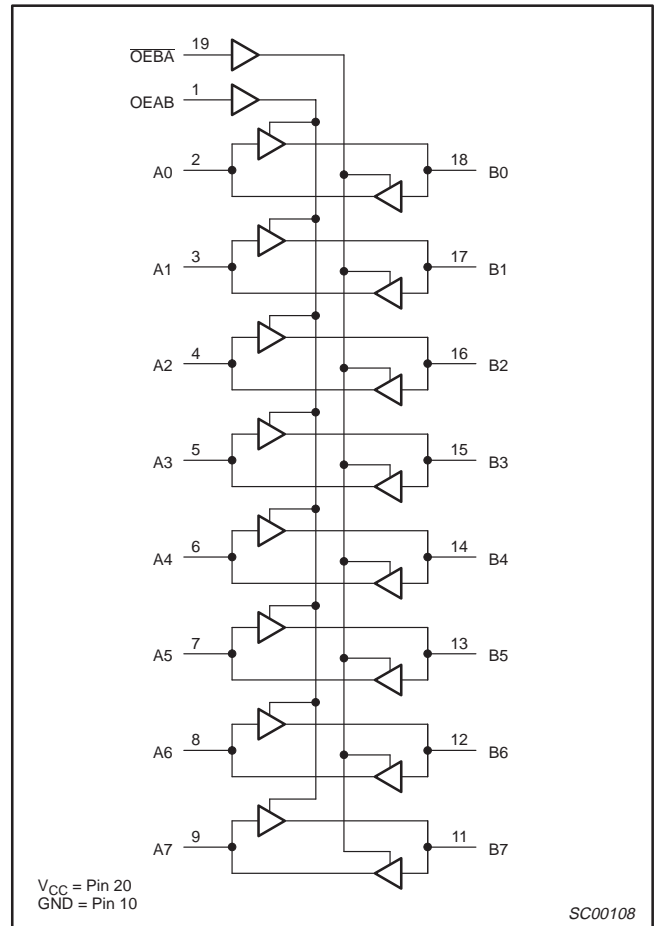
Transceivers

74ALS620A/74ALS620A-1
74ALS623A/74ALS623A-1

LOGIC DIAGRAM – 74ALS620A/74ALS620A-1



LOGIC DIAGRAM – 74ALS623A/74ALS623A-1



FUNCTION TABLE

INPUTS		OPERATING MODES	
OEBA-bar	OEAB	74ALS620A	74ALS623A
L	L	B-bar data to A Bus	B data to A Bus
L	H	A-bar data to B Bus	A data to B Bus
H	L	Z	Z
L	H	B-bar data to A Bus	B data to A Bus
L	H	A-bar data to B Bus	A data to B Bus

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Transceivers

74ALS620A/74ALS620A-1
74ALS623A/74ALS623A-1**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		-0.5 to +7.0	V
V _{IN}	Input voltage		-0.5 to +7.0	V
I _{IN}	Input current		-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state		-0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version	96	mA
T _{amb}	Operating free-air temperature range		0 to +70	°C
T _{stg}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-15	mA
I _{OL}	Low-level output current	All versions		24	mA
		-1 version		48 ¹	mA
T _{amb}	Operating free-air temperature range	0		+70	°C

NOTE:

1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ±5%.

Transceivers

74ALS620A/74ALS620A-1
74ALS623A/74ALS623A-1**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹		LIMITS			UNIT
					MIN	TYP ²	MAX	
V _{OH}	High-level output voltage		V _{CC} = ±10%, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -0.4mA	V _{CC} - 2			V
				I _{OH} = -3mA	2.4	3.2		V
			V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -15mA	2.0			V
V _{OL}	Low-level output voltage	All versions	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 12mA		0.25	0.40	V
				I _{OL} = 24mA		0.35	0.50	V
		-1 versions	V _{CC} = 4.75V, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 48mA		0.35	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.5	V
I _I	Input current at maximum input voltage	OEBA or OEAB	V _{CC} = MAX, V _I = 7.0V				0.1	mA
		A or B ports	V _{CC} = MAX, V _I = 5.5V				0.1	mA
I _{IH}	High-level input current ³		V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	Low-level input current ³		V _{CC} = MAX, V _I = 0.4V				-0.1	mA
I _O	Output current ⁴		V _{CC} = MAX, V _O = 2.25V		-30		-112	mA
I _{CC}	Supply current (total)	74ALS620A 74ALS620A-1	I _{CCH}	V _{CC} = MAX		24	34	mA
			I _{CCL}			42	49	mA
			I _{CCZ}			45	52	mA
		74ALS623A 74ALS623A-1	I _{CCH}			24	43	mA
			I _{CCL}			41	50	mA
			I _{CCZ}			46	55	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- For I/O ports, the parameter I_{IH} and I_{IL} include the off-state current.
- The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Transceivers

74ALS620A/74ALS620A-1
74ALS623A/74ALS623A-1

AC ELECTRICAL CHARACTERISTICS FOR 74ALS620A/74ALS620A-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 1	2.0 2.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{\text{OEBA}}$ to An	Waveform 3 Waveform 4	2.0 3.0	17.0 25.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{\text{OEBA}}$ to An	Waveform 3 Waveform 4	2.0 2.0	12.0 18.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	Waveform 3 Waveform 4	2.0 3.0	18.0 25.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	Waveform 3 Waveform 4	2.0 3.0	12.0 18.0	ns

AC ELECTRICAL CHARACTERISTICS FOR 74ALS623A/74ALS623A-1

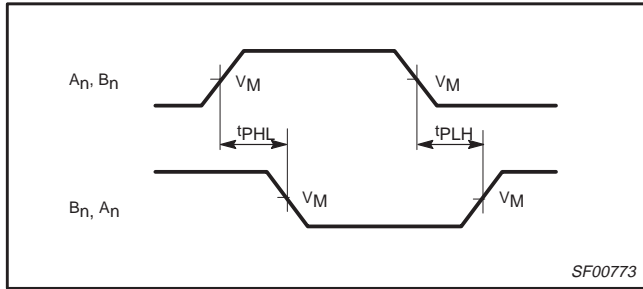
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 2	2.0 2.0	13.0 11.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{\text{OEBA}}$ to An	Waveform 3 Waveform 4	2.0 3.0	22.0 22.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{\text{OEBA}}$ to An	Waveform 3 Waveform 4	2.0 2.0	16.0 19.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	Waveform 3 Waveform 4	2.0 3.0	22.0 22.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	Waveform 3 Waveform 4	2.0 2.0	16.0 19.0	ns

Transceivers

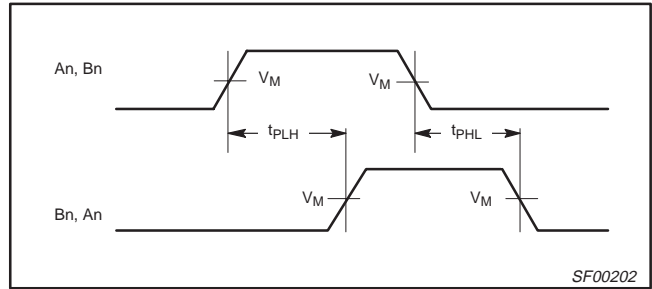
74ALS620A/74ALS620A-1 74ALS623A/74ALS623A-1

AC WAVEFORMS

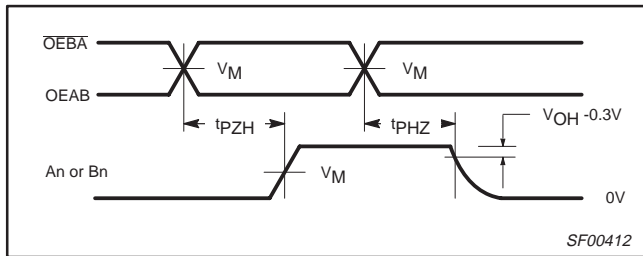
For all waveforms, $V_M = 1.3V$.



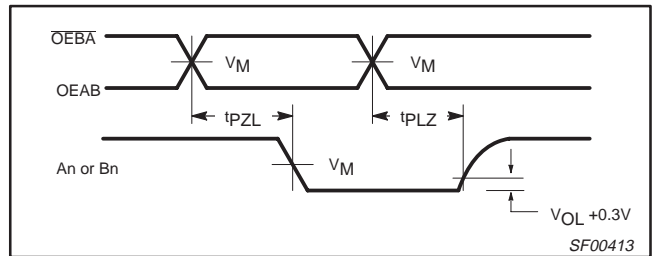
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-inverting Outputs



Waveform 3. 3-State Output Enable Time to High Level and Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:
 R_L = Load resistor; see AC electrical characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

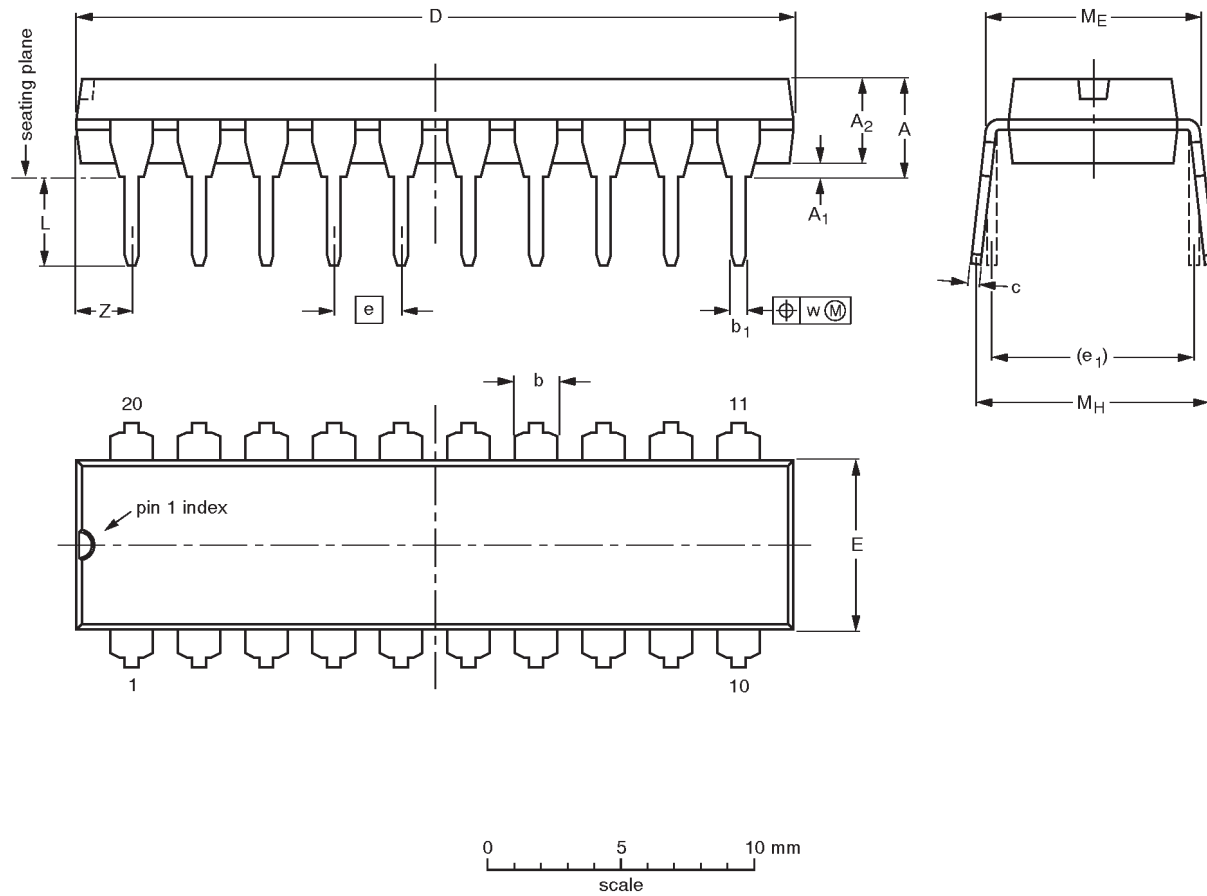
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Transceivers

74ALS620A/74ALS620A-1
74ALS623A/74ALS623A-1

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

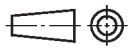


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

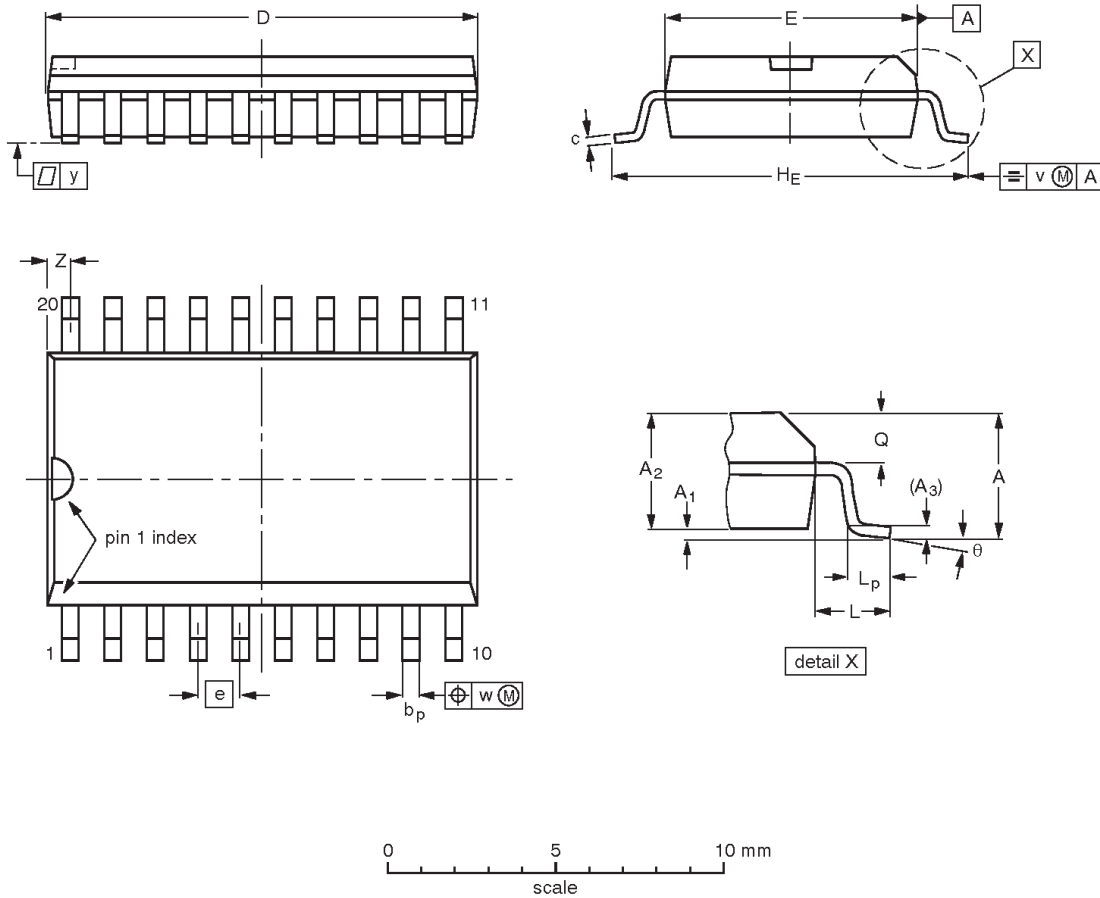
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

Transceivers

74ALS620A/74ALS620A-1
74ALS623A/74ALS623A-1

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

Transceivers

74ALS620A/74ALS620A-1
74ALS623A/74ALS623A-1

DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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