

## MOS FIELD EFFECT TRANSISTOR

## 2SK3481

### **SWITCHING** N-CHANNEL POWER MOS FET

#### **DESCRIPTION**

The 2SK3481 is N-channel MOS Field Effect Transistor designed for high current switching applications.

#### **FEATURES**

• Super low on-state resistance:

RDS(on)1 =  $50 \text{ m}\Omega$  MAX. (VGS = 10 V, ID = 15 A) RDS(on)2 =  $58 \text{ m}\Omega$  MAX. (VGS = 4.5 V, ID = 15 A)

- Low Ciss: Ciss = 2300 pF TYP.
- Built-in gate protection diode

#### ORDERING INFORMATION

| PART NUMBER | PACKAGE                   |
|-------------|---------------------------|
| 2SK3481     | TO-220AB                  |
| 2SK3481-S   | TO-262                    |
| 2SK3481-ZJ  | TO-263                    |
| 2SK3481-Z   | TO-220SMD <sup>Note</sup> |

Note TO-220SMD package is produced only in Japan.

(TO-220AB)

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

| Drain to Source Voltage (Vgs = 0 V)             | VDSS            | 100         | V  |
|---|-----------------|-------------|----|
| Gate to Source Voltage (Vps = 0 V)              | Vgss            | ±20         | V  |
| Drain Current (DC) (Tc = 25°C)                  | ID(DC)          | ±30         | Α  |
| Drain Current (pulse) Note1                     | ID(pulse)       | ±60         | Α  |
| Total Power Dissipation (Tc = 25°C)             | P <sub>T1</sub> | 56          | W  |
| Total Power Dissipation (T <sub>A</sub> = 25°C) | P <sub>T2</sub> | 1.5         | W  |
| Channel Temperature                             | Tch             | 150         | °C |
| Storage Temperature                             | Tstg            | -55 to +150 | °C |
| Single Avalanche Current Note2                  | las             | 26          | Α  |
| Single Avalanche Energy Note2                   | Eas             | 68          | mJ |

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty cycle  $\leq$  1%

**2.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V



(TO-262)



(TO-263, TO-220SMD)



#### THERMAL RESISTANCE

Channel to Case Thermal Resistance 2.23 °C/W  $R_{th(ch-C)}$ Channel to Ambient Thermal Resistance 83.3 °C/W Rth(ch-A)

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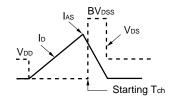


#### **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

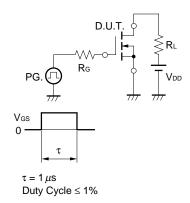
| CHARACTERISTICS                     | SYMBOL               | TEST CONDITIONS                                | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|----------------------|--|------|------|------|------|
| Zero Gate Voltage Drain Current     | IDSS                 | V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V |      |      | 10   | μΑ   |
| Gate Leakage Current                | Igss                 | Vgs = ±20 V, Vps = 0 V                         |      |      | ±10  | μΑ   |
| Gate Cut-off Voltage                | V <sub>GS(off)</sub> | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA  | 1.5  | 2.0  | 2.5  | V    |
| Forward Transfer Admittance         | yfs                  | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A  | 9    | 18   |      | S    |
| Drain to Source On-state Resistance | RDS(on)1             | Vgs = 10 V, ID = 15 A                          |      | 40   | 50   | mΩ   |
|                                     | RDS(on)2             | Vgs = 4.5 V, ID = 15 A                         |      | 44   | 58   | mΩ   |
| Input Capacitance                   | Ciss                 | V <sub>DS</sub> = 10 V                         |      | 2300 |      | pF   |
| Output Capacitance                  | Coss                 | Vgs = 0 V                                      |      | 230  |      | pF   |
| Reverse Transfer Capacitance        | Crss                 | f = 1 MHz                                      |      | 120  |      | pF   |
| Turn-on Delay Time                  | td(on)               | V <sub>DD</sub> = 50 V, I <sub>D</sub> = 15 A  |      | 13   |      | ns   |
| Rise Time                           | <b>t</b> r           | Vgs = 10 V                                     |      | 10   |      | ns   |
| Turn-off Delay Time                 | td(off)              | $R_G = 0 \Omega$                               |      | 53   |      | ns   |
| Fall Time                           | <b>t</b> f           |  |      | 5.0  |      | ns   |
| Total Gate Charge                   | QG                   | VDD = 80 V                                     |      | 48   |      | nC   |
| Gate to Source Charge               | Qgs                  | Vgs = 10 V                                     |      | 7.0  |      | nC   |
| Gate to Drain Charge                | QGD                  | ID = 30 A                                      |      | 12   |      | nC   |
| Body Diode Forward Voltage          | V <sub>F(S-D)</sub>  | IF = 30 A, VGS = 0 V                           |      | 1.0  |      | V    |
| Reverse Recovery Time               | trr                  | IF = 30 A, VGS = 0 V                           |      | 70   |      | ns   |
| Reverse Recovery Charge             | Qrr                  | di/dt = 100 A/ μs                              |      | 160  |      | nC   |

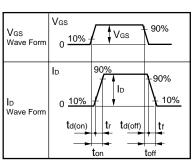
#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $\begin{array}{c|c} \text{D.U.T.} \\ \text{RG} = 25 \ \Omega \\ \text{PG.} \\ \hline \\ \text{VGS} = 20 \rightarrow 0 \ V \\ \end{array} \begin{array}{c} \text{D.U.T.} \\ \\ \text{VDD} \\ \end{array}$

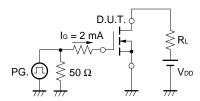


#### **TEST CIRCUIT 2 SWITCHING TIME**



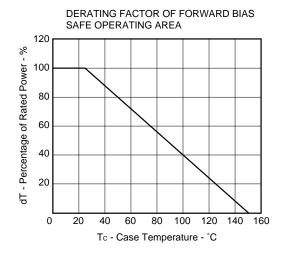


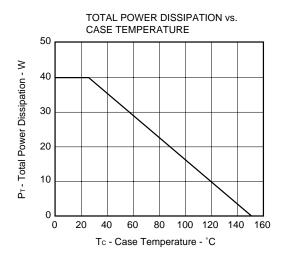
#### **TEST CIRCUIT 3 GATE CHARGE**



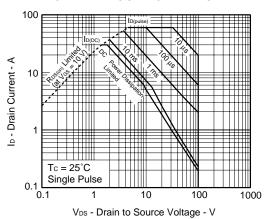


#### TYPICAL CHARACTERISTICS (TA = 25°C)

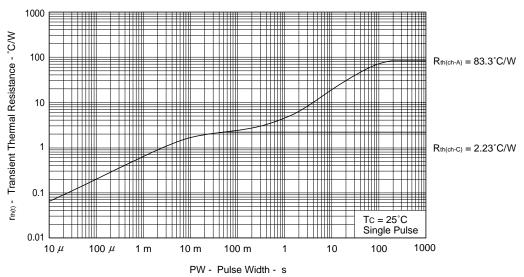




#### FORWARD BIAS SAFE OPERATING AREA





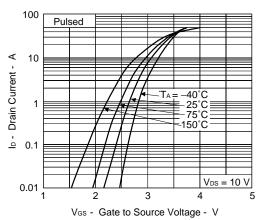


Data Sheet D15063EJ1V0DS

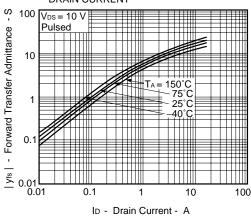
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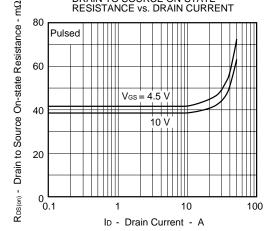
#### FORWARD TRANSFER CHARACTERISTICS



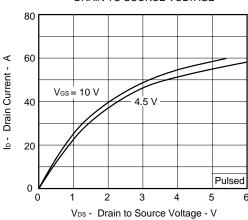
## FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



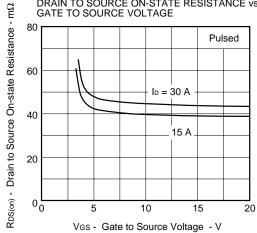
## DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

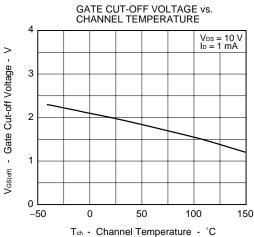


## DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

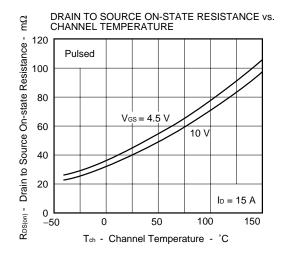


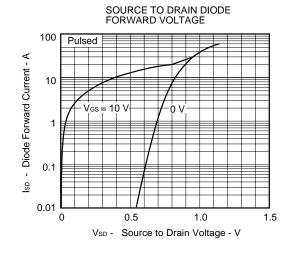
## DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

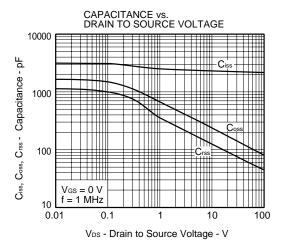


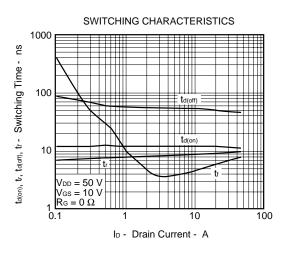


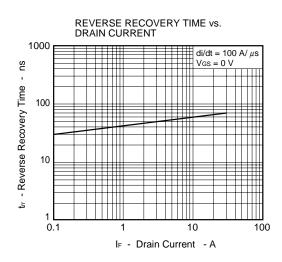


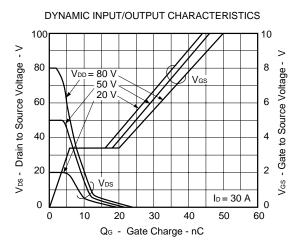




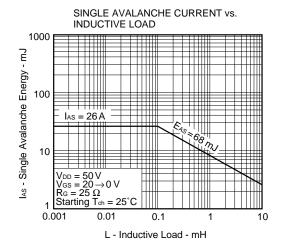


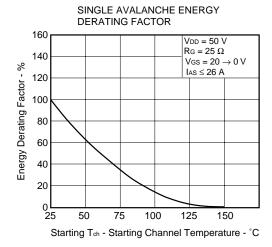






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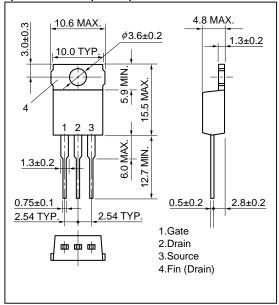




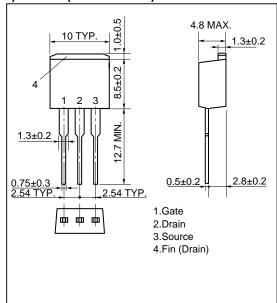


#### PACKAGE DRAWINGS (Unit: mm)

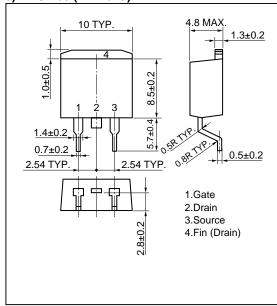
#### 1) TO-220AB (MP-25)



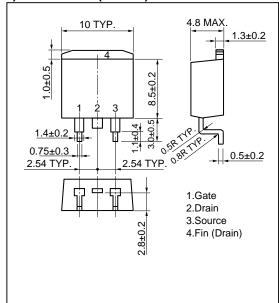
#### 2) TO-262 (MP-25 Fin Cut)



#### 3) TO-263 (MP-25ZJ)

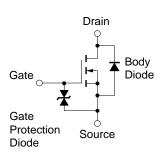


4) TO-220SMD (MP-25Z)<sup>Note</sup>



Note This package is produced only in Japan.

#### **EQUIVALENT CIRCUIT**



#### Remark

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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