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Status	Product Specification
ECL Products	

10129
Line Receiver

Quad TTL-to-ECL Translator

FEATURES

- **Typical propagation delay: 10.0ns**
- **Typical TTL supply current (I_{CC}): 3.0mA**
- **Typical ECL supply current ($-I_{EE}$): 144mA**

DESCRIPTION

The 10129 is intended to allow interfacing of 10K family types with other logic devices or systems. The enable, reset and strobe inputs are compatible with 10K family logic levels whereas data inputs accept TTL logic levels compatible with IBM-type busses. The information received from the bus is stored temporarily in latch storage elements.

The strobe input is useful to provide accurate synchronization of signals and/or connection to 10K family type level busses. When the enable is Low, the reset input is disabled and the outputs will follow the data inputs. The latches store data when the enable goes High. Unused data inputs must be tied to V_{CC} or ground. On the other hand, enable, strobe and reset inputs must be tied to V_{IL} or V_{EE} if unused.

The outputs are enabled when the strobe input is High. Two modes of operation are provided. In the first mode, obtained by tying the hysteresis control input to V_{EE}, the input threshold points of the D inputs are fixed. In the second mode this hysteresis control input is connected to ground which gives an hysteresis input effect useful for increasing the D input noise margin.

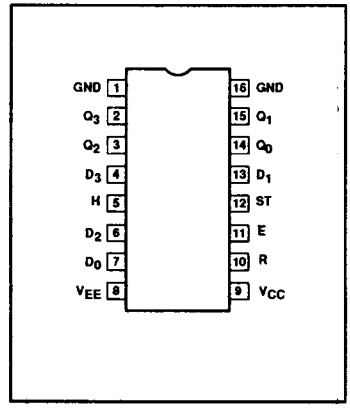
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10129N
16–Pin Ceramic DIP	10129F

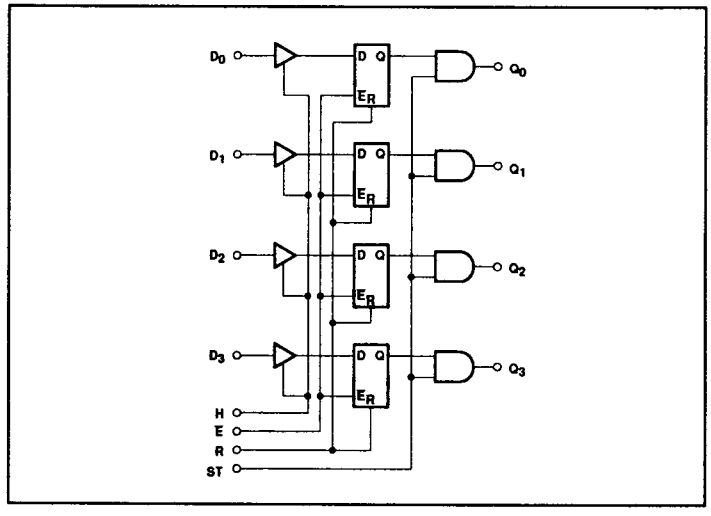
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
H	Hysteresis control Input
$\overline{E}$	Enable Input
R	Reset Input
ST	Strobe Input
$Q_1 - Q_3$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
D_n	$\overline{E}$	ST	R	$\overline{Q}_{n+1}$
X	X	L	X	L
X	H	X	H	L
L	L	H	X	H
X	H	H	L	Q_n
H	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS FOR ECL–COMPATIBLE LINES

SYMBOL	PARAMETER		LIMIT	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

ABSOLUTE MAXIMUM RATINGS FOR TTL–COMPATIBLE LINES

SYMBOL	PARAMETER	LIMIT	UNIT
V_{CC}	TTL supply voltage	–5.0 to +7.0	V
V_{IN}	Input voltage	–0.5 to V_{TTL}	V
I_{IN}	Input current	–30 to +5	mA

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS FOR ALL INPUT LEVELS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	NOM.	MAX.	
GND	Circuit ground	0	0	0	V
V_{EE}	ECL supply voltage		–5.2		V
V_{CC}	TTL supply voltage		+5.0		V
T_A	Operating ambient temperature range	–30	+25	+85	°C

NOTE:
When operating at V_{EE} other than specified voltage (–5.2V), the DC and AC Characteristics will vary slighly from specified values. (See table of DC Characteristics.)

DC OPERATING CONDITIONS FOR ECL INPUT LEVELS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{IH}	High level input voltage	$T_A = -30°C$			-890	mV
		$T_A = +25°C$			-810	mV
		$T_A = +85°C$			-700	mV
V_{IHT}	High level input threshold voltage	$T_A = -30°C$	-1205			mV
		$T_A = +25°C$	-1105			mV
		$T_A = +85°C$	-1035			mV
V_{ILT}	Low level input threshold voltage	$T_A = -30°C$			-1500	mV
		$T_A = +25°C$			-1475	mV
		$T_A = +85°C$			-1440	mV
V_{IL}	Low level input voltage	$T_A = -30°C$	-1890			mV
		$T_A = +25°C$	-1850			mV
		$T_A = +85°C$	-1825			mV

DC OPERATING CONDITIONS FOR TTL INPUT LEVELS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{IH}	High level input voltage	$T_A = -30°C$	3.000			V
		$T_A = +25°C$	3.000			V
		$T_A = +85°C$	3.000			V
V_{IHT}'	High level input threshold voltage	$T_A = -30°C$	2.000			V
		$T_A = +25°C$	2.000			V
		$T_A = +85°C$	2.000			V
V_{ILT}'	Low level input threshold voltage	$T_A = -30°C$			0.800	V
		$T_A = +25°C$			0.800	V
		$T_A = +85°C$			0.800	V
V_{IL}	Low level input voltage	$T_A = -30°C$			0.400	V
		$T_A = +25°C$			0.400	V
		$T_A = +85°C$			0.400	V

DC OPERATING CONDITIONS FOR IBM INPUT LEVELS

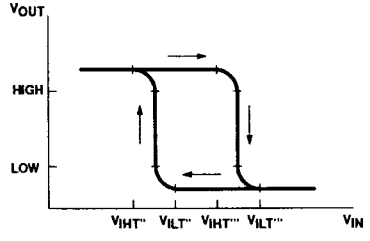
SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{IH}	High level input voltage	$T_A = -30°C$	3.110			V
		$T_A = +25°C$	3.110			V
		$T_A = +85°C$	3.110			V
V_{IHT}'	High level input threshold voltage	$T_A = -30°C$				V
		$T_A = +25°C$	1.700			V
		$T_A = +85°C$				V
V_{ILT}'	Low level input threshold voltage	$T_A = -30°C$				V
		$T_A = +25°C$			0.700	V
		$T_A = +85°C$				V
V_{IL}	Low level input voltage	$T_A = -30°C$			0.150	V
		$T_A = +25°C$			0.150	V
		$T_A = +85°C$			0.150	V

DC OPERATING CONDITIONS FOR HYSTERESIS MODE THRESHOLD VOLTAGES

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{IHT}''	Hysteresis mode High level input threshold voltage	$T_A = -30°C$	2.900			V
		$T_A = +25°C$	2.600			V
		$T_A = +85°C$	2.300			V
V_{ILT}''	Hysteresis mode Low level input threshold voltage	$T_A = -30°C$			2.000	V
		$T_A = +25°C$			1.700	V
		$T_A = +85°C$			1.400	V
V_{IHT}'''	Hysteresis mode High level input threshold voltage	$T_A = -30°C$	2.200			V
		$T_A = +25°C$	1.900			V
		$T_A = +85°C$	1.600			V
V_{ILT}'''	Hysteresis mode Low level input threshold voltage	$T_A = -30°C$			1.300	V
		$T_A = +25°C$			1.000	V
		$T_A = +85°C$			0.700	V

NOTE:
V_{IH}'', V_{IL}'', V_{IH}''' and V_{IL}''' are logic "1" and "0" threshold voltages in the hystersis mode.

HYSTERSIS MODE THRESHOLD VOLTAGES



DC ELECTRICAL CHARACTERISTICS

GND = ground, V_{EE} = –5.2V ± 0.010V, V_{CC} = +5.0V ± 0.010V, T_A = –30°C to +85°C output loading 50Ω to –2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		T_A = –30°C	ST = V_{IHMAX}, $\overline{E}$ = V_{ILMIN}, R = V_{ILMIN}	–1060		–890	mV
			T_A = +25°C		–960		–810	mV
			T_A = +85°C		–890		–700	mV
V_{OHT}	High level output threshold voltage		T_A = –30°C	ST = V_{IHMAX}, $\overline{E}$ = V_{ILMIN}, R = V_{ILMIN}	–1080			mV
			T_A = +25°C		–980			mV
			T_A = +85°C		–910			mV
V_{OLT}	Low level output threshold voltage		T_A = –30°C	ST = V_{IHMAX}, $\overline{E}$ = V_{ILMIN}, R = V_{ILMIN}			–1655	mV
			T_A = +25°C				–1630	mV
			T_A = +85°C				–1595	mV
V_{OL}	Low level output voltage		T_A = –30°C	ST = V_{IHMAX}, $\overline{E}$ = V_{ILMIN}, R = V_{ILMIN}	–1890		–1675	mV
			T_A = +25°C		–1850		–1650	mV
			T_A = +85°C		–1825		–1615	mV
I_{IH}	High level input current	D_n inputs	T_A = –30°C				150	µA
			T_A = +25°C				95	µA
			T_A = +85°C				95	µA
		R input	T_A = –30°C	$\overline{E}$ = R = V_{ILMAX}			720	µA
			T_A = +25°C				450	µA
			T_A = +85°C				450	µA
		$\overline{E}$, ST inputs	T_A = –30°C	$\overline{E}$ or ST = V_{IHMAX}			390	µA
			T_A = +25°C				245	µA
			T_A = +85°C				245	µA
$-I_{CBO}$	Input leakage current	D_n inputs	T_A = –30°C	Apply V_{EE} to H one D_n = V_{IL} (TTL or IBM) at a time.			1.5	µA
			T_A = +25°C				1.0	µA
			T_A = +85°C				1.0	µA
I_{IL}	Low level input current	R, $\overline{E}$, ST inputs	T_A = –30°C		0.5			µA
			T_A = +25°C		0.5			µA
			T_A = +85°C		0.3			µA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
$-I_{EE}$	ECL supply current	T_A = –30°C	Connect H to GND			167	mA
		T_A = +25°C	ST = V_{IHMIN}, $\overline{E}$ = V_{ILMIN}			152	mA
		T_A = +85°C				167	mA
		T_A = –30°C	Apply V_{EE} to H			189	mA
		T_A = +25°C	ST = V_{IHMIN}, $\overline{E}$ = V_{ILMIN}			172	mA
		T_A = +85°C				189	mA
I_{CC}	TTL supply current	T_A = –30°C	Apply V_{EE} to H			8.0	mA
		T_A = +25°C				8.0	mA
		T_A = +85°C				8.0	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	T_A = +25°C			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

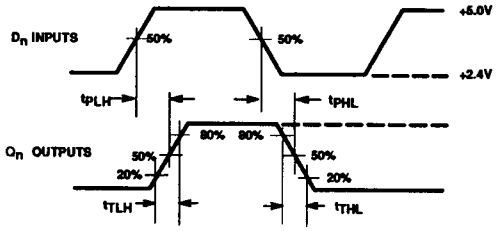
NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS GND = ground, V_{EE} = –5.2V ± 0.010V, V_{CC} = +5.0V ± 0.010V

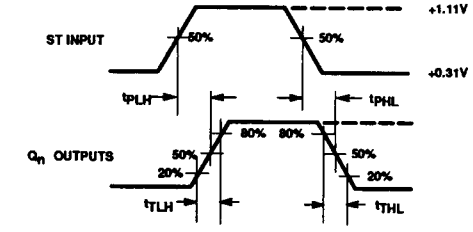
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = –30°C MIN.	LIMITS T_A = –30°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C TYP.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH}	Propagation delay without Hysteresis, D_n to Q_n	Connect H to V_{EE}, Waveform 1	3.7	15	3.7	10.0	15	3.7	30	ns
t_{PHL}			3.7	15	3.7	10.0	15	3.7	40	ns
t_{PLH}	Propagation delay with Hysteresis, D_n to Q_n	Connect H to GND, Waveform 1	6.6	30	6.7	18.0	25	6.6	30	ns
t_{PHL}			3.7	17	3.7	10.0	15	3.7	40	ns
t_{PLH}	Propagation delay $\overline{E}$ to Q_n	Waveforms 2, 4	2.7	11	2.7	5.0	9.0	2.7	11	ns
t_{PHL}			2.7	11	2.7	5.0	9.0	2.7	11	ns
t_{PLH}	Propagation delay ST to Q_n	Waveform 3	1.6	8.0	1.6	4.0	7.0	1.6	8.0	ns
t_{PHL}			1.6	8.0	1.6	4.0	7.0	1.6	8.0	ns
t_{PLH}	Propagation delay R to Q_n	Waveform 4	2.0	8.0	2.0	5.0	6.5	2.0	8.0	ns
t_{PHL}			2.0	8.0	2.0	5.0	6.5	2.0	8.0	ns
t_s	Setup time D_n to $\overline{E}$	Waveform 5	30		2.7	15.0		30		ns
t_h	Hold time D_n to $\overline{E}$	Waveform 5	0		–2.0	15.0		–2.0		ns
t_{TLH}	Transition time 20% to 80%, 80% to 20%	Waveforms 1, 2, 3, 4	1.5	5.0	1.5	2.0	4.3	1.5	5.0	ns
t_{THL}			1.5	5.0	1.5	2.0	4.3	1.5	5.0	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

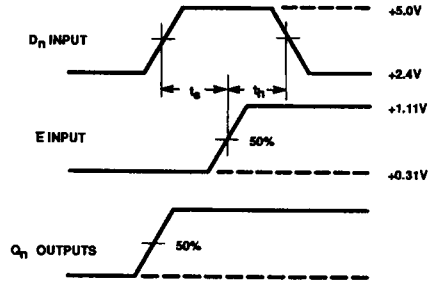
AC WAVEFORMS



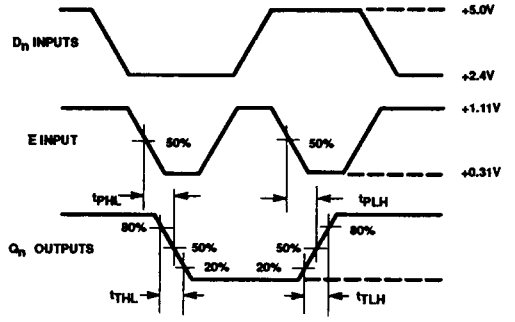
Waveform 1. D_n Timing ($\overline{E}$ and R are Low, ST is High)



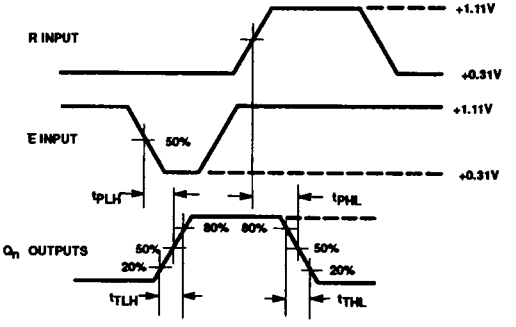
Waveform 3. Strobe Timing ($\overline{E}$ and R are Low, D_n is High)



Waveform 5. Setup and Hold Times

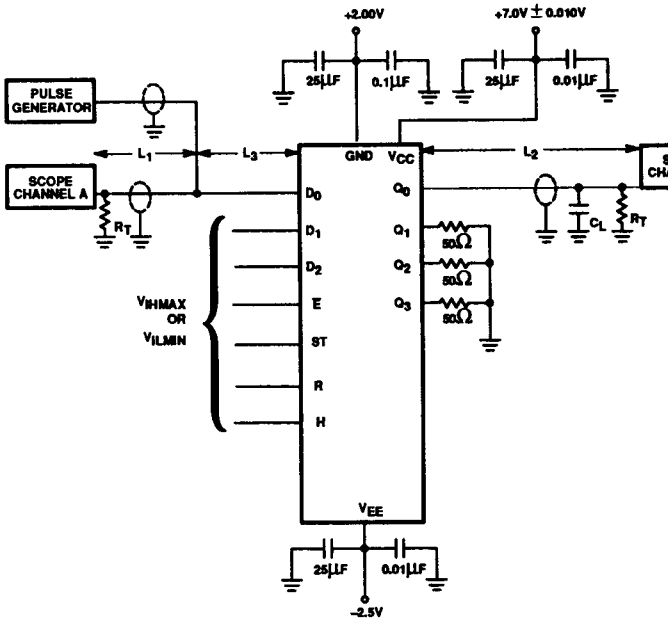


Waveform 2. D_n Timing (R is Low, ST is High)



Waveform 4. Reset Timing (D_n and ST are High)

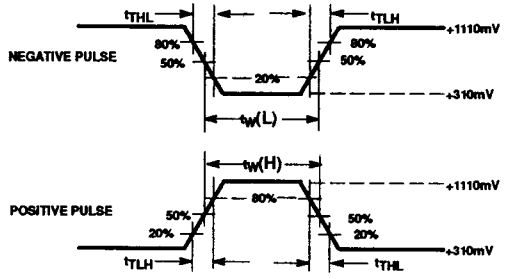
AC TEST CIRCUIT



NOTES:

1. GND =+2.0V ±0.010V, V_{CC} = + 7.0V ± 0.010V. V_{EE} = –3.2V ± 0.010V
2. Decoupling 0.1µF and 25µFfrom GND to system ground, 0.01µF and 25µF from V_{CC} to system ground (0.01µF and 0.1µF capacitors should be NPO Ceramic or MLC type). All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either a High or a Low state, consistent with the logic function required.
4. All unused outputs are loaded with 50Ω to system ground.
5. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
6. R_T = 50Ω termination internal to scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. Fixture and stray capacitance = $C_L \leq 3pF$.
9. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

ECL INPUT PULSE DEFINITION

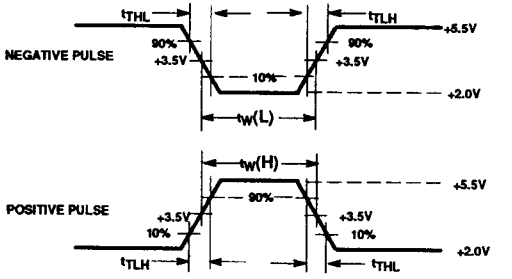


INPUT PULSE REQUIREMENTS

GND = +2.0V± 0.010V, V_{CC} = +7.0V ± 0.010V, V_{EE} = –3.2V± 0.010V, V_T = 0V (system ground)

Family	Amplitude	Rep Rate	$t_W(H)$, $t_W(L)$	t_{TLH}	t_{THL}
10K ECL	800mV_{P-P}	1MHz	500ns	2.0 ± 0.2ns	2.0 ± 0.2ns

TTL INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS

GND = +2.0V ± 0.010V, V_{CC} = +7.0V ±0.010V, V_{EE} = –3.2V ±0.010V, V_T = 0V (system ground)

Family	Amplitude	Rep Rate	$t_W(H)$, $t_W(L)$	t_{TLH}	t_{THL}
TTL	3.0V_{P-P}	1MHz	500ns	2.5 ± 0.2ns	2.5 ± 0.2ns