MT90823

3 V Large Digital Switch

Data Sheet

July 2005

Features

- 2,048 × 2,048 channel non-blocking switching at 8.192 Mb/s
- Per-channel variable or constant throughput delay
- Automatic identification of ST-BUS/GCI interfaces
- Accept ST-BUS streams of 2.048, 4.096 or 8.192 Mb/s
- Automatic frame offset delay measurement
- Per-stream frame delay offset programming
- Per-channel high impedance output control
- Per-channel message mode
- Control interface compatible to Motorola non-multiplexed CPUs
- Connection memory block programming
- 3.3 V local I/O with 5 V tolerant inputs and TTL-compatible outputs
- IEEE-1149.1 (JTAG) Test Port

Ordering Information

MT90823AP	84 Pin PLCC	Tubes
MT90823AL	100 Pin MQFP	Trays
MT90823AB	100 Pin LQFP	Trays
MT90823AG	120 Pin BGA	Trays
MT90823AB1	100 Pin LQFP*	Trays
MT90823AP1	84 Pin PLCC*	Tubes
MT90823AL1	100 Pin MQFP*	Trays

*Pb Free Matte Tin

-40°C to +85°C

Applications

- Medium and large switching platforms
- CTI application
- Voice/data multiplexer
- Digital cross connects
- ST-BUS/GCI interface functions
- Support IEEE 802.9a standard

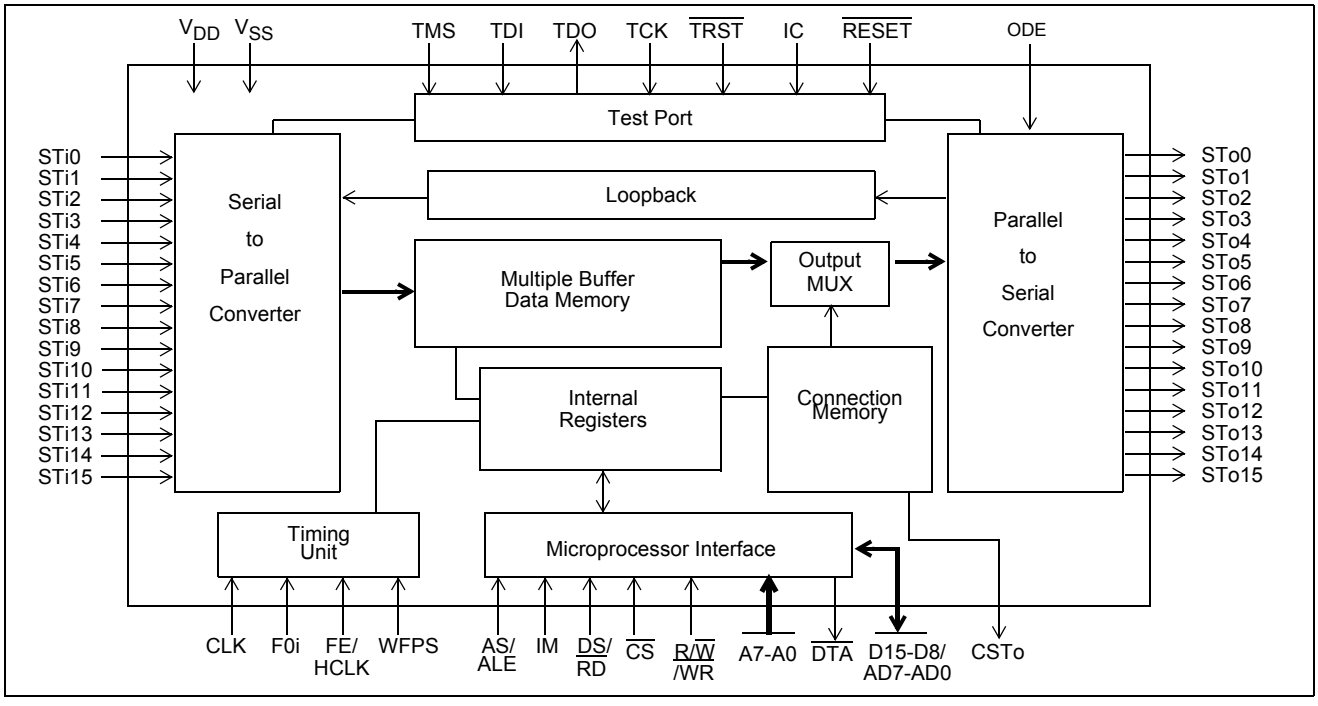


Figure 1 - Functional Block Diagram

Description

The MT90823 Large Digital Switch has a non-blocking switch capacity of: 2,048 x 2,048 channels at a serial bit rate of 8.192 Mb/s; 1,024 x 1,024 channels at 4.096 Mb/s; and 512 x 512 channels at 2.048 Mb/s. The device has many features that are programmable on a per stream or per channel basis, including message mode, input offset delay and high impedance output control.

Per stream input delay control is particularly useful for managing large multi-chip switches that transport both voice channel and concatenated data channels.

In addition, the input stream can be individually calibrated for input frame offset using a dedicated pin.

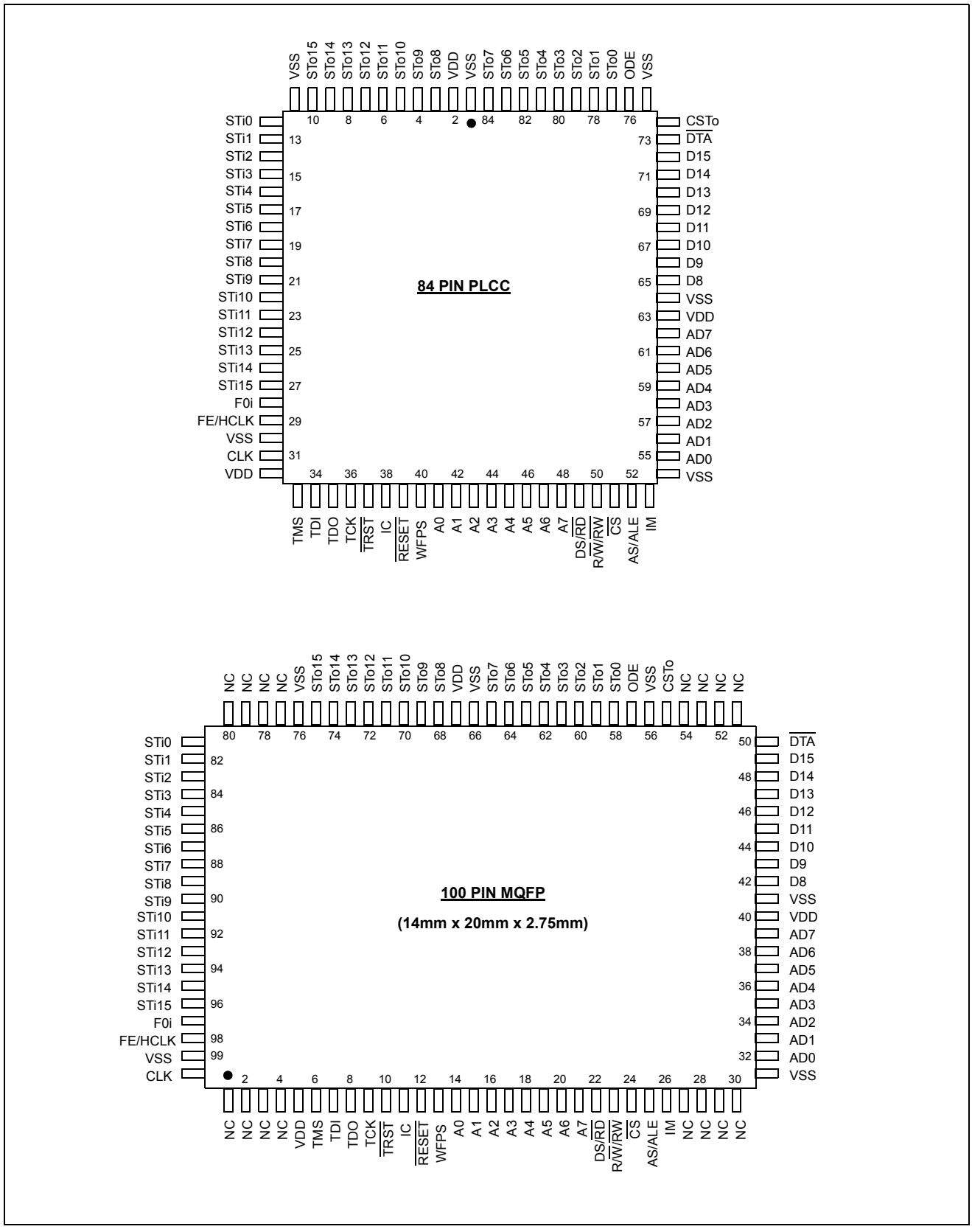
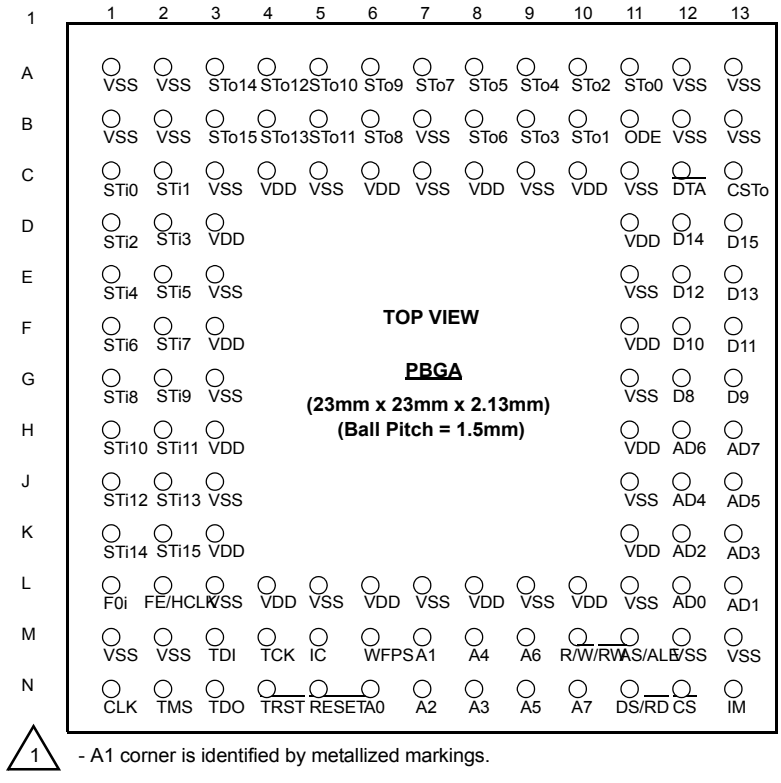


Figure 2 - PLCC and MQFP Pin Connections



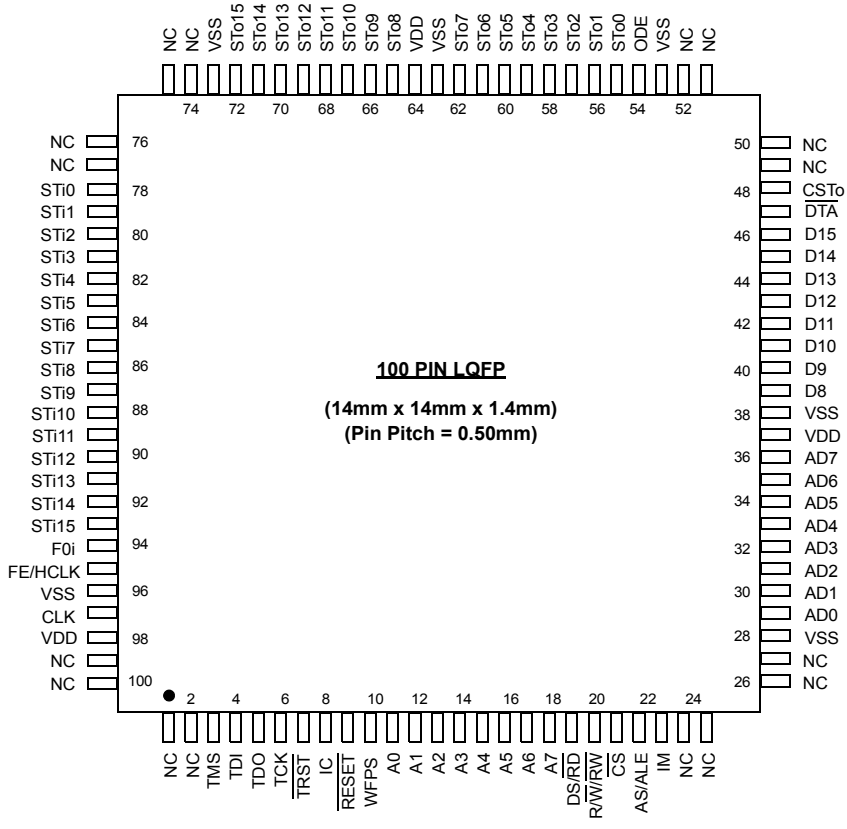


Figure 3 - PBGA and LQFP Pin Connections

Pin Description

Pin #				Name	Description
84 PLCC	100 MQFP	100 LQFP	120 BGA		
1, 11, 30, 54 64, 75	31, 41, 56, 66, 76, 99	28, 38, 53, 63, 73, 96	A1,A2,A12,A13, B1,B2,B7,B12, B13,C3,C5,C7, C9,C11,E3,E11 G3,G11,J3,J11, L3,L5,L7,L9,L11, M1,M2,M12,M13	V_{SS}	**Ground.**
2, 32, 63	5, 40, 67	37, 64,98	C4,C6,C8,C10, D3,D11,F3,F11, H3,H11,K3,K11, L4,L6,L8,L10	V_{DD}	**+3.3 Volt Power Supply.**
3 - 10	68-75	65 - 72	B6,A6,A5,B5,A4, B4,A3,B3	STo8 - 15	**ST-BUS Output 8 to 15 (5 V Tolerant Three-state Outputs):** Serial data Output stream. These streams may have data rates of 2.048, 4.096 or 8.192 Mb/s, depending upon the value programmed at bits DR0 - 1 in the IMS register.
12 - 27	81-96	78 - 93	C1,C2,D1,D2,E1, E2,F1,F2,G1,G2, H1,H2,J1,J2,K1, K2	STi0 - 15	**ST-BUS Input 0 to 15 (5 V Tolerant Inputs):** Serial data input stream. These streams may have data rates of 2.048, 4.096 or 8.192 Mb/s, depending upon the value programmed at bits DR0 - 1 in the IMS register.
28	97	94	L1	F0i	**Frame Pulse (5 V Tolerant Input):** When the WFPS pin is low, this input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS and GCI specifications. When the WFPS pin is high, this pin accepts a negative frame pulse which conforms to WFPS formats.
29	98	95	L2	FE/HCLK	**Frame Evaluation / HCLK Clock (5 V Tolerant Input):** When the WFPS pin is low, this pin is the frame measurement input. When the WFPS pin is high, the HCLK (4.096MHz clock) is required for frame alignment in the wide frame pulse (WFP) mode.
31	100	97	N1	CLK	**Clock (5 V Tolerant Input):** Serial clock for shifting data in/out on the serial streams (STi/o 0 - 15). Depending upon the value programmed at bits DR0 - 1 in the IMS register, this input accepts a 4.096, 8.192 or 16.384 MHz clock.
33	6	3	N2	TMS	**Test Mode Select (3.3 V Input with internal pull-up):** JTAG signal that controls the TAP controller state transitions.
34	7	4	M3	TDI	**Test Serial Data In (3.3 V Tolerant Input with internal pull-up):** JTAG serial test instructions and data are shifted in on this pin.

Pin Description (continued)

Pin #				Name	Description
84 PLCC	100 MQFP	100 LQFP	120 BGA		
35	8	5	N3	TDO	**Test Serial Data Out (3.3 V Output):** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
36	9	6	M4	TCK	**Test Clock (5 V Tolerant Input):** Provides the clock to the JTAG test logic.
37	10	7	N4	$\overline{\text{TRST}}$	**Test Reset (3.3 V Input with internal pull-up):** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up, or held low, to ensure that the MT90823 is in the normal functional mode.
38	11	8	M5	IC	**Internal Connection (3.3 V Input with internal pull-down):** Connect to V_{SS} for normal operation. This pin must be low for the MT90823 to function normally and to comply with IEEE 1149 (JTAG) boundary scan requirements.
39	12	9	N5	$\overline{\text{RESET}}$	**Device Reset (5 V Tolerant Input):** This input (active LOW) puts the MT90823 in its reset state to clear the device internal counters, registers and bring STo0 - 15 and microport data outputs to a high impedance state. The time constant for a power up reset circuit must be a minimum of five times the rise time of the power supply. In normal operation, the $\overline{\text{RESET}}$ pin must be held low for a minimum of 100 nsec to reset the device.
40	13	10	M6	WFPS	**Wide Frame Pulse Select (5 V Tolerant Input):** When 1, enables the wide frame pulse (WFP) Frame Alignment interface. When 0, the device operates in ST-BUS/GCI mode.
41 - 48	14-21	11 - 18	N6,M7,N7,N8, M8,N9,M9,N10	A0 - A7	**Address 0 - 7 (5 V Tolerant Input):** When non-multiplexed CPU bus operation is selected, these lines provide the A0 - A7 address lines to the internal memories.
49	22	19	N11	DS/$\overline{\text{RD}}$	**Data Strobe / Read (5 V Tolerant Input):** For Motorola multiplexed bus operation, this input is DS. This active high DS input works in conjunction with $\overline{\text{CS}}$ to enable the read and write operations. For Motorola non-multiplexed CPU bus operation, this input is DS. This active low input works in conjunction with $\overline{\text{CS}}$ to enable the read and write operations. For multiplexed bus operation, this input is $\overline{\text{RD}}$. This active low input sets the data bus lines (AD0-AD7, D8-D15) as outputs.

Pin Description (continued)

Pin #				Name	Description
84 PLCC	100 MQFP	100 LQFP	120 BGA		
50	23	20	M10	R/$\overline{W}$ / $\overline{WR}$	**Read/Write / Write (5 V Tolerant Input):** In the cases of Motorola non-multiplexed and multiplexed bus operations, this input is R/W. This input controls the direction of the data bus lines (AD0 - AD7, D8-D15) during a microprocessor access. For multiplexed bus operation, this input is WR. This active low input is used with RD to control the data bus (AD0 - 7) lines as inputs.
51	24	21	N12	$\overline{CS}$	**Chip Select (5 V Tolerant Input):** Active low input used by a microprocessor to activate the microprocessor port of MT90823.
52	25	22	M11	AS/ALE	**Address Strobe or Latch Enable (5 V Tolerant Input):** This input is used if multiplexed bus operation is selected via the IM input pin. For Motorola non-multiplexed bus operation, connect this pin to ground.
53	26	23	N13	IM	**CPU Interface Mode (5 V Tolerant Input):** When IM is high, the microprocessor port is in the multiplexed mode. When IM is low, the microprocessor port is in non-multiplexed mode.
55 - 62	32-39	29 - 36	L12,L13,K12, K13,J12,J13, H12,H13	AD0 - 7	**Address/Data Bus 0 to 7 (5 V Tolerant I/O):** These pins are the eight least significant data bits of the microprocessor port. In multiplexed mode, these pins are also the input address bits of the microprocessor port.
65 - 72	42-49	39 - 46	G12,G13,F12, F13,E12,E13, D12,D13	D8 - 15	**Data Bus 8-15 (5 V Tolerant I/O):** These pins are the eight most significant data bits of the microprocessor port.
73	50	47	C12	$\overline{DTA}$	**Data Transfer Acknowledgement (5 V tolerant Three-state Output):** Indicates that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then tri-states, allowing for faster bus cycles with a weaker pull-up resistor. A pull-up resistor is required to hold a HIGH level when the pin is tri-stated.
74	55	48	C13	CSTo	**Control Output (5 V Tolerant Output).** This is a 4.096, 8.192 or 16.384 Mb/s output containing 512, 1024 or 2048 bits per frame respectively. The level of each bit is determined by the CSTo bit in the connection memory. See External Drive Control Section.

Pin Description (continued)

Pin #				Name	Description
84 PLCC	100 MQFP	100 LQFP	120 BGA		
76	57	54	B11	ODE	**Output Drive Enable (5 V Tolerant Input):** This is the output enable control for the STo0-15 serial outputs. When ODE input is low and the OSB bit of the IMS register is low, STo0-15 are in a high impedance state. If this input is high, the STo0-15 output drivers are enabled. However, each channel may still be put into a high impedance state by using the per channel control bit in the connection memory.
77 - 84	58-65	55 - 62	A11,B10,A10,B9, A9,A8,B8,A7	STo0 - 7	**Data Stream Output 0 to 7 (5 V Tolerant Three-state Outputs):** Serial data Output stream. These streams have selectable data rates of 2.048, 4.096 or 8.192 Mb/s.
-	1 - 4, 27 - 30, 51 - 54 77 - 80	1 - 2, 24 - 27, 49 - 52, 74 - 77, 99 - 100		NC	**No connection.**

Device Overview

The MT90823 Large Digital Switch is capable of switching up to 2,048 × 2,048 channels. The MT90823 is designed to switch 64 kb/s PCM or N x 64 kb/s data. The device maintains frame integrity in data applications and minimum throughput delay for voice applications on a per channel basis.

The serial input streams of the MT90823 can have a bit rate of 2.048, 4.096 or 8.192 Mbit/s and are arranged in 125 μs wide frames, which contain 32, 64 or 128 channels, respectively. The data rates on input and output streams are identical.

By using Zarllink's message mode capability, the microprocessor can access input and output time-slots on a per channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS devices. The MT90823 automatically identifies the polarity of the frame synchronization input signal and configures its serial streams to be compatible to either ST-BUS or GCI formats.

Two different microprocessor bus interfaces can be selected through the Input Mode pin (IM): Non-multiplexed or Multiplexed. These interfaces provide compatibility with multiplexed and Motorola multiplexed/non-multiplexed buses.

The frame offset calibration function allows users to measure the frame offset delay using a frame evaluation pin (FE). The input offset delay can be programmed for individual streams using internal frame input offset registers, see Table 11.

The internal loopback allows the ST-BUS output data to be looped around to the ST-BUS inputs for diagnostic purposes.

Functional Description

A functional Block Diagram of the MT90823 is shown in Figure 1.

Data and Connection Memory

For all data rates, the received serial data is converted to parallel format by internal serial-to-parallel converters and stored sequentially in the data memory. Depending upon the selected operation programmed in the interface mode select (IMS) register, the useable data memory may be as large as 2,048 bytes. The sequential addressing of the data memory is performed by an internal counter, which is reset by the input 8 kHz frame pulse (F0i) to mark the frame boundaries of the incoming serial data streams.

Data to be output on the serial streams may come from either the data memory or connection memory. Locations in the connection memory are associated with particular ST-BUS output channels. When a channel is due to be transmitted on an ST-BUS output, the data for this channel can be switched either from an ST-BUS input in connection mode, or from the lower half of the connection memory in message mode. Data destined for a particular channel on a serial output stream is read from the data memory or connection memory during the previous channel time-slot. This allows enough time for memory access and parallel-to-serial conversion.

Connection and Message Modes

In the connection mode, the addresses of the input source data for all output channels are stored in the connection memory. The connection memory is mapped in such a way that each location corresponds to an output channel on the output streams. For details on the use of the source address data (CAB and SAB bits), see Table 13 and Table 14. Once the source address bits are programmed by the microprocessor, the contents of the data memory at the selected address are transferred to the parallel-to-serial converters and then onto an ST-BUS output stream.

By having several output channels connected to the same input source channel, data can be broadcasted from one input channel to several output channels.

In message mode, the microprocessor writes data to the connection memory locations corresponding to the output stream and channel number. The lower half (8 least significant bits) of the connection memory content is transferred directly to the parallel-to-serial converter. This data will be output on the ST-BUS streams in every frame until the data is changed by the microprocessor.

The five most significant bits of the connection memory controls the following for an output channel: message or connection mode; constant or variable delay; enables/tristate the ST-BUS output drivers; and, enables/disable the loopback function. In addition, one of these bits allows the user to control the CSTo output.

If an output channel is set to a high-impedance state through the connection memory, the ST-BUS output

will be in a high impedance state for the duration of that channel. In addition to the per-channel control, all channels on the ST-BUS outputs can be placed in a high impedance state by either pulling the ODE input pin low or programming the output standby (OSB) bit in the interface mode selection register to low. This action overrides the individual per-channel programming by the connection memory bits.

The connection memory data can be accessed via the microprocessor interface through the D0 to D15 pins. The addressing of the device internal registers, data and connection memories is performed through the address input pins and the Memory Select (MS) bit of the control register. For details on device addressing, see Software Control and Control Register bits description (Tables 4, 6 and 7).

Serial Data Interface Timing

The master clock frequency must always be twice the data rate. The master clock (CLK) must be either at 4.096, 8.192 or 16.384 MHz for serial data rate of 2.048, 4.096 or 8.192 Mb/s respectively. The input and output stream data rates will always be identical.

The MT90823 provides two different interface timing modes controlled by the WFPS pin. If the WFPS pin is low, the MT90823 is in ST-BUS/GCI mode. If the WFPS pin is high, the MT90823 is in the wide frame pulse (WFP) frame alignment mode.

In ST-BUS/GCI mode, the input 8 kHz frame pulse can be in either ST-BUS or GCI format. The MT90823 automatically detects the presence of an input frame pulse and identifies it as either ST-BUS or GCI. In ST-BUS format, every second falling edge of the master clock marks a bit boundary and the data is clocked in on the rising edge of CLK, three quarters of the way into the bit cell, see Figure 11. In GCI format, every second rising edge of the master clock marks the bit boundary and data is clocked in on the falling edge of CLK at three quarters of the way into the bit cell, see Figure 12.

Wide Frame Pulse (WFP) Frame Alignment Timing

When the device is in WFP frame alignment mode, the CLK input must be at 16.384 MHz, the FE/HCLK input is 4.096 MHz and the 8 kHz frame pulse is in ST-BUS format. The timing relationship between CLK, HCLK and the frame pulse is defined in Figure 13.

When the WFPS pin is high, the frame alignment evaluation feature is disabled, but the frame input offset registers may still be programmed to compensate for the varying frame delays on the serial input streams.

Switching Configurations

The MT90823 maximum non-blocking switching configurations is determined by the data rates selected for the serial inputs and outputs. The switching configuration is selected by two DR bits in the IMS register. See Table 8 nd Table 9.

2.048 Mb/s Serial Links (DR0=0, DR1=0)

When the 2.048 Mb/s data rate is selected, the device is configured with 16-input/16-output data streams each having 32 64 kb/s channels. This mode requires a CLK of 4.094 MHz and allows a maximum non-blocking capacity of 512 x 512 channels.

4.096 Mb/s Serial Links (DR0=1, DR1=0)

When the 4.096 Mb/s data rate is selected, the device is configured with 16-input/16-output data streams each having 64 64 kb/s channels. This mode requires a CLK of 8.192 MHz and allows a maximum non-blocking capacity of 1,024 x 1,024 channels.

8.192 Mb/s Serial Links (DR0=0, DR1=1)

When the 8.192 Mb/s data rate is selected, the device is configured with 16-input/16-output data streams each having 128 64 kb/s channels. This mode requires a CLK of 16.384 MHz and allows a maximum non-blocking capacity of 2,048 x 2,048 channels. Table 1 summarizes the switching configurations and the relationship between different serial data rates and the master clock frequencies.

Serial Interface Data Rate	Master Clock Required (MHz)	Matrix Channel Capacity
2 Mb/s	4.096	512 x 512
4 Mb/s	8.192	1,024 x 1,024
8 Mb/s	16.384	2,048 x 2,048

Table 1 - Switching Configuration

Input Frame Offset Selection

Input frame offset selection allows the channel alignment of individual input streams to be offset with respect to the output stream channel alignment (i.e., F0i). This feature is useful in compensating for variable path delays caused by serial backplanes of variable lengths, which may be implemented in large centralized and distributed switching systems.

Each input stream can have its own delay offset value by programming the frame input offset (FOR) registers. Possible adjustment can range up to +4 master clock (CLK) periods forward with resolution of 1/2 clock period. The output frame offset cannot be offset or adjusted. See Figure 4, Table 11 and Table 12 for delay offset programming.

Serial Input Frame Alignment Evaluation

The MT90823 provides the frame evaluation (FE) input to determine different data input delays with respect to the frame pulse F0i.

A measurement cycle is started by setting the start frame evaluation (SFE) bit low for at least one frame. Then the evaluation starts when the SFE bit in the IMS register is changed from low to high. Two frames later, the complete frame evaluation (CFE) bit of the frame alignment register (FAR) changes from low to high. This signals that a valid offset measurement is ready to be read from bits 0 to 11 of the FAR register. The SFE bit must be set to zero before starting a new measurement cycle.

In ST-BUS mode, the falling edge of the frame measurement signal (FE) is evaluated against the falling edge of the ST-BUS frame pulse. In GCI mode, the rising edge of FE is evaluated against the rising edge of the GCI frame pulse. See Table 10 and Figure 3 for the description of the frame alignment register.

This feature is not available when the WFP Frame Alignment mode is enabled (i.e., when the WFPS pin is connected to VDD).

Memory Block Programming

The MT90823 provides users with the capability of initializing the entire connection memory block in two frames. Bits 11 to 15 of every connection memory location will be programmed with the pattern stored in bits 5 to 9 of the IMS register.

The block programming mode is enabled by setting the memory block program (MBP) bit of the control register high. When the block programming enable (BPE) bit of the IMS register is set to high, the block programming data will be loaded into the bits 11 to 15 of every connection memory location. The other connection memory bits (bit 0 to bit 10) are loaded with zeros. When the memory block programming is complete, the device resets the BPE bit to zero.

Loopback Control

The loopback control (LPBK) bit of each connection memory location allows the ST-BUS output data to be looped backed internally to the ST-BUS input for diagnostic purposes.

If the LPBK bit is high, the associated ST-BUS output channel data is internally looped back to the ST-BUS input channel (i.e., data from STo *n* channel *m* will appear in STi n channel M). **Note:** when LPBK is activated in channel *m* STo n+1 (for *n* even) or STo n-1 (for *n* odd), the data from channel *m* of STi *n* will be switched to channel *m* STo *n*. The associated frame delay offset register must be set to zero for proper operation of the per-channel loopback function. If the LPBK bit is low, the per-channel loopback feature is disabled and the device will function normally.

Delay Through the MT90823

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time-slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice application, select variable throughput delay to ensure minimum delay between input and output data. In wideband data applications, select constant throughput delay to maintain the frame integrity of the information through the switch.

The delay through the device varies according to the type of throughput delay selected in the $\overline{V}$/C bit of the connection memory.

Variable Delay Mode ($\overline{V}$/C bit = 0)

The delay in this mode is dependent only on the combination of source and destination channels. It is independent of input and output streams. The minimum delay achievable in the MT90823 is three time-slots. When the input channel data is switched to the same output channel (channel n, frame p), it will be output in the following frame (channel n, frame p+1). The same frame delay occurs if the input channel n is switched to output channel n+1 or n+2. When input channel n is switched to output channel n+3, n+4,..., the new output data will appear in the same frame. Table 2 shows the possible delays for the MT90823 in the variable delay mode.

Constant Delay Mode ($\overline{V}$/C bit = 1)

In this mode, frame integrity is maintained in all switching configurations by using a multiple data memory buffer. Input channel data written into the data memory buffers during frame n will be read out during frame n+2.

In the MT90823, the minimum throughput delay achievable in the constant delay mode is one frame. For example, in 2 Mb/s mode, when input time-slot 31 is switched to output time-slot 0. The maximum delay of 94 time-slots occurs when time-slot 0 in a frame is switched to time-slot 31 in the frame. See Table 3.

Microprocessor Interface

The MT90823 provides a parallel microprocessor interface for non-multiplexed or multiplexed bus structures. This interface is compatible with Motorola non-multiplexed and multiplexed buses.

If the IM pin is low, the MT90823 microprocessor interface assumes Motorola non-multiplexed bus mode. If the IM pin is high, the device micro- processor interface accepts two different timing modes (mode1 and mode2) which allows direct connection to multiplexed microprocessors.

The microprocessor interface automatically identifies the type of microprocessor bus connected to the MT90823. This circuit uses the level of the DS/$\overline{RD}$ input pin at the rising edge of AS/ALE to identify the appropriate bus timing connected to the MT90823. If DS/$\overline{RD}$ is high at the falling edge of AS/ALE, then the mode 1 multiplexed timing is selected. If DS/$\overline{RD}$ is low at the falling edge of AS/ALE, then the mode 2 multiplexed bus timing is selected.

Input Rate	Delay for Variable Throughput Delay Mode (m - output channel number) (n - input channel number))		
	m < n	m = n, n+1, n+2	m > n+2
2.048 Mb/s	32 - (n-m) time-slots	m-n + 32 time-slots	m-n time-slots
4.096 Mb/s	64 - (n-m) time-slots	m-n + 64 time-slots	m-n time-slots
8.192 Mb/s	128 - (n-m) time-slots	m-n + 128 time-slots	m-n time-slots

Table 2 - Variable Throughput Delay Value

Input Rate	Delay for Constant Throughput Delay Mode (m - output channel number) (n - input channel number))
2.048 Mb/s	32 + (32 - n) + (m - 1) time-slots
4.096 Mb/s	64 + (64 - n) + (m- 1) time-slots
8.192 Mb/s	128 + (128 - n) + (m- 1) time-slots

Table 3 - Constant Throughput Delay Value

For multiplexed operation, the 8-bit data and address (AD0-AD7), 8-bit Data (D8-D15), Address strobe/Address latch enable (AS/ALE), Data strobe/Read (DS/$\overline{RD}$), Read/Write /Write (R/$\overline{W}$ / $\overline{WR}$), Chip select ($\overline{CS}$) and Data transfer acknowledge ($\overline{DTA}$) signals are required. See Figure 13 and Figure 14 for multiplexed parallel microport timing.

For the Motorola non-multiplexed bus, the 16-bit data bus (AD0-AD7, D8-D15), 8-bit address bus (A0-A7) and 4 control lines ($\overline{CS}$, DS, R/$\overline{W}$ and $\overline{DTA}$) signals are required. See Figure 15 for Motorola non- multiplexed microport timing.

The MT90823 microport provides access to the internal registers, connection and data memories. All locations provide read/write access except for the data memory and the frame alignment register which are read only.

Memory Mapping

The address bus on the microprocessor interface selects the MT90823 internal registers and memory. If the A7 address input is low, then the control (CR), interface mode selection (IMS), frame alignment (FAR) and frame input offset (FOR) registers are addressed by A6 to A0 as shown in Table 4.

If the A7 address input is high, then the remaining address input lines are used to select up to 128 memory subsection locations. The number selected corresponds to the maximum number of channels per input or output stream. The address input lines and the stream address bits (STA) of the control register allow access to the entire data and connection memories.

The control and IMS registers together control all the major functions of the device. The IMS register should be programmed immediately after system power-up to establish the desired switching configuration (see “Serial Data Interface Timing” and “Switching Configurations”).

The control register controls switching operations in the MT90823. It selects the internal memory locations that specify the input and output channels selected for switching.

The data in the control register consists of the memory block programming bit (MBP), the memory select bit (MS) and the stream address bits (STA). The memory block programming bit allows users to program the entire connection memory block, (see “Memory Block Programming”). The memory select bit controls the selection of the connection memory or the data Memory. The stream address bits define an internal memory subsections corresponding to input or output ST-BUS streams.

The data in the IMS register consists of block programming bits (BPD0-BPD4), block programming enable bit (BPE), output standby bit (OSB), start frame evaluation bit (SFE) and data rate selection bits (DR0, DR1). The block programming and the block programming enable bits allows users to program the entire connection memory, (see Memory Block Programming section). If the ODE pin is low, the OSB bit enables (if high) or disables (if low) all ST-BUS output drivers. If the ODE pin is high, the contents of the OSB bit is ignored and all ST-BUS output drivers are enabled.

Connection Memory Control

The contents of the CSTo bit of each connection memory location are output on the CSTo pin once every frame. The CSTo pin is a 4.096, 8.192 or 16.384 Mb/s output carrying 512, 1,024 or 2,048 bits respectively. If the CSTo bit is set high, the corresponding bit on the CSTo output is transmitted high. If the CSTo bit is low, the corresponding bit on the CSTo output is transmitted low. The contents of the CSTo bits of the connection memory are transmitted sequentially via the CSTo pin and are synchronous with the data rates on the other ST-BUS streams.

The CSTo bit is output one channel before the corresponding channel on the ST-BUS. For example, in 2 Mb/s mode, the contents of the CSTo bit in position 0 (STo0, CH0) of the connection memory is output on the first clock cycle of channel 31 via CSTo pin. The contents of the CSTo bit in position 32 (STo1, CH0) of the connection memory is output on the second clock cycle of channel 31 via CSTo pin.

When either the ODE pin or the OSB bit is high, the OE bit of each connection memory location enables (if high) or disables (if low) the output drivers for an individual ST-BUS output stream and channel. Table 5 details this function.

The connection memory message channel (MC) bit (if high) enables message mode in the associated ST-BUS output channel. When message mode is enabled, only the lower half (8 least significant bits) of the connection memory is transferred to the ST-BUS outputs.

If the MC bit is low, the contents of the connection memory stream address bit (SAB) and channel address bit (CAB) defines the source information (stream and channel) of the time-slot that will be switched to the output.

Bit $\overline{V}$/C (Variable/Constant Delay) of each connection memory location allows the per-channel selection between variable and constant throughput delay modes.

The loopback bit should be used for diagnostic purpose only; this bit should be set to zero for normal operation. If all LPBK bits are set high for all connection memory locations, the associated ST-BUS output channel data is internally looped back to the ST-BUS input channel (i.e., STo*N* channel *m* data loops back to STi *N* channel *m*).

A7 (Note 1)	A6	A5	A4	A3	A2	A1	A0	Location
0	0	0	0	0	0	0	0	Control Register, CR
0	0	0	0	0	0	0	1	Interface Mode Selection Register, IMS
0	0	0	0	0	0	1	0	Frame Alignment Register, FAR
0	0	0	0	0	0	1	1	Frame Input Offset Register 0, FOR0
0	0	0	0	0	1	0	0	Frame Input Offset Register 1, FOR1
0	0	0	0	0	1	0	1	Frame Input Offset Register 2, FOR2
0	0	0	0	0	1	1	0	Frame Input Offset Register 3, FOR3
1	0	0	0	0	0	0	0	Ch 0
1	0	0	0	0	0	0	1	Ch 1
1	0	0	.	.	.	.	.	.
1	0	0	1	1	1	1	0	Ch 30
1	0	0	1	1	1	1	1	Ch 31 (Note 2)
1	0	1	0	0	0	0	0	Ch 32
1	0	1	0	0	0	0	1	Ch 33
1	0	1	.	.	.	.	.	.
1	0	1	1	1	1	1	0	Ch 62
1	0	1	1	1	1	1	1	Ch 63 (Note 3)
1	1	0	0	0	0	0	0	Ch 64
1	1	0	0	0	0	0	1	Ch 65
1	1	.	.	.	.	.	.	.
1	1	1	1	1	1	1	0	Ch 126
1	1	1	1	1	1	1	1	Ch 127 (Note 4)

Notes:
1. Bit A7 must be high for access to data and connection memory positions. Bit A7 must be low for access to registers.
2. Channels 0 to 31 are used when serial interface is at 2Mb/s mode.
3. Channels 0 to 63 are used when serial interface is at 4Mb/s mode.
4. Channels 0 to 127 are used when serial interface is at 8Mb/s mode.

Table 4 - Internal Register and Address Memory Mapping

OE bit in Connection Memory	ODE pin	OSB bit in IMS register	ST-BUS Output Driver Status
0	Don't Care	Don't Care	Per Channel High Impedance
1	0	0	High Impedance
1	0	1	Enable
1	1	Don't care	Enable

Table 5 - Output High Impedance Control

If the LPBK bit is low, the loopback feature is disabled. For proper per-channel loopback operation, the contents of the frame delay offset registers must be set to zero.

Initialization of the MT90823

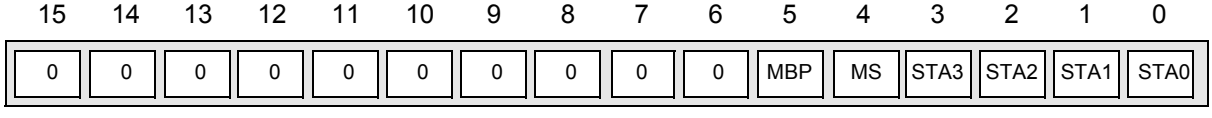
During power up, the $\overline{\text{TRST}}$ pin should be pulsed low, or held low continuously, to ensure that the MT90863 is in the normal functional mode. A 5K pull-down resistor can be connected to this pin so that the device will not enter the JTAG test mode during power up.

Upon power up, the contents of the connection memory can be in any state and the ODE pin should be held low to keep all ST-BUS outputs in a high impedance state until the microprocessor has initialized the switching matrix.

To prevent two ST-BUS outputs from driving the same stream simultaneously, the microprocessor should program the desired active paths through the switch and put all other channels into a high impedance state during the initialization routine by using the block programming mode. In addition, the loopback bits in the connection memory should be cleared for normal operation.

When this process is complete, the microprocessor controlling the matrices can bring the ODE pin or OSB bit high to relinquish the high impedance state control to the OE bit in the connection memory.

Read/Write Address: 00_H,
Reset Value: 0000_H.



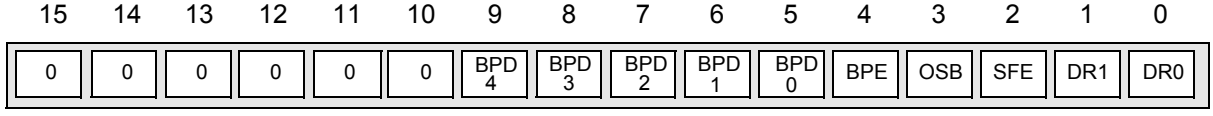
Bit	Name	Description
15 - 6	Unused	Must be zero for normal operation.
5	MBP	**Memory Block Program.** When 1, the connection memory block programming feature is ready for the programming of Connection Memory high bits, bit 11 to bit 15. When 0, this feature is disabled.
4	MS	**Memory Select.** When 0, connection memory is selected for read or write operations. When 1, the data memory is selected for read operations and connection memory is selected for write operations. (No microprocessor write operation is allowed for the data memory.)
3 - 0	STA3-0	**Stream Address Bits**. The binary value expressed by these bits refers to the input or output data stream, which corresponds to the subsection of memory made accessible for subsequent operations. (STA3 = MSB, STA0 = LSB)

Table 6 - Control (CR) Register Bits

Input/Output Data Rate	Valid Address Lines
2.048 Mb/s	A4, A3, A2, A1, A0
4.096 Mb/s	A5, A4, A3, A2, A1, A0
8.192 Mb/s	A6, A5, A4 A3, A2, A1, A0

Table 7 - Valid Address lines for Different Bit Rates

Read/Write Address: 01_H,
Reset Value: 0000_H.



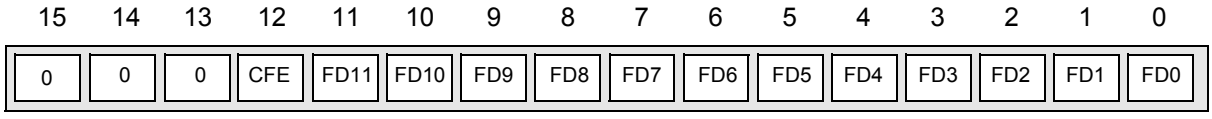
Bit	Name	Description
15-10	Unused	Must be zero for normal operation.
9-5	BPD4-0	**Block Programming Data.** These bits carry the value to be loaded into the connection memory block whenever the memory block programming feature is activated. After the MBP bit in the control register is set to 1 and the BPE bit is set to 1, the contents of the bits BPD4- 0 are loaded into bit 15 to bit 11 of the connection memory. Bit 10 to bit 0 of the connection memory are set to 0.
4	BPE	**Begin Block programming Enable.** A zero to one transition of this bit enables the memory block programming function. The BPE and BPD4-0 bits in the IMS register have to be defined in the same write operation. Once the BPE bit is set high, the device requires two frames to complete the block programming. After the programming function has finished, the BPE bit returns to zero to indicate the operation is completed. When the BPE = 1, the BPE or MBP can be set to 0 to abort the programming operation. When BPE = 1, the other bits in the IMS register must not be changed for two frames to ensure proper operation.
3	OSB	**Output standby.** When ODE = 0 and OSB = 0, the output drivers of STo0 to STo15 are in high impedance mode. When ODE = 0 and OSB = 1, the output driver of STo0 to STo15 function normally. When ODE = 1, STo0 to STo15 output drivers function normally.
2	SFE	**Start Frame Evaluation.** A zero to one transition in this bit starts the frame evaluation procedure. When the CFE bit in the FAR register changes from zero to one, the evaluation procedure stops. To start another frame evaluation cycle, set this bit to zero for at least one frame.
1 - 0	DR1-0	**Data Rate Select.** Input/Output data rate selection. See Table 9 for detailed programming.

Table 8 - Interface Mode Selection (IMS) Register Bits

DR1	DR0	Data Rate Selected	Master Clock Required
0	0	2.048 Mb/s	4.096 MHz
0	1	4.096 Mb/s	8.192 MHz
1	0	8.192 Mb/s	16.384 MHz
1	1	Reserved	Reserved

Table 9 - Serial Data Rate Selection (16 input x 16 output)

Read Address: 02_H,
Reset Value: 0000_H.



Bit	Name	Description
15 - 13	Unused	Must be zero for normal operation.
12	CFE	**Complete Frame Evaluation.** When CFE = 1, the frame evaluation is completed and bits FD10 to FD0 bits contains a valid frame alignment offset. This bit is reset to zero, when SFE bit in the IMS register is changed from 1 to 0.
11	FD11	**Frame Delay Bit 11.** The falling edge of FE (or rising edge for GCI mode) is sampled during the CLK-high phase (FD11 = 1) or during the CLK-low phase (FD11 = 0). This bit allows the measurement resolution to 1/2 CLK cycle.
10 - 0	FD10-0	**Frame Delay Bits.** The binary value expressed in these bits refers to the measured input offset value. These bits are reset to zero when the SFE bit of the IMS register changes from 1 to 0. (FD10 = MSB, FD0 = LSB)

Table 10 - Frame Alignment (FAR) Register Bits

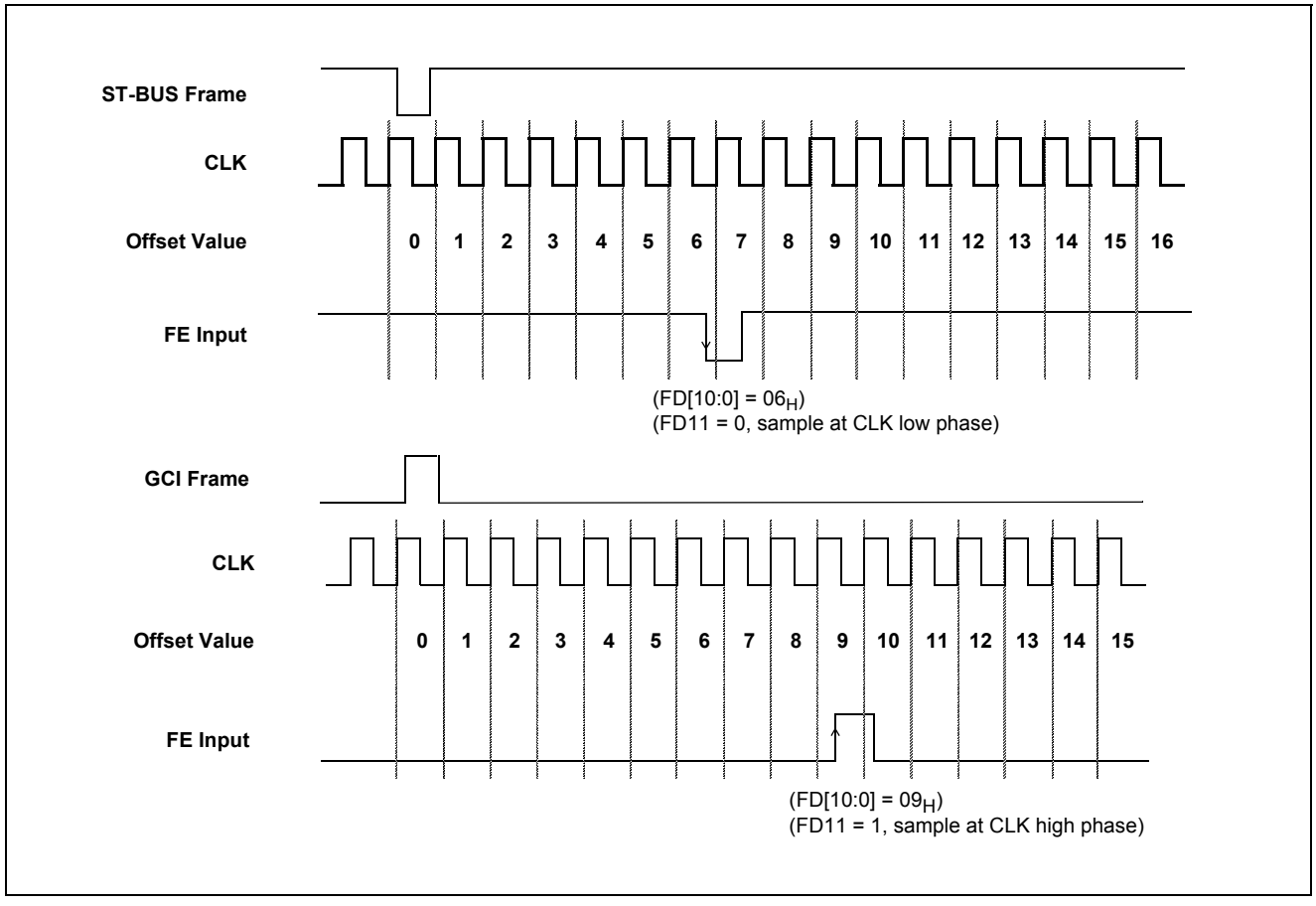
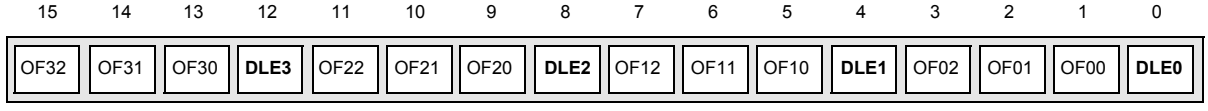


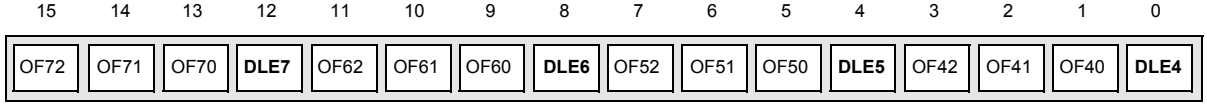
Figure 4 - Example for Frame Alignment Measurement

Read/Write Address: 03_H for FOR0 register,
04_H for FOR1 register,
05_H for FOR2 register,
06_H for FOR3 register,

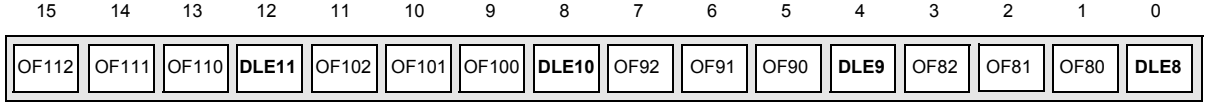
Reset value: 0000_H for all FOR registers.



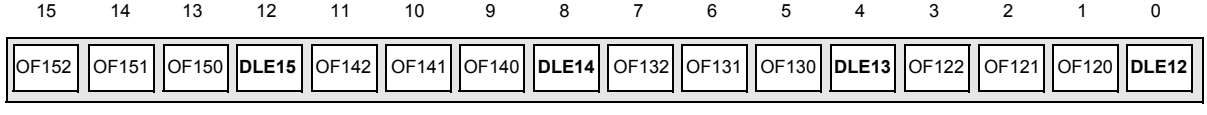
FOR0 register



FOR1 register



FOR2 register



FOR3 register

Name (Note 1)	Description
OFn2, OFn1, OFn0	**Offset Bits 2,1 & 0.** These three bits define how long the serial interface receiver takes to recognize and store bit 0 from the STi input pin: i.e., to start a new frame. The input frame offset can be selected to +4 clock periods from the point where the external frame pulse input signal is applied to the F0i input of the device. See Figure 4.
DLEn	Data Latch Edge. ST-BUS mode:DLEn =0, if clock rising edge is at the 3/4 point of the bit cell. DLEn =1, if when clock falling edge is at the 3/4 of the bit cell. GCI mode:DLEn =0, if clock falling edge is at the 3/4 point of the bit cell. DLEn =1, if when clock rising edge is at the 3/4 of the bit cell.
Note 1: n denotes an input stream number from 0 to 15.	

Table 11 - Frame Input Offset (FOR) Register Bits

Input Stream Offset	Measurement Result from Frame Delay Bits				Corresponding Offset Bits			
	FD11	FD2	FD1	FD0	OFn2	OFn1	OFn0	DLEn
No clock period shift (Default)	1	0	0	0	0	0	0	0
+ 0.5 clock period shift	0	0	0	0	0	0	0	1
+1.0 clock period shift	1	0	0	1	0	0	1	0
+1.5 clock period shift	0	0	0	1	0	0	1	1
+2.0 clock period shift	1	0	1	0	0	1	0	0
+2.5 clock period shift	0	0	1	0	0	1	0	1
+3.0 clock period shift	1	0	1	1	0	1	1	0
+3.5 clock period shift	0	0	1	1	0	1	1	1
+4.0 clock period shift	1	1	0	0	1	0	0	0
+4.5 clock period shift	0	1	0	0	1	0	0	1

Table 12 - Offset Bits (OFn2, OFn1, OFn0, DLEn) and Frame Delay Bits (FD11, FD2-0)

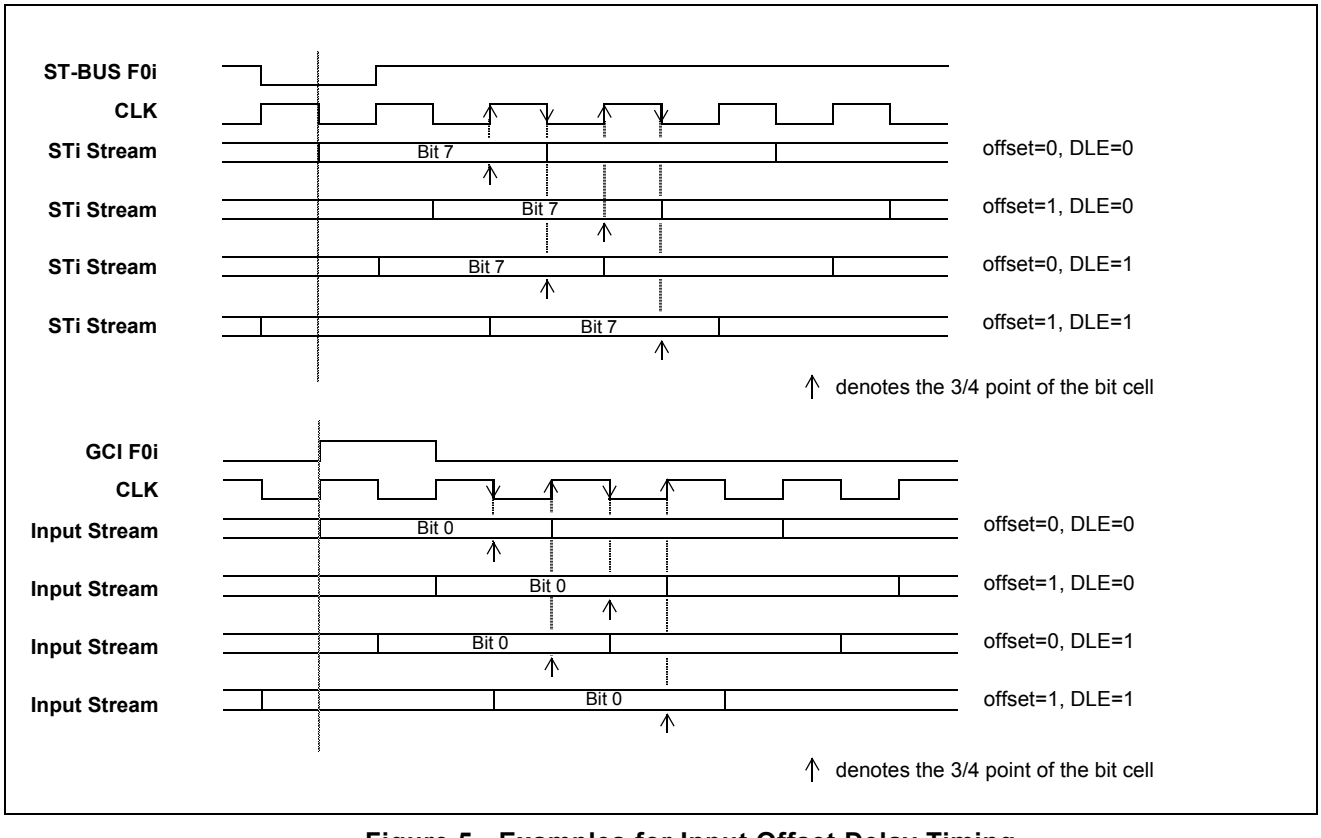
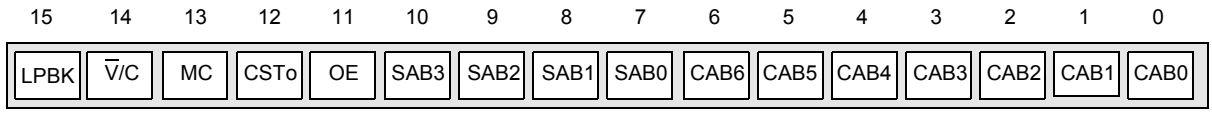


Figure 5 - Examples for Input Offset Delay Timing



Bit	Name	Description
15	LPBK	**Per Channel Loopback.** This bit should be use for diagnostic purpose only. Set this bit to zero for normal operation. When loopback bit is set for all memory location, the STi *n* channel *m* data comes from STo *n* channel *m*. For proper per channel loopback operations, set the delay offset register bits OFn[2:0] to zero for the streams which are in the loopback mode.
14	$\overline{V}$/C	**Variable /Constant Throughput Delay.** This bit is used to select between the variable (low) and the constant delay (high) modes on a per-channel basis.
13	MC	**Message Channel.** When 1, the contents of the connection memory are output on the corresponding output channel and stream. Only the lower byte (bit 7 - bit 0) will be output to the ST-BUS output pins. When 0, the contents of the connection memory are the data memory address of the switched input channel and stream.
12	CSTo	**Control ST-BUS output.** This bit is output on the CSTo pin one channel early. The CSTo bit for stream 0 is output first.
11	OE	**Output Enable.** This bit enables the ST-BUS output drivers on a per-channel basis. When 1, the output driver functions normally. When 0, the output driver is in a high-impedance state.
10 - 8, 7 (Note 1)	SAB3-0	**Source Stream Address Bits.** The binary value is the number of the data stream for the source of the connection.
6 - 0 (Note 1)	CAB6-0	**Source Channel Address Bits.** The binary value is the number of the channel for the source of the connection.

Note 1: If bit 13 (MC) of the corresponding connection memory location is 1 (device in message mode), then these entire 8 bits (SAB0, CAB6 - CAB0) are output on the output channel and stream associated with this location.

Table 13 - Connection Memory Bits

Data Rate	CAB Bits Used to Determine the Source Channel of the Connection
2.048 Mb/s	CAB4 to CAB0 (32 channel/input stream)
4.096 Mb/s	CAB5 to CAB0 (64 channel/input stream)
8.192 Mb/s	CAB6 to CAB0 (128 channel/input stream)

Table 14 - CAB Bits Programming for Different Data Rates

JTAG Support

The MT90823 JTAG interface conforms to the IEEE 1149.1 Boundary-Scan standard and the Boundary-Scan Test (BST) design-for-testability technique it specifies. The operation of the boundary-scan circuitry is controlled by an external test access port (TAP) Controller.

Test Access Port (TAP)

The Test Access Port (TAP) provides access to the many test functions of the MT90823. It consists of three input pins and one output pin. The following pins comprise the TAP.

- **Test Clock Input** (TCK)
  TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.

- **Test Mode Select Input** (TMS)
  The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to Vdd when it is not driven from an external source.

- **Test Data Input** (TDI)
  Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to Vdd when it is not driven from an external source.

- **Test Data Output** (TDO)
  Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high impedance state.

- **Test Reset** ($\overline{\text{TRST}}$)
  Resets the JTAG scan structure. This pin is internally pulled to VDD.

Instruction Register

In accordance with the IEEE 1149.1 standard, the MT90823 uses public instructions. The MT90823 JTAG Interface contains a three-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current, and to define the serial test data register path, which is used to shift data between TDI and TDO during data register scanning.

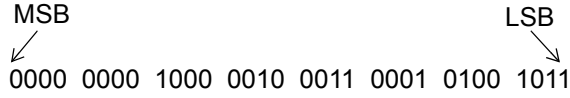
Test Data Register

As specified in IEEE 1149.1, the MT90823 JTAG Interface contains three test data registers:

- **The Boundary-Scan Register**
  The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the MT90823 core logic.

- **The Bypass Register**
  The Bypass register is a single stage shift register that provides a one-bit path from TDI to its TDO.

- **The Device Identification Register**
  The device identification register is a 32-bit register with the register contain of:



The LSB bit in the device identification register is the first bit clocked out.

The MT90823 boundary scan register contains 118 bits. Bit 0 in Table 15 Boundary Scan Register is the first bit clocked out. All tristate enable bits are active high.

Device Pin	Boundary Scan Bit 0 to Bit 117		
	Tristate Control	Output Scan Cell	Input Scan Cell
STo7	0	1	
STo6	2	3	
STo5	4	5	
STo4	6	7	
STo3	8	9	
STo2	10	11	
STo1	12	13	
STo0	14	15	
ODE			16
CSTo	17	18	
DTA		19	
D15	20	21	22
D14	23	24	25
D13	26	27	28
D12	29	30	31
D11	32	33	34
D10	35	36	37
D9	38	39	40
D8	41	42	43
AD7	44	45	46
AD6	47	48	49
AD5	50	51	52
AD4	53	54	55
AD3	56	57	58
AD2	59	60	61
AD1	62	63	64
AD0	65	66	67
IM			68
AS/ALE			69
CS			70
R/$\overline{W}$ / $\overline{WR}$			71
DS/$\overline{RD}$			72

Table 14 - Boundary Scan Register Bits

Device Pin	Boundary Scan Bit 0 to Bit 117		
	Tristate Control	Output Scan Cell	Input Scan Cell
A7			73
A6			74
A5			75
A4			76
A3			77
A2			78
A1			79
A0			80
WFPS			81
RESET			82
CLK			83
FE/HCLK			84
F0i			85
STi15			86
STi14			87
STi13			88
STi12			89
STi11			90
STi10			91
STi9			92
STi8			93
STi7			94
STi6			95
STi5			96
STi4			97
STi3			98
STi2			99
STi1			100
STi0			101
STo15	102	103	
STo14	104	105	
STo13	106	107	
STo12	108	109	
STo11	110	111	
STo10	112	113	
STo9	114	115	
STo8	116	117	

Table 14 - Boundary Scan Register Bits (continued)

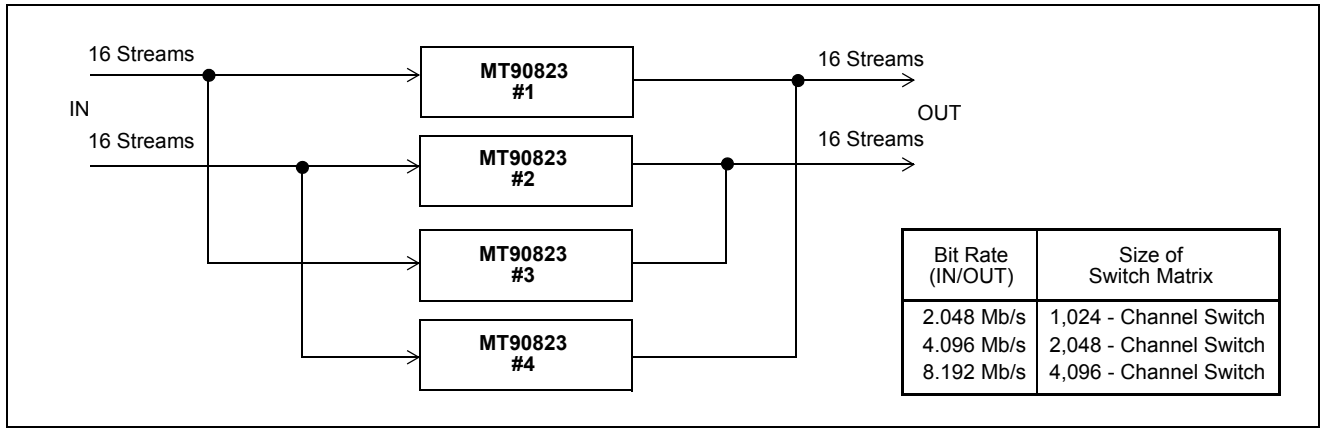
Applications

Switch Matrix Architectures

The MT90823 is an ideal device for medium to large size switch matrices where voice and grouped data channels are transported within the same frame. In such applications, the voice samples have to be time interchanged with a minimum delay while maintaining the integrity of grouped data. To ensure the integrity of grouped data during switching and to provide a minimum delay for voice connections, the MT90823 provides per-channel selection between variable and constant throughput delay. This can be selected by the $\overline{V}$/C bit of the Connection Memory. Figure 6 illustrates how four MT90823 devices can be used to form non-blocking switches for up to 4096 channels with data rate of 8.192 Mb/s.

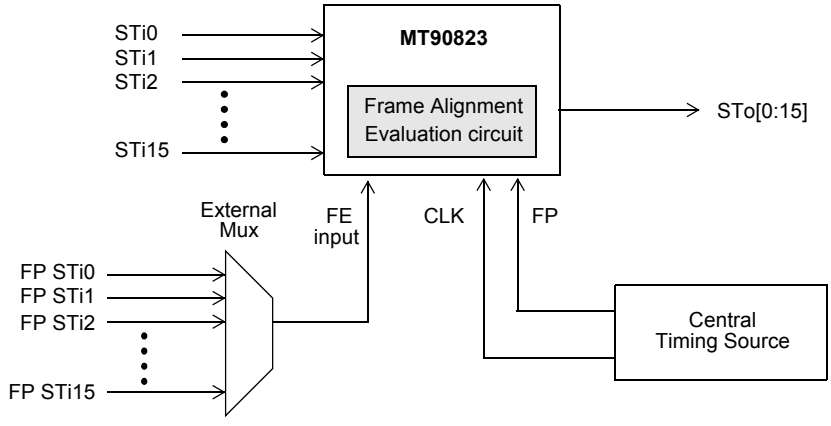
Serial Input Frame Alignment Evaluation

The MT90823 is capable of performing frame alignment evaluation. The frame pulse under evaluation is connected to the FE (frame measurement) pin. An external multiplexer is required to select one of the frame pulses related to the different input streams. Figure 7 - The block diagram at Figure 7 shows a switch matrix that performs frame alignment evaluation for 16 frame pulses.



Bit Rate (IN/OUT)	Size of Switch Matrix
2.048 Mb/s	1,024 - Channel Switch
4.096 Mb/s	2,048 - Channel Switch
8.192 Mb/s	4,096 - Channel Switch

Figure 6 - Switch Matrix with Serial Stream at Various Bit Rates



Note:
1. Use the external mux to select one of the serial frame pulses.
2. To start a measurement cycle, set the Start Frame Evaluation (SFE) bit in the IMS register low for at least 1 frame.
3. Frame evaluation starts when the SFE bit is changed from low to high.
4. Two frames later, the Complete Frame Evaluation (CFE) bit of the Frame Alignment Register (FAR) changes from low to high to signal the CPU that a valid offset measurement is ready to be read from bit [11:0] of the FAR register.
5. The SFE bit must be set to zero before a new measurement cycle started.

Figure 7 - Serial Input Frame Alignment Evaluation for Various Frame Pulses

Wide Frame Pulse (WFP) Frame Alignment Mode

When the device is in the wide frame pulse mode and if the input data streams are sampled at 3/4 bit time, the device can operate in the HMVIP and MVIP-90 environment. When input data streams are sampled at half-bit time as specified in the HMVIP and MVIP-90 standard, the device can only operate with data rate of 2 Mb/s. Refer to the ST-BUS output delay parameter, t_{SOD}, as specified in the AC Electrical Characteristic table.

The MT90823 is designed to accept a common frame pulse F0i, the 4.096 MHz and 16.384 MHz clocks required by the HMVIP standards. To enable the Wide Frame Pulse Frame Alignment Mode, the WFPS pin has to be set to HIGH and the DR1 and DR0 bits set for 8.192M b/s data rate operation.

Digital Access Cross-Connect System

Figure 8 illustrates the use of MT90823 devices to construct a 256 E1/T1 Digital Access Cross- connect System (DACS). The system consists of 32 trunk cards each having eight E1 or T1 trunk interfaces for a total of 256 trunks. Each trunk card uses two MT8986 Multi-rate Digital Switches. The central switching block uses 16 MT90823 devices.

The block diagram at Figure 9 shows how an 8,192 x 8,192 channel switch can be constructed from 4,096 x 4,096 channel switch modules. Figure 6 shows the implementation of the individual 4,096 x 4,096 channel switch modules from four MT90823 devices.

Figure 10 shows an eight-stream trunk card using MT8986 Multi-rate Digital Switches to concentrate 32-channel 2.048 Mb/s ST-BUS (DSTi and DSTo) streams at each E1/T1 trunk onto four 128-channel 8.192 Mb/s streams.

The DACS switching matrix that formerly required 256 MT8986 devices in a square (16 x 16) configuration can now be provided by 64 MT8986 and 16 MT90823 devices (see Figure 8).

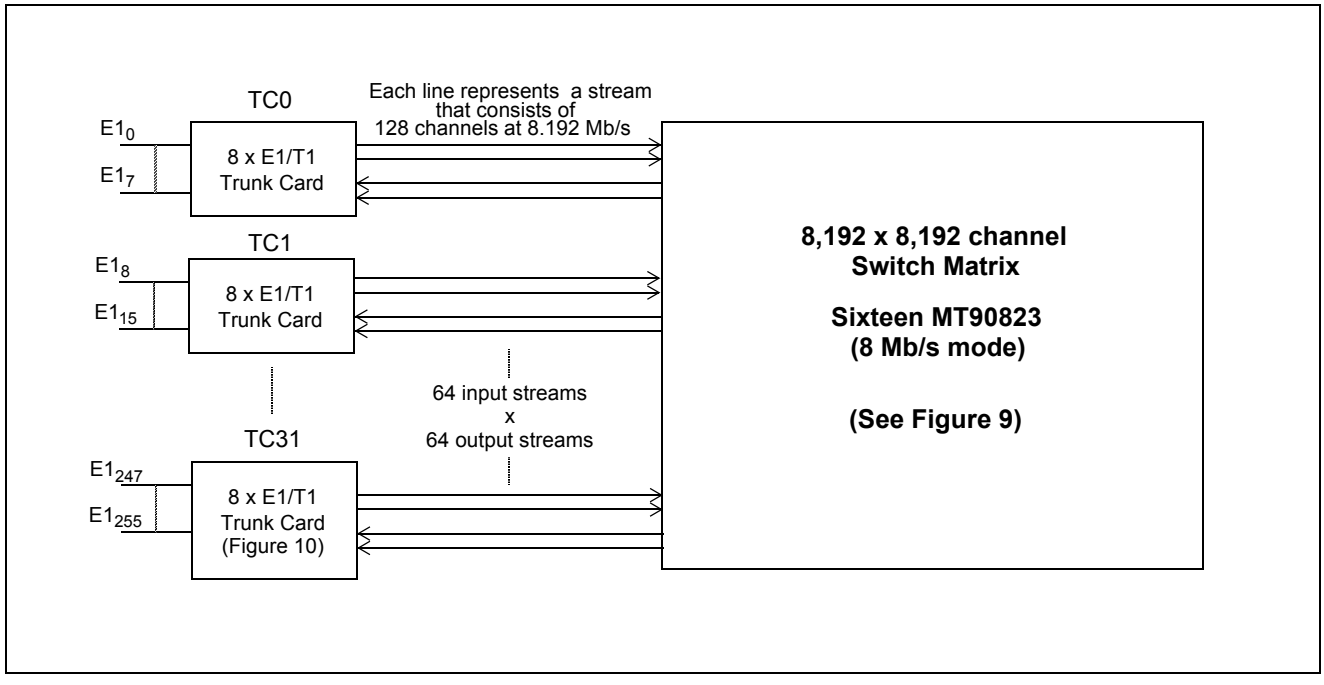


Figure 8 - 256 E1/T1 Digital Access Cross-Connect System (DACS)

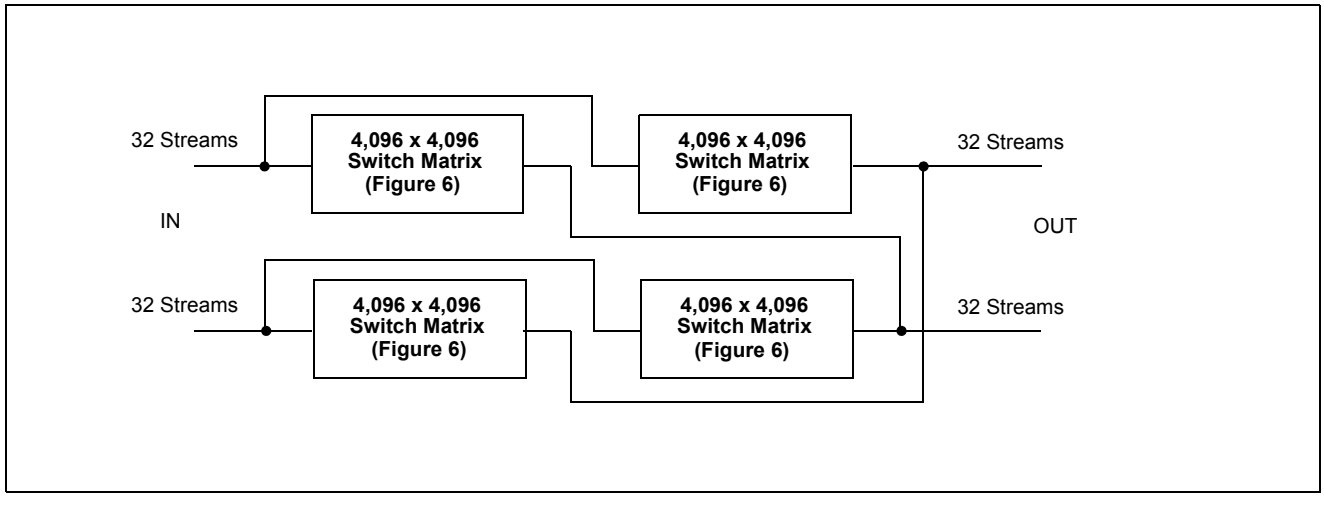


Figure 9 - 8,192 x 8,192 Channel Switch Matrix

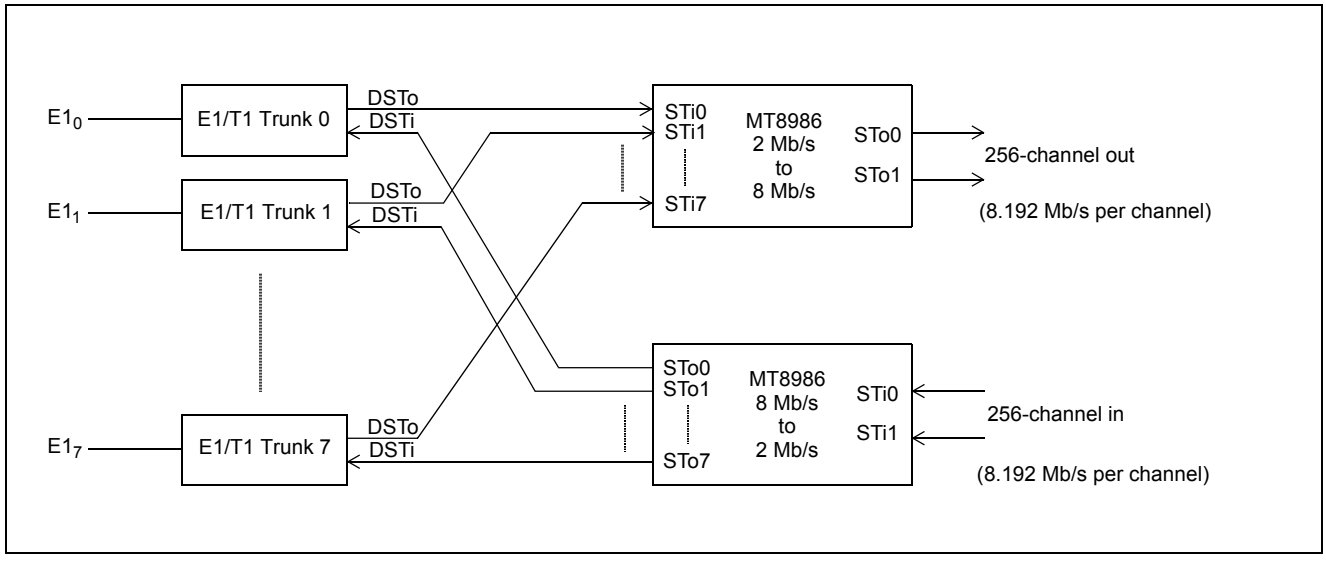


Figure 10 - Trunk Card Block Diagram

Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Max.	Units
1	Supply Voltage	V_{DD}	-0.3	5.0	V
2	Voltage on any 3.3 V Tolerant pin I/O (other than supply pins)	V_I	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Voltage on any 5 V Tolerant pin I/O (other than supply pins)	V_I	V_{SS} - 0.3	5.5	V
4	Continuous Current at digital outputs	I_o		20	mA
5	Package power dissipation (PLCC & PQFP)	P_D		1	W
6	Storage temperature	T_S	- 65	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied

Recommended Operating Conditions - Voltages are with respect to ground (V_{ss}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		+85	°C	
2	Positive Supply	V_{DD}	3.0		3.6	V	
3	Input High Voltage	V_{IH}	$0.7V_{DD}$		V_{DD}	V	400 mV noise margin
4	Input High Voltage on 5 V Tolerant Inputs	V_{IH}			5.5	V	
5	Input Low Voltage	V_{IL}	V_{SS}		$0.3V_{DD}$	V	400 mV noise margin

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics		Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	INPUTS	Supply Current	@ 2 Mb/s	I_{DD}		12	15	mA	Output unloaded
			@ 4 Mb/s			20	26	mA	
			@ 8 Mb/s			45	70	mA	
2		Input High Voltage		V_{IH}	$0.7V_{DD}$			V	
3		Input Low Voltage		V_{IL}			$0.3V_{DD}$	V	
4		Input Leakage (input pins) Input Leakage (with pull-up or pull-down)		I_{IL} I_{BL}			15 50	µA µA	$0 \leq < V \leq V_{DD}$ See Note 1
5		Input Pin Capacitance		C_I			10	pF	
6	OUTPUTS	Output High Voltage		V_{OH}	$0.8V_{DD}$			V	I_{OH} = -10 mA
7		Output Low Voltage		V_{OL}			0.4	V	I_{OL} = 10 mA
8		High Impedance Leakage		I_{OZ}			5	µA	$0 < V < V_{DD}$ See Note 1
9		Output Pin Capacitance		C_O			10	pF	

Note:
1. Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V)

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{CT}	$0.5V_{DD}$	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD}$	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD}$	V	

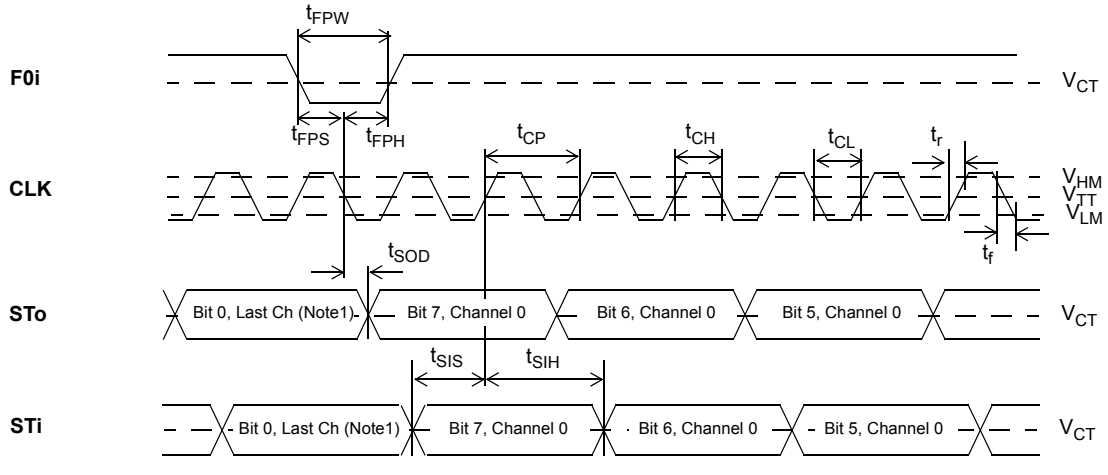
AC Electrical Characteristics - Frame Pulse and CLK

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	Frame pulse width (ST-BUS, GCI) Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{FPW}	 26 26 26		 295 145 80	 ns ns ns	WFPS Pin = 0
2	Frame Pulse Setup time before CLK falling (ST-BUS or GCI)	t_{FPS}	5			ns	WFPS Pin = 0
3	Frame Pulse Hold Time from CLK falling (ST-BUS or GCI)	t_{FPH}	10			ns	WFPS Pin = 0
4	CLK Period Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{CP}	 190 110 55		 300 150 70	 ns ns ns	WFPS Pin = 0
5	CLK Pulse Width High Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{CH}	 85 50 20		 150 75 40	 ns ns ns	WFPS Pin = 0
6	CLK Pulse Width Low Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{CL}	 85 50 20		 150 75 40	 ns ns ns	WFPS Pin = 0
7	Clock Rise/Fall Time	t_r, t_f			10	ns	
8	Wide frame pulse width Bit rate = 8.192 Mb/s	t_{HFPW}	195		295	ns	WFPS Pin = 1
9	Frame Pulse Setup Time before HCLK falling	t_{HFPS}	5		150	ns	WFPS Pin = 1
10	Frame Pulse Hold Time from HCLK falling	t_{HFPH}	10		150	ns	WFPS Pin = 1
11	HCLK (4.096MHz) Period Bit rate = 8.192 Mb/s	t_{HCP}	190		300	ns	WFPS Pin = 1
12	HCLK (4.096MHz) Pulse Width High Bit rate = 8.192 Mb/s	t_{HCH}	85		150	ns	WFPS Pin = 1
13	HCLK (4.096MHz) Pulse Width Low Bit rate = 8.192 Mb/s	t_{HCL}	85		150	ns	WFPS Pin = 1
14	HCLK Rise/Fall Time	t_{Hr}, t_{Hf}			10	ns	
15	Delay between falling edge of HCLK and falling edge of CLK	t_{DIF}	-10		10	ns	WFPS Pin = 0 or 1

AC Electrical Characteristics - Serial Streams for ST-BUS and GCI Backplanes

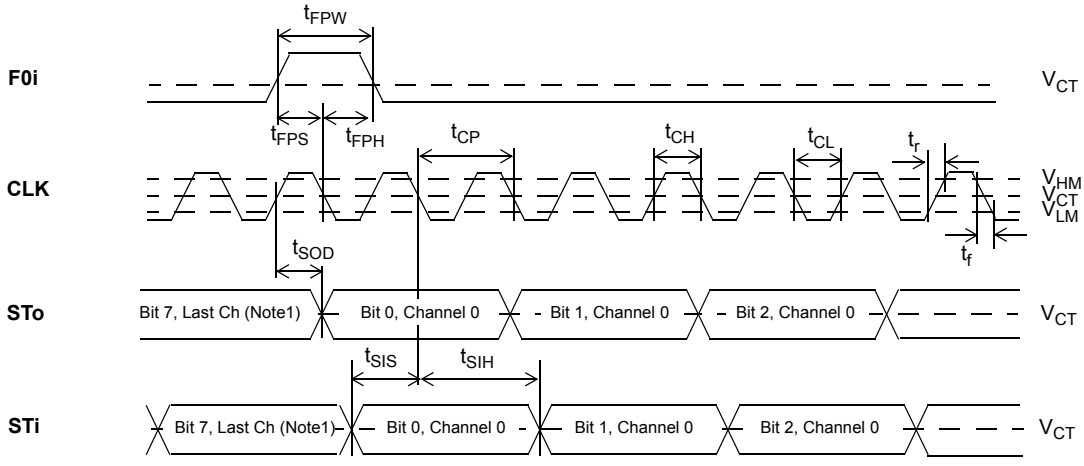
	Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Sti Set-up Time	t_{SIS}	0			ns	
2	Sti Hold Time	t_{SIH}	10			ns	
3	Sto Delay - Active to Active	t_{SOD}			30 40	ns ns	C_L=30pF C_L=200pF
4	STo delay - Active to High-Z	t_{DZ}			32		R_L=1K, C_L=200pF, See Note 1
5	Sto delay - High-Z to Active	t_{ZD}			32		R_L=1K, C_L=200pF, See Note 1
6	Output Driver Enable (ODE) Delay	t_{ODE}			32	ns	R_L=1K, C_L=200pF, See Note 1
7	CSTo Output Delay	t_{XCD}			30 40	ns ns	C_L=30pF C_L=200pF

Note:
1. High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.



Note 1:
2.048 Mb/s mode, last channel = ch 31,
4.196 Mb/s mode, last channel = ch 63,
8.192 Mb/s mode, last channel = ch 127.

Figure 11 - ST-BUS Timing for 2.048 Mb/s and High Speed Serial Interface at 4.096 Mb/s or 8.192 Mb/s, when WFPS pin = 0.



Note 1:
2 Mb/s mode, last channel = ch 31,
4 Mb/s mode, last channel = ch 63,
8 Mb/s mode, last channel = ch 127

Figure 12 - GCI Timing at 2.048 Mb/s and High Speed Serial Interface at 4.096 Mb/s or 8.192 Mb/s, when WFPS pin = 0

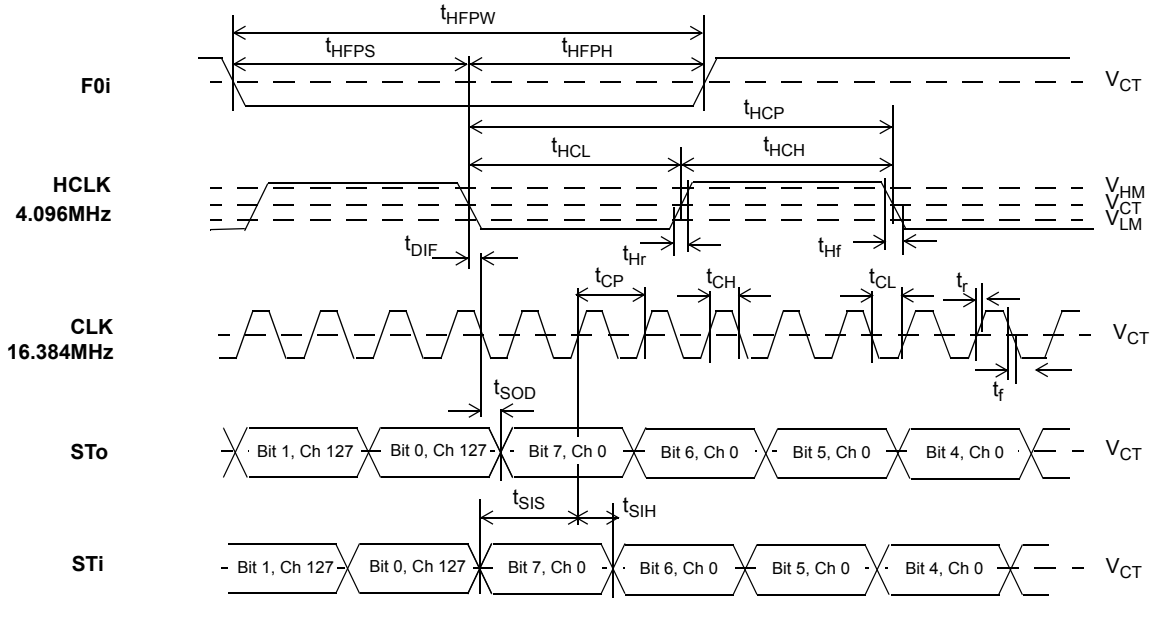


Figure 13 - WFP Bus Timing for High Speed Serial Interface (8.192 Mb/s), when WFPS pin = 1

Note:
1. High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

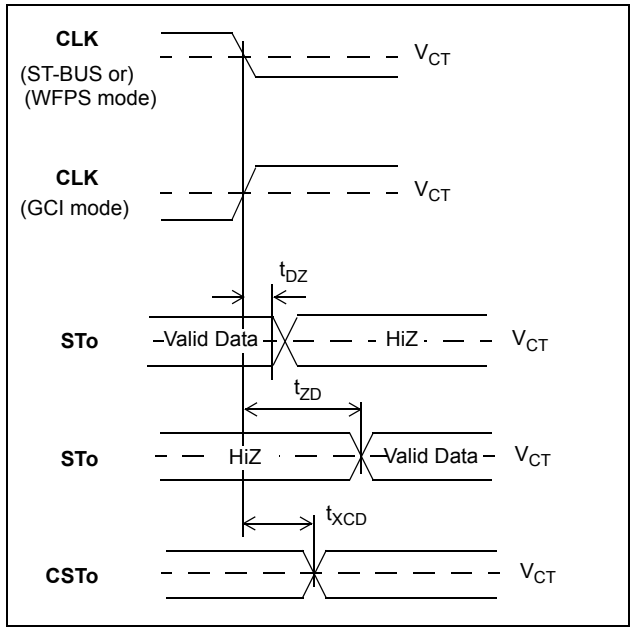


Figure 14 - Serial Output and External Control

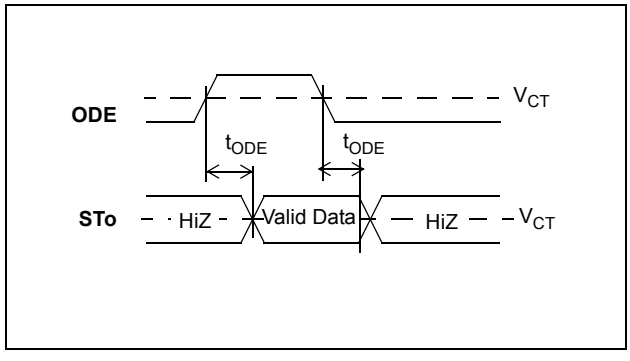


Figure 15 - Output Driver Enable (ODE)

AC Electrical Characteristics - Multiplexed Bus Timing (Mode 1)

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	ALE pulse width	t_{ALW}	20			ns	
2	Address setup from ALE falling	t_{ADS}	3			ns	
3	Address hold from ALE falling	t_{ADH}	3			ns	
4	$\overline{RD}$ active after ALE falling	t_{ALRD}	3			ns	
5	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	5			ns	C_L=150pF
6	$\overline{CS}$ hold after $\overline{RD}$/$\overline{WR}$	t_{CSRW}	5			ns	
7	$\overline{RD}$ pulse width (fast read)	t_{RW}	45			ns	
8	$\overline{CS}$ setup from $\overline{RD}$	t_{CSR}	0			ns	
9	Data hold after $\overline{RD}$	t_{DHR}	10		20	ns	C_L=150pF, R_L=1K, Note 1.
10	$\overline{WR}$ pulse width (fast write)	t_{WW}	45			ns	
11	$\overline{WR}$ delay after ALE falling	t_{ALWR}	3			ns	
12	$\overline{CS}$ setup from $\overline{WR}$	t_{CSW}	0			ns	
13	Data setup from $\overline{WR}$ (fast write)	t_{DSW}	20			ns	
14	Valid Data Delay on write (slow write)	t_{SWD}			122	ns	
15	Data hold after $\overline{WR}$ inactive	t_{DHW}	5			ns	
16	Acknowledgment Delay: Reading/Writing Registers Reading/Writing Memory @ 2Mb/s @ 4Mb/s @ 8Mb/s	t_{AKD}			 43/43 760/750 400/390 220/210	 ns ns ns ns	 C_L=150pF C_L=150pF C_L=150pF C_L=150pF
17	Acknowledgment Hold Time	t_{AKH}			22	ns	C_L=150pF, R_L=1K, Note 1.

Note:

1. High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

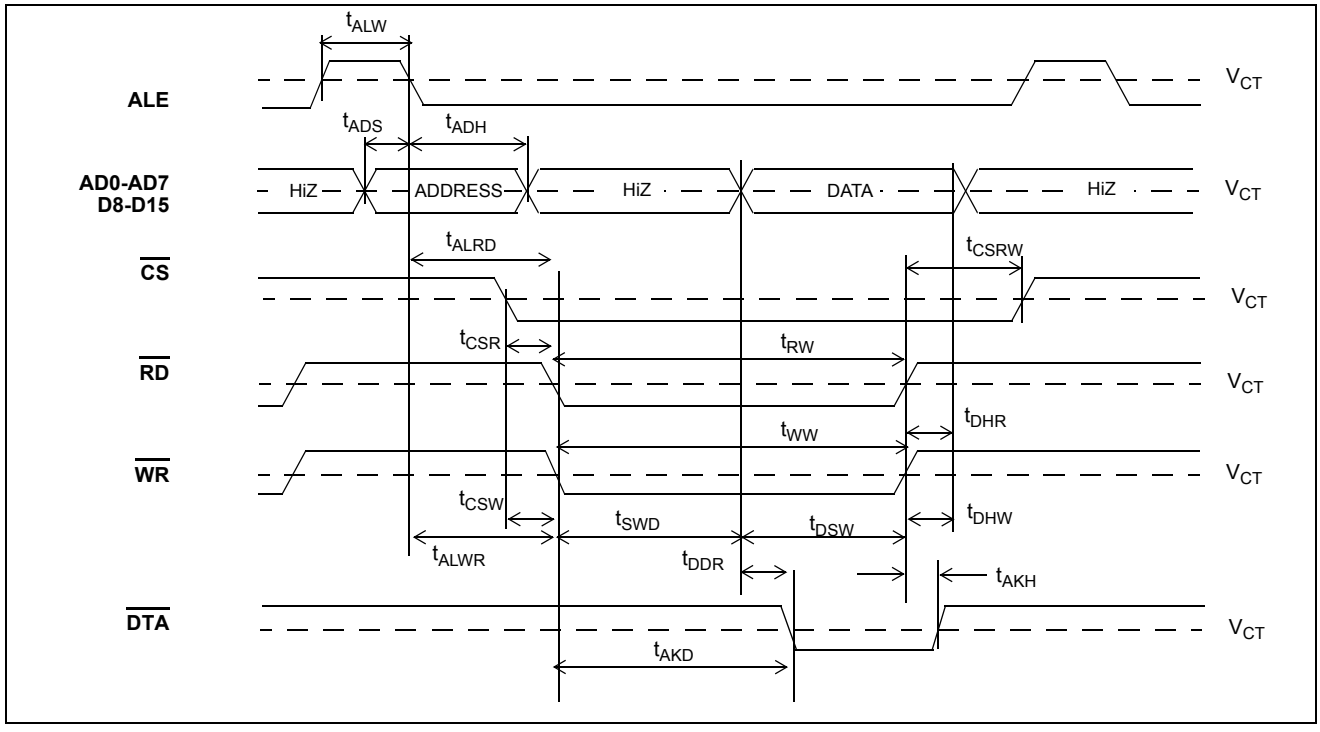


Figure 16 - Multiplexed Bus Timing (Mode 1)

AC Electrical Characteristics - Multiplexed Bus Timing (Mode 2)

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	AS pulse width	t_{ASW}	20			ns	
2	Address setup from AS falling	t_{ADS}	3			ns	
3	Address hold from AS falling	t_{ADH}	3			ns	
4	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	5			ns	C_L=150pF
5	$\overline{CS}$ hold after DS falling	t_{CSH}	0			ns	
6	$\overline{CS}$ setup from DS rising	t_{CSS}	0			ns	
7	Data hold after write	t_{DHW}	5			ns	
8	Data setup from DS -Write (fast write)	t_{DWS}	20			ns	
9	Valid Data Delay on write (slow write)	t_{SWD}			122	ns	
10	R/$\overline{W}$ setup from DS rising	t_{RWS}	60			ns	
11	R/$\overline{W}$ hold after DS falling	t_{RWH}	5			ns	
12	Data hold after read	t_{DHR}	10		20	ns	C_L=150pF, R_L=1K, Note 1
13	DS delay after AS falling	t_{DSH}	10			ns	
14	Acknowledgment Delay: Reading/Writing Registers Reading/Writing Memory @ 2Mb/s @ 4Mb/s @ 8Mb/s	t_{AKD}			 43/43 760/750 400/390 220/210	 ns ns ns ns	 C_L=150pF C_L=150pF C_L=150pF C_L=150pF
15	Acknowledgment Hold Time	t_{AKH}			22	ns	C_L=150pF, R_L=1K, Note 1

Note 1. High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

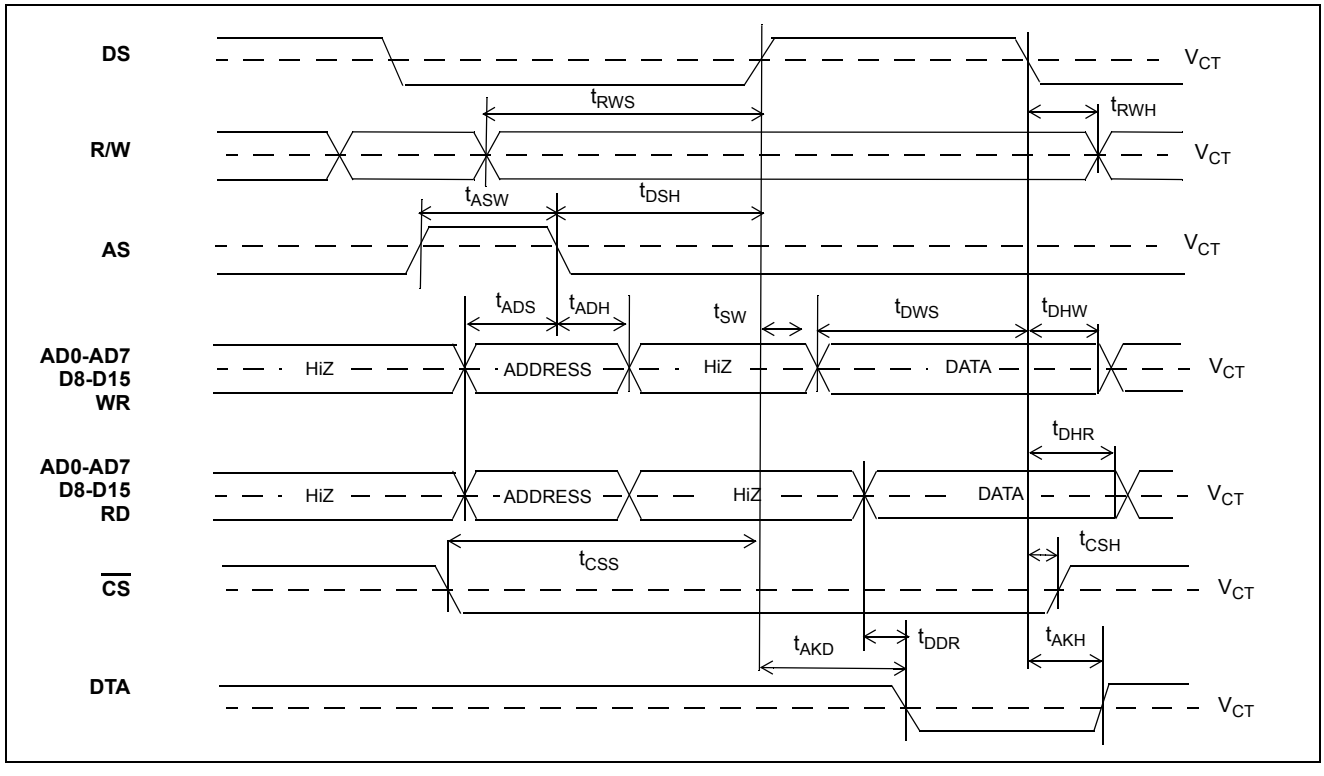


Figure 17 - Multiplexed Bus Timing (Mode2)

AC Electrical Characteristics - Motorola Non-Multiplexed Bus Mode

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	$\overline{CS}$ setup from DS falling	t_{CSS}	0			ns	
2	R/$\overline{W}$ setup from DS falling	t_{RWS}	10			ns	
3	Address setup from DS falling	t_{ADS}	2			ns	
4	$\overline{CS}$ hold after DS rising	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after DS rising	t_{RWH}	2			ns	
6	Address hold after DS rising	t_{ADH}	2			ns	
7	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	2			ns	C_L=150pF
8	Data hold on read	t_{DHR}	10		20	ns	C_L=150pF, R_L=1K Note 1
9	Data setup on write (fast write)	t_{DSW}	0			ns	
10	Valid Data Delay on write (slow write)	t_{SWD}			122	ns	
11	Data hold on write	t_{DHW}	5			ns	
12	Acknowledgment Delay: Reading/Writing Registers Reading/Writing Memory @ 2Mb/s @ 4Mb/s @ 8Mb/s	t_{AKD}			 43/43 760/750 400/390 220/210	 ns ns ns ns	 C_L=150pF C_L=150pF C_L=150pF C_L=150pF
13	Acknowledgment Hold Time	t_{AKH}			22	ns	C_L=150pF, R_L=1K, Note 1

Note:
1. High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

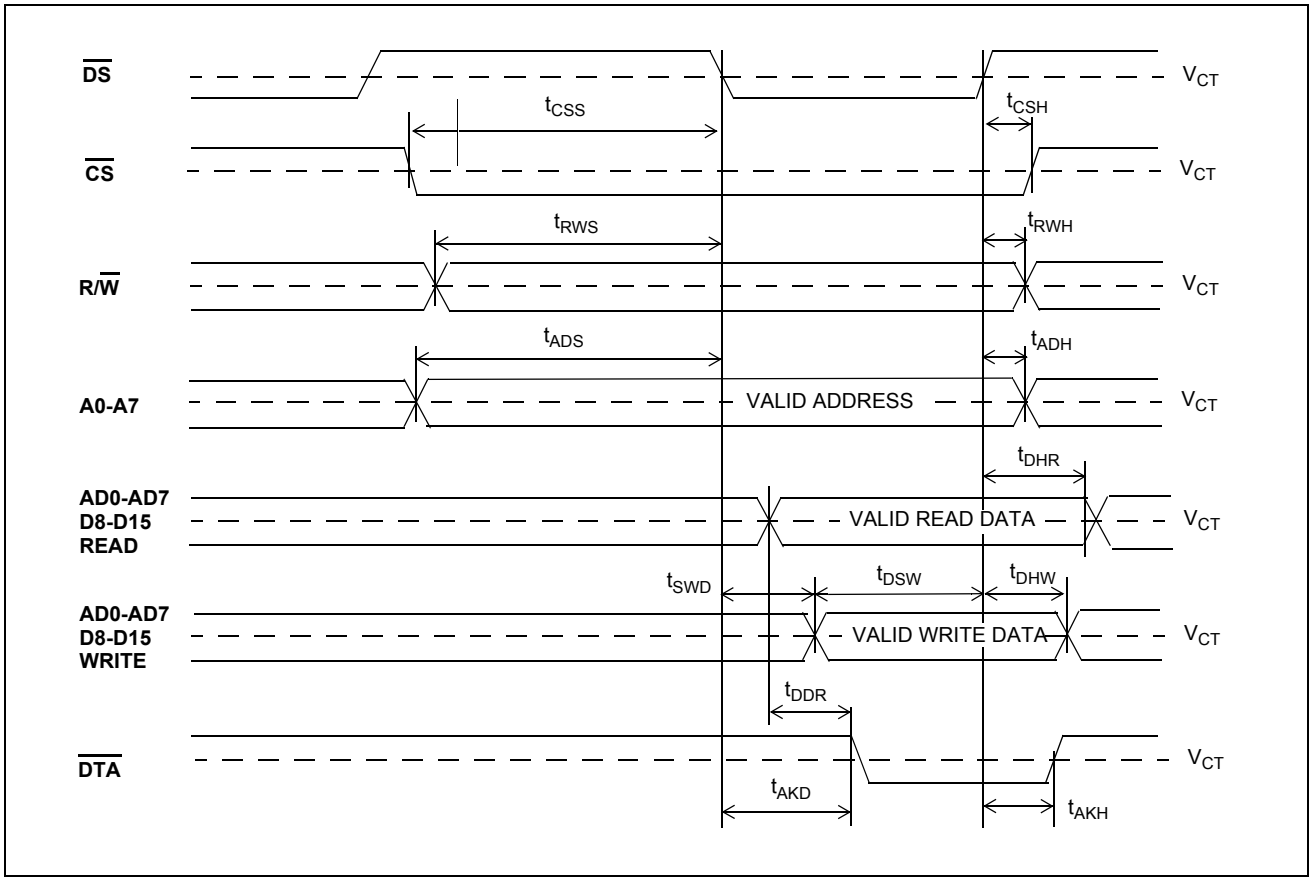
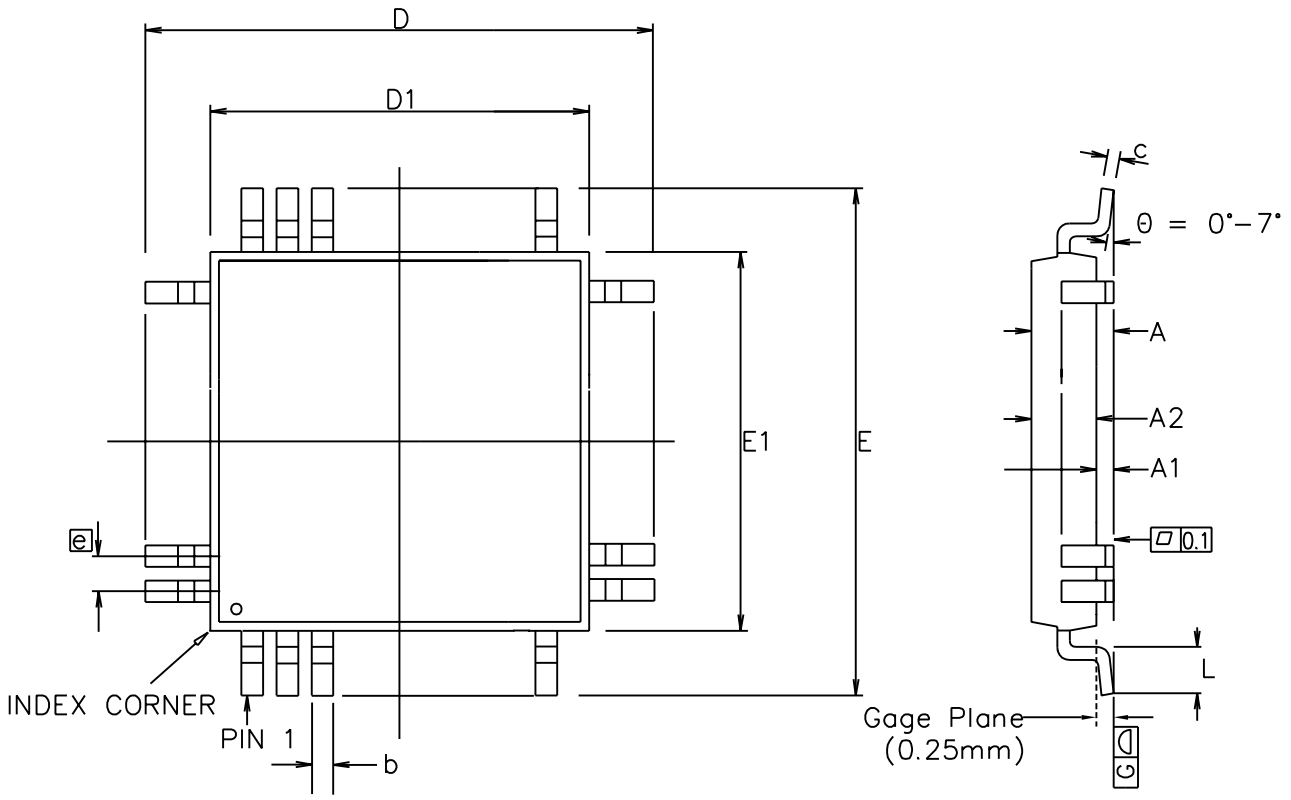


Figure 18 - Motorola Non-Multiplexed Bus Timing



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	– – –	3.40		– – –	0.134
A1	0.25	– – –		0.010	– – –
A2	2.55	3.05		0.100	0.120
D	23.90 BSC			0.941 BSC	
D1	20.00 BSC			0.787 BSC	
E	17.90 BSC			0.705 BSC	
E1	14.00 BSC			0.551 BSC	
L	0.73	1.03		0.029	0.041
e	0.65 BSC			0.026 BSC	
b	0.22	0.38		0.009	0.015
c	0.11	0.23		0.004	0.009
	Pin features				
N	100				
ND	30				
NE	20				
NOTE	RECTANGULAR				

Conforms to JEDEC MO-112 CC-1 Iss. B

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar prorusion.
6. Coplanarity, measured at seating plane G, to be 0.10 mm max.

This drawing supersedes 418/ED/51210/005 (Swindon)

ISSUE	2	3	4	5
ACN	203201	204759	207063	212834
DATE	20Oct97	24Jun98	1Jul99	21May02
APPRD.				

ZARLINK SEMICONDUCTOR

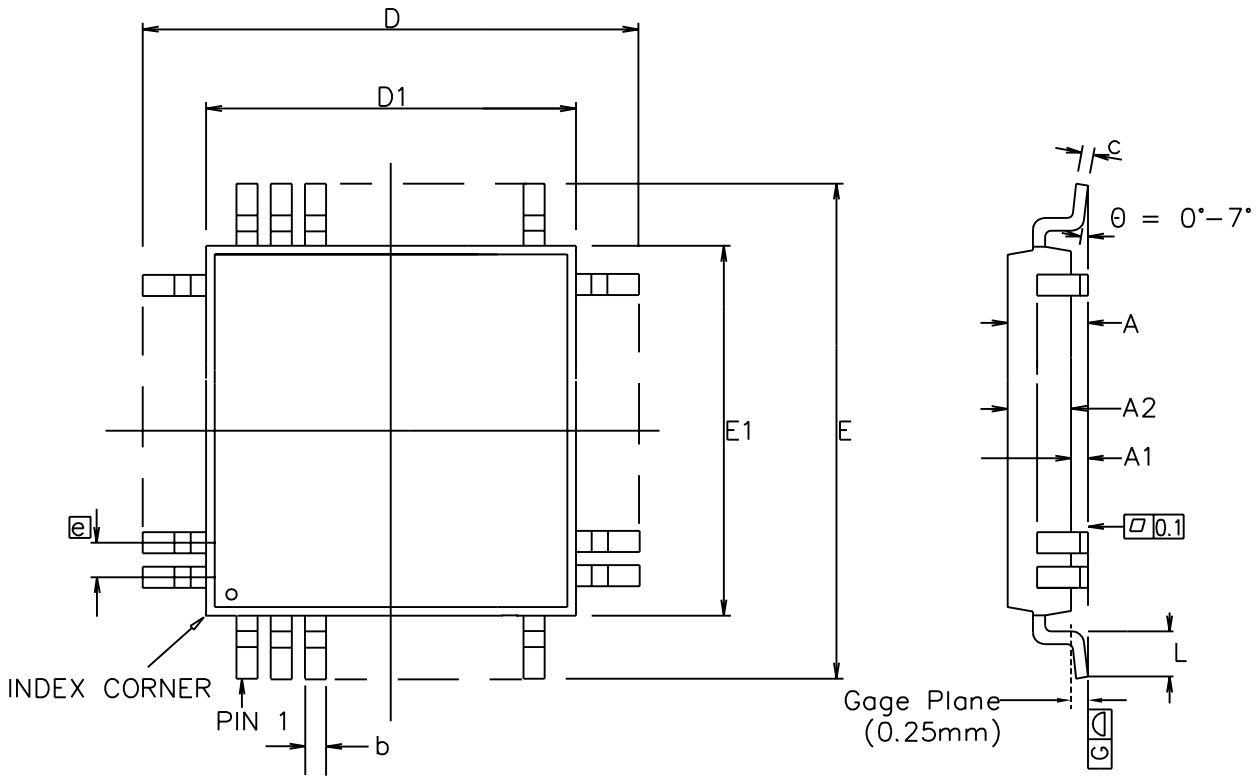
Previous package codes

GP / L

Package Code QB

Package Outline for 100 lead MQFP (14 x 20 x 2.8mm) 3.9mm Footprint

GPD00241



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	– – –	1.60		– – –	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	16.00 BSC			0.630 BSC	
D1	14.00 BSC			0.551 BSC	
E	16.00 BSC			0.630 BSC	
E1	14.00 BSC			0.551 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	100				
ND	25				
NE	25				
NOTE	SQUARE				

Conforms to JEDEC MS-026 BED Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

This drawing supersedes 418/ED/51210/023 (Swindon)

ISSUE	1	2	3	
ACN	201373	207144	212447	
DATE	29Oct96	15Jul99	26Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

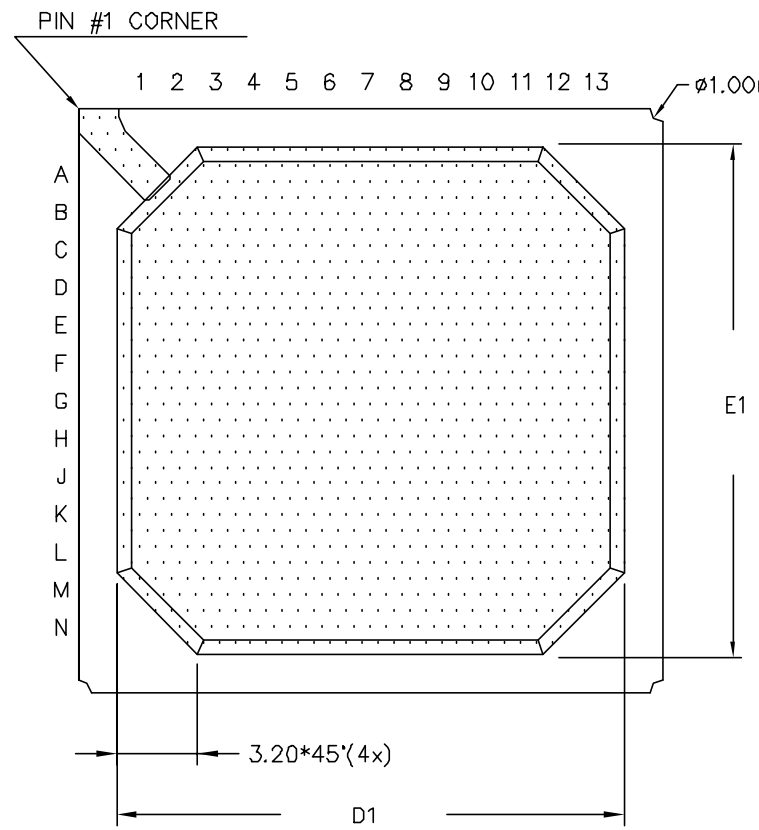
GP / B

Package Code QC

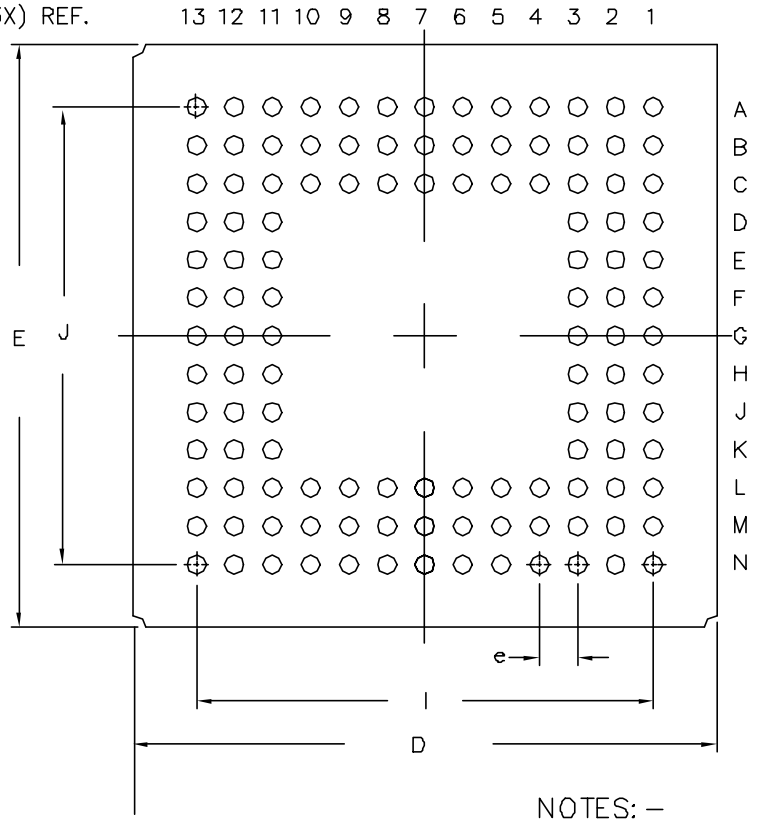
Package Outline for 100 lead LQFP (14 x 14 x 1.4mm) 2.0mm Footprint

GPD00253

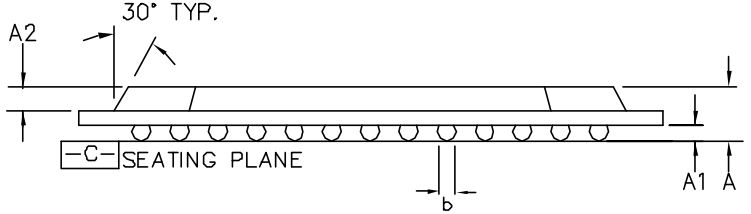
TOP VIEW



BOTTOM VIEW



DIMENSION	MIN	MAX
A	2.00	2.26
A1	0.50	0.70
A2	0.97 REF	
D	22.80	23.20
D1	20.00 REF	
E	22.80	23.20
E1	20.00 REF	
b	0.60	0.90
e	1.5	
N	120	
I	18.00	
J	18.00	
Substrate Layers: 2		
Reference spec: JEDEC MS-034		



SIDE VIEW

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.56 MM REF.

ISSUE	1			
ACN	213934			
DATE	20Jan03			
APPRD.				

ZARLINK SEMICONDUCTOR

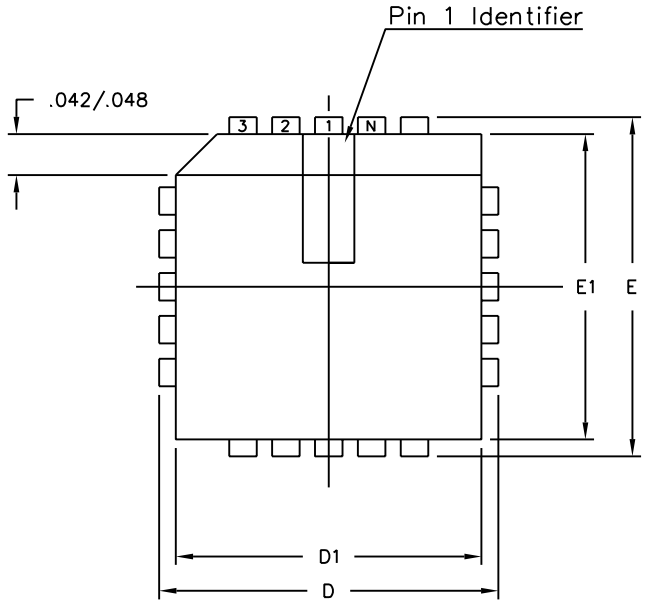
Previous package codes:

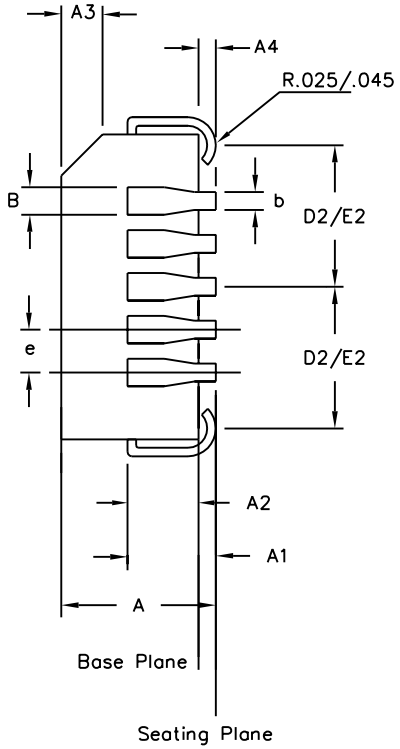
BP/G

Package Code : GA

Package Outline for
120Ball PBGA
23x23x2.13mm

GPD00820





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.059	0.080	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	1.185	1.195	30.10	30.35
D1	1.150	1.158	29.21	29.41
D2	0.541	0.569	13.74	14.45
E	1.185	1.195	30.10	30.35
E1	1.150	1.158	29.21	29.41
E2	0.541	0.569	13.74	14.45
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	21			
NE	21			
N	84			
Note	Square			
Conforms to JEDEC MS-018AF Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

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ZARLINK SEMICONDUCTOR

Previous package codes

HP / P

Package Code QA

Package Outline for 84 lead PLCC

GPD00006

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TECHNICAL DOCUMENTATION - NOT FOR RESALE