MH89626C

OPS/DID SLIC

Preliminary Information

ISSUE 3 May 1995

Features

- Transformerless 2-4 wire conversion
- Constant current with constant voltage fallback for long loops
- Long length capability (R_{Loop} > 1850Ω)
- Input impedance
- 200Ω + 560Ω // 0.1µF (MH89626C-02)
- 200Ω + 680Ω // 0.1µF (MH89626C-04)
- Ring trip filter with auto ring trip
- Three relay drivers
- Built-in Tip/Ring reversal capability on the hybrid
- Serial control interface
- External or software programmable receive gain, -3.5 or -7.0dB

Applications

- Off-Premise PBX Line Cards
- DID (Direct Inward Dial) Line Cards
- Central Office Line Cards

Ordering Information

MH89626C-02	38 Pin SIL Package
MH89626C-04	38 Pin SIL Package

0°C to 70°C

Description

The MH89626C SLIC provides all of the functions required to interface 2-wire off premise subscriber loops to a serial TDM, PCM, switching network of a modern PBX. The MH89626C is manufactured using thick film hybrid technology which offers high voltage capability, reliability and high density resulting in significant printed circuit board area saving of the line cards. A complete line card can be implemented with very few external components.

The SLIC has a simple serial control interface to control the receive gain setting, relay drivers for ringing, and Tip/Ring reversal for DID operation.

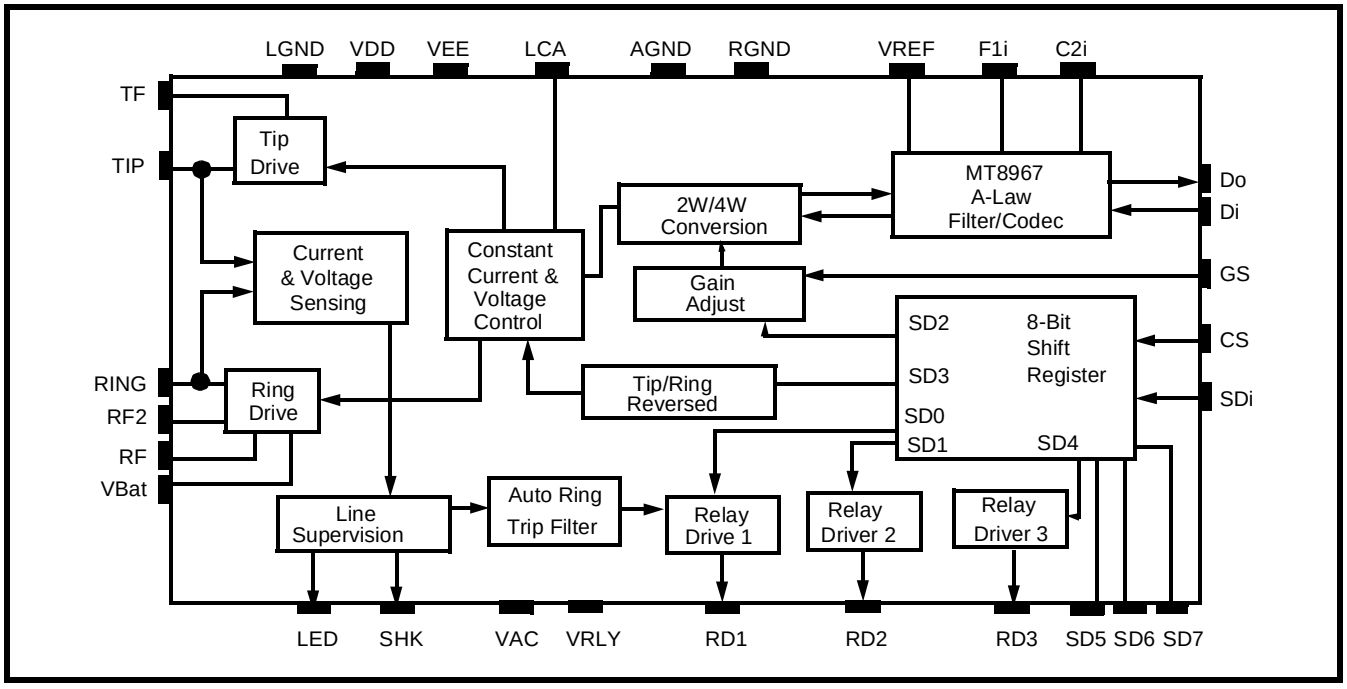

Figure 1 - Functional Block Diagram

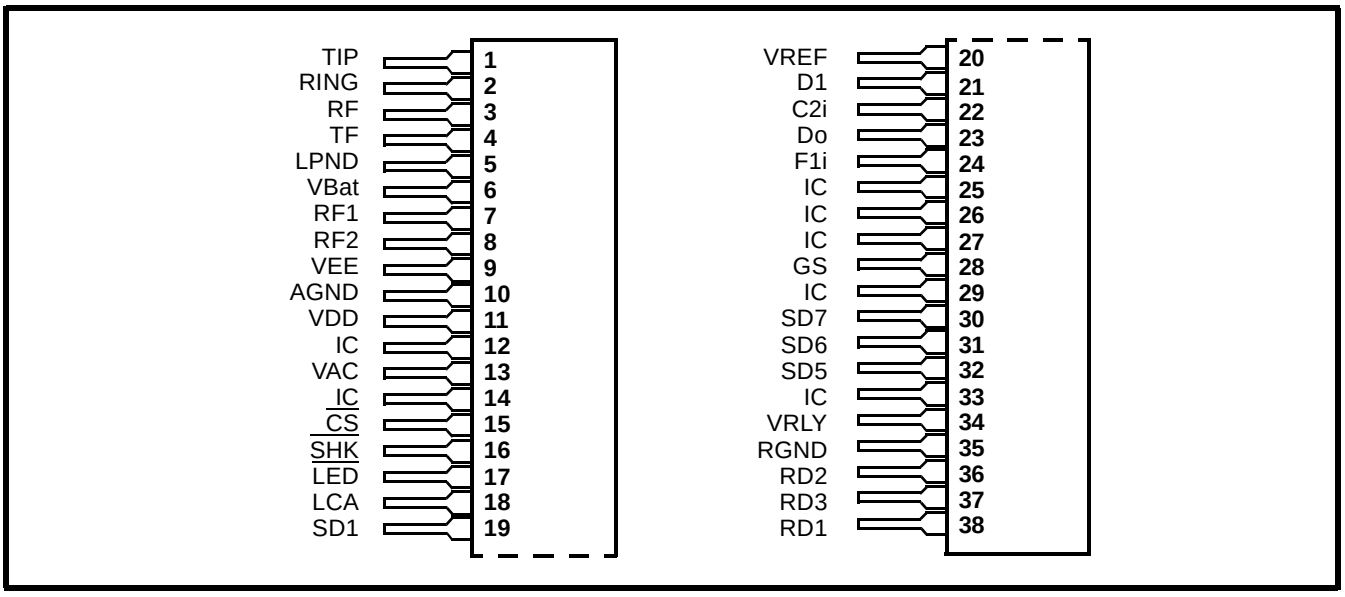

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	TIP	**Tip Lead:** Connects to the TIP lead of the telephone line.
2	RING	**Ring Lead:** Connects to the Ring lead of the telephone line.
3	RF	**Ring Feed**.
4	TF	**Tip Feed.**
5	LGND	**Loop Ground:** Return path for the battery (V_{Bat}) supply voltage. Connects to System Ground.
6	V_{Bat}	**Battery Supply Voltage:** Normally -48V.
7	RF1	**Ring Feed 1:** Ringing input.
8	RF2	**Ring Feed 2:** Ringing output.
9	V_{EE}	**Negative Supply Voltage.** (-5V)**.**
10	AGND	**Analog Ground:** Analog and Digital Ground. Connects to system ground.
11	V_{DD}	**Positive Supply Voltage.** (+5V).
12	IC	**Internal Connection.**
13	VAC	**Battery AC Component (input).** AC noise present in the V_{Bat} supply isolated from the DC components, can be applied to this pin to reduce longitudinal noise on TIP and RING. To implement this feature, connect a 0.1µF 100V capacitor from V_{Bat} to VAC, and 1kΩ resistor from VAC to AGND. This pin must be tied to AGND when not used.
14	IC	**Internal Connection.**
15	$\overline{CS}$	**Chip Select (Input):** A TTL compatible digital input to enable the SDi to control all the functions of the driver.
16	$\overline{SHK}$	**Switch Hook Detect (Output):** A logic low indicates an off-hook condition.
17	$\overline{LED}$	**LED Drive (Output).**: Drives an LED directly through an internal 2.2kΩ resistor. A logic low indicates an off-hook condition.
18	LCA	**Loop Current Adjust (input):** If this pin is left open, the constant current will be set at 23mA. The loop current can be adjusted by connecting a resistor to V_{EE}.

Pin Description (Continued)

Pin #	Name	Description
19	SDi	**Serial Data in (input):** A TTL compatible digital input. The 8-bit serial input enables the drivers. See Table 1 and Figure 3b.
20	V_{Ref}	**Voltage Reference (Input)** +2.5V for the internal codec.
21	Di	**Data in (Input).** A TTL compatible digital input which accepts the 8-bit PCM word from the incoming PCM bus.
22	C2i	**Clock input (input).** A TTl compatible digital input which accepts the 2048 kHz clock.
23	Do	**Data Out (Output)** A three state TTL compatible digital output which drives the 8-bit PCM word to the outgoing PCM bus.
24	$\overline{F1i}$	**Synchronization input (Input).** A TTL compatible, active low digital output input enabling the PCM input, PCM output and digital control input. It is internally sampled on every positive edge of the clock, C2i and provides frame and channel synchronization. See fig 3a.
25-27	IC	**Internal Connection**.
28	GS	**Gain setting (Input).** A logic '0' at this input will set the receiving gain to -7.0dB and a logic '1' will set the receiving gain to -3.5dB. If this pin is left open, the receiving gain can be set by SDi, bit 2.
29	IC	**Internal Connection.**
30	SD7	**Serial Data (Output).** A TTL compatible output coming from the SDi, bit 7. Bit inverted.
31	SD6	**Serial Data (Output).** A TTL compatible output coming from the SDi, bit 6. Bit inverted.
32	SD5	**Serial Data (Output).** A TTL compatible output coming from the SDi, bit 5. Bit inverted.
33	IC	**Internal Connection.**
34	V_{RLY}	**Relay Positive Supply Voltage.** Normally +5V. Connects to the relay coil and the relay supply voltage.
35	RGND	**Relay Ground.** Return path for relay supply voltage.
36	$\overline{RD2}$	**Relay Driver 2 (Output).** Connects to a user provided external relay coil. A logic '0' from the SDi, bit 1 will activate this driver. This relay driver is typically used for system in-test.
37	$\overline{RD3}$	**Relay Driver 3 (Output).** Connects to a user provided external relay coil. A logic '0' from the SDi, bit 4 will activate this driver. This relay driver is typically used for system in-test.
38	$\overline{RD1}$	**Relay Driver 1 (Output).** Connects to a user provided external relay coil. A logic '0' from the SDi, bit 0 will activate this driver. This relay driver is typically used for ringing.

Absolute Maximum Ratings*- All voltages are with respect to AGND unless otherwise specified.

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltage	V_{DD} V_{EE}	-0.3 0.3	7 -7	V V
2	DC Battery Voltages ①	V_{Bat}	0.3	-65	V
3	DC Ring Relay Voltage	V_{RLY}	-0.3	7	V
4	DC Reference Voltage	V_{REF}	-0.3	V_{DD}	V
5	AC Ring Generator Voltage			150	V_{RMS}
6	DC Digital Input Voltage	GS,SDi,Di, C2i,F1i	-0.3	V_{DD}	V
7	Storage Temperature	TS	-40	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

	Parameter	Symbol	Min	TYP*	Max	Units	Comments
1	DC Supply Voltage	V_{DD} V_{EE}	4.75 -4.75	5.0 -5.0	5.25 -5.25	V V	
2	DC Battery Voltage ①	V_{Bat}	-39.8	-48	-60	V	
3	DC Ring Relay Voltage	V_{RLY}		5.0	7.0	V	
4	DC Reference Voltage ②	V_{REF}	2.488	2.500	2.512	V	
5	AC Ring Generator Voltage Ringing Generator Frequency		22	90 25	130 28	V_{RMS} Hz	
6	Operating Temperature	T_{OP}	0	25	70	°C	

① LGND is connected to AGND

② Temperature coefficient of V_{REF} should be better than 100ppm/C

DC Electrical Characteristics*

		Characteristics	Sym	Min	Typ†	Max	Units	Test Comments
1		Supply and Battery Current ①	I_{DD} I_{EE}	5 5	12.5 11.7	15 15	mA mA	
		Short Loop	I_{Bat}		23.5	28	mA	R_{Loop} = 0Ω, LCA =Open
		Open Loop	I_{Bat}	0	1.5	2	mA	R_{Loop} = Open
2		Power Consumption	PC					
		On Hook (V_{Bat})				100	mW	R_{Loop} = Open
		Powerdown (V_{DD} and V_{EE})				150	mW	
		Off-Hook (V_{DD}, V_{EE}, V_{Bat})				1500	mW	R_{Loop} = 0Ω
3	V_{Ref}	DC Reference Voltage Mean Current			2		µA	
4	$\overline{SHK}$	Low Level Output Voltage High Level Output Voltage	V_{OL} V_{OH}	-0.3 3.7	0 5	0.5 5.25	V V	I_{OL} = 2mA I_{OH} = 2mA
5	$\overline{LED}$	Low Level Output Voltage② High Level Output Voltage	V_{OL} V_{OH}	 2.0		3.0	V V	I_{OL} = 1.1mA I_{OH} = 0.7mA
6	$\overline{RD1}$ $\overline{RD2}$ $\overline{RD3}$	Sink Current, Relay to V_{DD} Clamp Diode Current	I_{OL} I_{CD}	65 100			mA mA	V_{OL} = 1.0V
7	GS	Low Level Input Voltage High Level Input Voltage	V_{IL} V_{IH}	 2.0		0.8	V V	
8		Low Level Input Current High Level Input Current	I_{IL} I_{IH}			1 1	µA µA	V_{IL} = 0V V_{IH} = 5.0V
9	SDi $\overline{RD}$	Low Level Input Current Intermediate Input Current High Level Input Current	I_{IL} I_{IM} I_{IH}			10 10 10	µA µA	V_{IL} = 5.0V V_{IM} = 0.5V V_{IH} = 5.0V
10	Do	Low Level Output Voltage High Level Output Voltage Tri-State Leakage Current	V_{OL} V_{OH} I_{OZ}	 4.0	 0.1	0.4	V V mA	I_{OL} = 1.6mA I_{OH} = 0.1mA
11	SDi Di	Low Level Input Current High Level Input Voltage	V_{IL} V_{IH}	 2.4		0.8	V V	
12	$\overline{C2i}$ $\overline{F1i}$	Low Level Input Current High Level Input Current	I_{IL} I_{IH}			10 10	µA µA	V_{IL} = 0V V_{IH} = 5.0V

* DC Electrical Characteristics are over Recommended Operating Conditions with V_{DD} at + 5.0V ± 5% unless otherwise stated.

† Typical figures are at 25°C with nominal ± 5V supplies and are for design aid only.

① Supply current and power consumption characteristics are over Recommended Operating Conditions with V_{DD} at 5.0V, V_{EE} at -5.0V and V_{Bat} at -48.0V.

② The LED output consists of a 2.2K Ω resistor in series with the $\overline{SHK}$ HCT output.

Loop Electrical Characteristics*

	Characteristics	Sym	Min	Typ†	Max	Units	Test Comments
1	Maximum AC Ringing ① Current Rejection		33			mA	25Hz, V_{Bat} = -48V
2	Ring Trip Detect Time ②			100	125	ms	
3	Hook Switch Detect Time: Off-Hook to On-Hook On-Hook to Off-Hook				 20 20	 ms ms	
4	Operating Loop Current	I_{IP}	18	22	50	mA	LCA = Adjustable
5	Operating Loop Resistance	R_{IP}	0 0		1900 2300	Ω Ω	V_{Bat} = -39.8V V_{Bat} = -48V
6	Loop Current at Off-Hook ③ Detect Threshold	I_{sh}	7	10	13	mA	

* Loop Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.
† Typical figures are at 25°C with nominal ± 5V supplies and are for design aid only.
① The SLIC can be loaded with an AC impedance as low as 4000Ω without generating a false $\overline{SHK}$ output. Since each REN represents 8kΩ, the SLIC can drive a REN of 2 without generating a false $\overline{SHK}$ output.
② This parameter is over Recommended Operating Conditions as well as the specified Operating Loop Resistance.
③ Off-Hook Detect ($\overline{SHK}$) will be detected for loop lengths of 2900Ω or less.

AC Electrical Characteristics*

	Characteristics	Sym	Min	Typ†	Max	Units	Test Comments
1	2- Wire input (200Ω + 560Ω // 0.1μF) –2 Variant (200Ω + 680Ω // 0.1μF) –4 Variant	Z_{in}		 720 813		 Ω Ω	 1020 Hz 1020 Hz
2	Return Loss at 2-Wire		14 18 14	51 40 32		dB dB dB	300 Hz 500-2000 Hz 3400 Hz
3	Longitudinal to Metallic Balance		40 46	65 65		dB dB	300-600 Hz 600-3400 Hz
4	Transhybrid Loss		16 20 16	36 24 24		dB dB dB	300 Hz 500-2500 Hz 3400 Hz
5	Power Supply Rejection Ratio at 2-wire and Do: V_{DD} V_{EE} V_{Bat}	PSRR	 20 20 20	 40 30 40		 dB dB dB	Ripple 50mV 1020 Hz

* AC Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.
† Typical figures are at 25°C with nominal ±5V supplies and are for design aid only.

AC Electrical Characteristics* - Transmit (A/D path)

	Characteristics	Sym	Min	Typ†	Max	Units	Test Comments
1	Absolute Gain Default (codec odB)		-0.5	0	0.5	dB	Input -6dB 1020 Hz
2	Transmit Gain			0		dB	
3	Loss Distortion with frequency (relative to level at 1020Hz with codec at 0dB)		0.0 -0.3 -0.3 -0.3 -0.3 -0.3 -0.3	 0.39 0.22	- - 1.0 0.75 0.35 0.55 1.5	dB dB dB dB dB dB dB	0-200 Hz 200-300 Hz 300-400 Hz 400-600 Hz 600-2400 Hz 2400-3000 Hz 3000-3400 Hz
4	Gain variation with Input Level (relative to gain at 1020Hz with -6dBm input)		 -0.25 -0.25 -0.5 -1.5		 0.25 0.25 0.5 1.5	 dB dB dB dB	Input 1020 Hz 0 to +3dBm -40 to 0dBm -50 to -40dBm -55 to -50dBm
5	Signal Input Overload Level at 2-Wire		3.14			dBm	THD ≤ 5% Input 1020Hz
6	Signal Output Overload Level at Do		3.14			dBm0	THD ≤ 5% Input 1020Hz
7	Signal to Total Distortion Ratio at Do		 35 33.8 28.8 19.5 14.5			 dB dB dB dB dB	Input at 2-Wire 0 to -10dB -20dBm -30dBm -40dBm -50dBm
8	Out-of-Band Discrimination at Do: Signals in 4.6 -72 kHz band Signals in 300-3400 Hz band other than 1020 Hz Signals in 4.6 -72 kHz band				 -50 -40 -25	 dBm0 dBm0 dBm0	Input at 2-wire -25dBm, 4.6 -72kHz 0dbm, 1020Hz 0dBm, 300 -3400 Hz
9	Harmonic Distortion (2nd or 3rd Harmonic) at DSTo				-41	dB	
10	Idle Channel Noise at Do			-70	-64	dBm0p	

† Typical figures are at 25°C with nominal ±5V supplies and are for design aid only.

* AC Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

AC Electrical* - Receive (D/A) path

	Characteristics	Sym	Min	Typ†	Max	Units	Test Comments
1	Absolute Gain (Codec 0dB, GS = 5V)		-0.5	0.0	0.5	dB	Input -10dBm0 1020 Hz
2	Gain programmable Range GS = 5V GS = 0V			 -3.5 -7.0		 dB dB	Input - 10dBm0 1020 Hz 1020 Hz
3	Loss Distortion with Frequency (relative to level at 1020 Hz with codec at 0dB and GS = 5V)		 -0.3 -0.3 -0.3 -0.3 -0.3 -0.3 -0.3	 -0.09 -0.08	 - - 1.0 0.75 0.35 0.55 1.5	 dB dB dB dB dB dB dB	Input -10dBm0 0-200 Hz 200-300 Hz 300-400 Hz 400-600 Hz 600-2400 Hz 2400-3000 Hz 3000-3400 Hz
4	Gain Variation with Input Level (relative to gain to 1020Hz with -10dBm0 input)		 -0.25 -0.25 -0.5 -1.5		 0.25 0.25 0.5 1.5	 dB dB dB dB	Input 1020 Hz 0 to +3dBm -40 to 0dBm -50 to -40dBm -55 to -55dBm
5	Signal Input Overload Level at Di		3.14			dBm	THD $\leq$ 5% Input 1020Hz
6	Signal Output Overload Level at 2-wire		3.14			dBm0	THD $\leq$ 5% Input 1020Hz
7	Signal Output to Total Distortion Ratio at 2-Wire		 35 32.9 24.9 19.9			 dB dB dB dB	Input at 2-Wire 0 to -20dB -30dBm -40dBm -50dBm
8	Out-of-Band Discrimination at 2-Wire: Signals in 4.6 -72 kHz band Signals in 300-3400 Hz band other than 1020 Hz Signals in 4.6 -72 kHz band				 -50 -40 -25	 dBm dBm dBm	Input at Di -25dBm0, 4.6 -72kHz 0dBm0, 1020 Hz 0dBm0, 300-3400 Hz
9	Harmonic Distortion (2nd or 3rd Harmonic) at 2-Wire				-41	dB	
10	Idle Channel Noise at 2-Wire			 -73 -73	 -67 -67	 dBmp dBmp	Gain Setting -3.5dB -7dB

* AC Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

† Typical figures are at 25°C with nominal ±5V supplies and are for design aid only.

Loop Electrical Characteristics

		Characteristics		Sym	Min	Typ*	Max	Units	Test Comments
1	DIGITAL	Clock Frequency	C2i	f_C	2.046	2.048	2.05	MHz	
2		Clock Rise Time	C2i	t_{CR}			50	ns	
3		Clock Fall Time	C2i	t_{CF}			50	ns	
4		Clock Duty Cycle	C2i		40	50	60	%	
5		Chip Enable Rise Time	$\overline{F1i}$	t_{ER}			100	ns	
6		Chip Enable Fall Time	$\overline{F1i}$	t_{EF}			100	ns	
7		Propagation Delay Clock to Output Enable	Do	t_{PZL} t_{PZH}			122 122	ns ns	R_L = 10kΩ to V_{CC} C_L = 100pF
8		Input Setup Time	Di	t_{ISH} t_{ISL}	25 0			ns ns	
9		Input Hold Time	Di	t_{IH}	60			ns	

* Typical figures are at 25°C with nominal ±5V supplies. For design aid only: not guaranteed and not subject to production testing.

Bit	Name	Description
0	SD0	When Logic ‘0’ activates relay driver 1 to apply ringing to the line
1	SD1	When logic ‘0’ activates relay driver 2. Normally used for in-test
2	SD2	When logic ‘0’ it will set the receive gain to -7.0dB When logic ‘1’ it will set the receive gain to -3.5dB
3	SD3	When logic ‘0’ reverses the TIP and RING.
4	SD4	When logic ‘0’ activates relay driver 3. Normally used for out-test
5	SD5	The output of the serial data stream SDi, bit 5. Bit inverted
6	SD6	The output of the serial data stream SDi, bit 6. Bit inverted
7	SD7	The output of the serial data stream SDi, bit 7. Bit inverted

Table 1 - Control of SLIC Functions through SD

Functional Description

The MITEL MH89626C OPS SLIC (Off-Premise Subscriber Line Interface Circuit) provides a complete interface between an off-premise telephone line and a digital switching system. All BORSCHT functions are provided requiring only a few external components. The input impedance conforms with Chinese standard requirements.

Overvoltage Protection

The MH89626C is protected from short term (20ms) transients (±250V) between TIP and RING, TIp and Ground, and RING and Ground. However, if the MH89626C is used in conjunction with MH80626C, protection sip, it will meet all CCITT K.20 requirements. The applications circuit is shown in Figure 2.

The MH80626C has two battery feed resistors (50 ohms) and one ringing feed resistor (560 ohms), that are required to be used with the MH89626C as a complete line interface. All resistors on the hybrid are specially designed to withstand high power. The two battery feed resistors are accurately trimmed to achieve good longitudinal balance. Two fuses and current limited resistors (5 ohms) are provided on the hybrid for lightning and high voltage surge protection.

Battery Feed

The MH89626C powers the telephone set with constant DC loop current for short lines and automatically reverts to constant voltage for long lines. If the LCA pin is left open, the constant current is set at 23 mA. The Constant current can also be set by adding a resistor connected fro the LCA pin to V_{EE}. The resistance (R) can be calculated as:

$$R = \frac{147.2 - I_{Loop}}{(0.0001176 \times I_{Loop}) - 0.002586}$$

Where I_{Loop} is the desired constant loop current in mA, and R is the resistance from pin LCA to pin V_{EE} in ohms.

R(kΩ)	348K	200K	80K	50K	30K
I_{Loop} (mA)	25.0	27.1	34.0	40.2	49.7

TIP/RING Reversal

For a Direct Inward Dialling (DID) operation, the MH89626C provides a TIP and RING reversal function on the hybrid. This built-in line polarity reversal capability will eliminate the use of an external bulky mechanical relay and provides fast and reliable Tip and Ring reversed function. The serial control stream, SDi, bit 3 at logic low will reverse the polarity of the Tip and Ring. Refer to Table 1 for control of the SLIC functions.

Ringing

The ringing insertion circuitry has the capability to provide ringing voltage to a telephone set by simply adding an external relay, ring generator. The serial control stream, SDi, bit 0 at logic low will activate the Refer to Table 1 for the control of SLIC functions.

Supervision

The loop detection circuit determines whether a low enough impedance is across Tip and Ring to be recognized as an off-hook condition. When an off-hook condition occurs, the $\overline{SHK}$ and the $\overline{LED}$ outputs toggle to a low level. These outputs also toggle with incoming dial pulses.

During applied ringing, the loop detection circuit engages a ringing filter. This filter prevents a false off-hook detection due to the current associated with the AC ringing voltage as well as current transients that occur when the ringing voltage is switched in and out. The Ring trip detection circuitry deactivates the ring driver after an off-hook condition is detected.

Transmit and Receive Gain

The Transmit Gain (Tip-Ring to Do) is fixed at 0dB. The Receive Gain (Di to Tip-Ring) is programmable in -3.5 or -7.0dB, either using software (SDi, bit 2) or external hardware (GS pin).

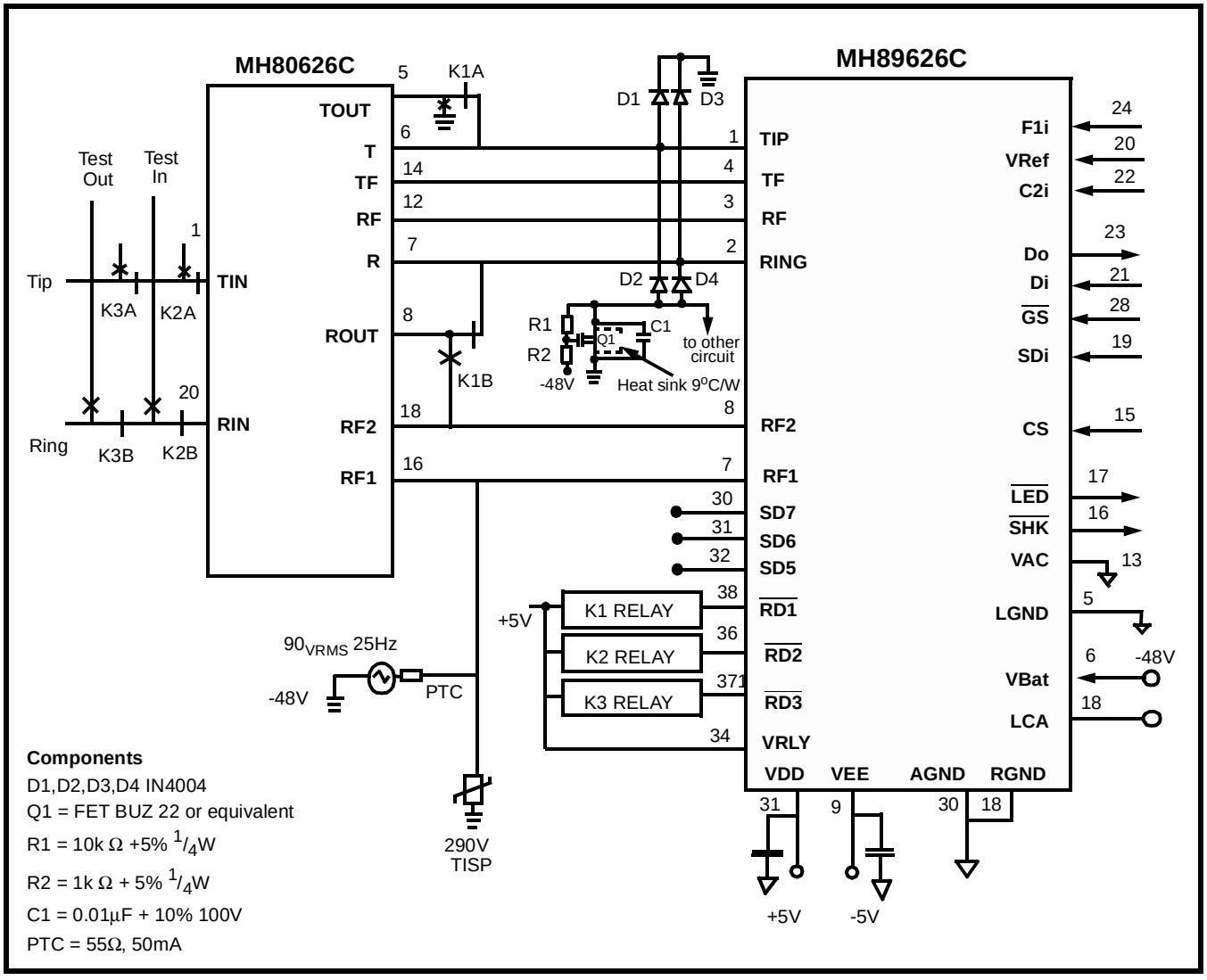

Figure 3 - Application Circuit

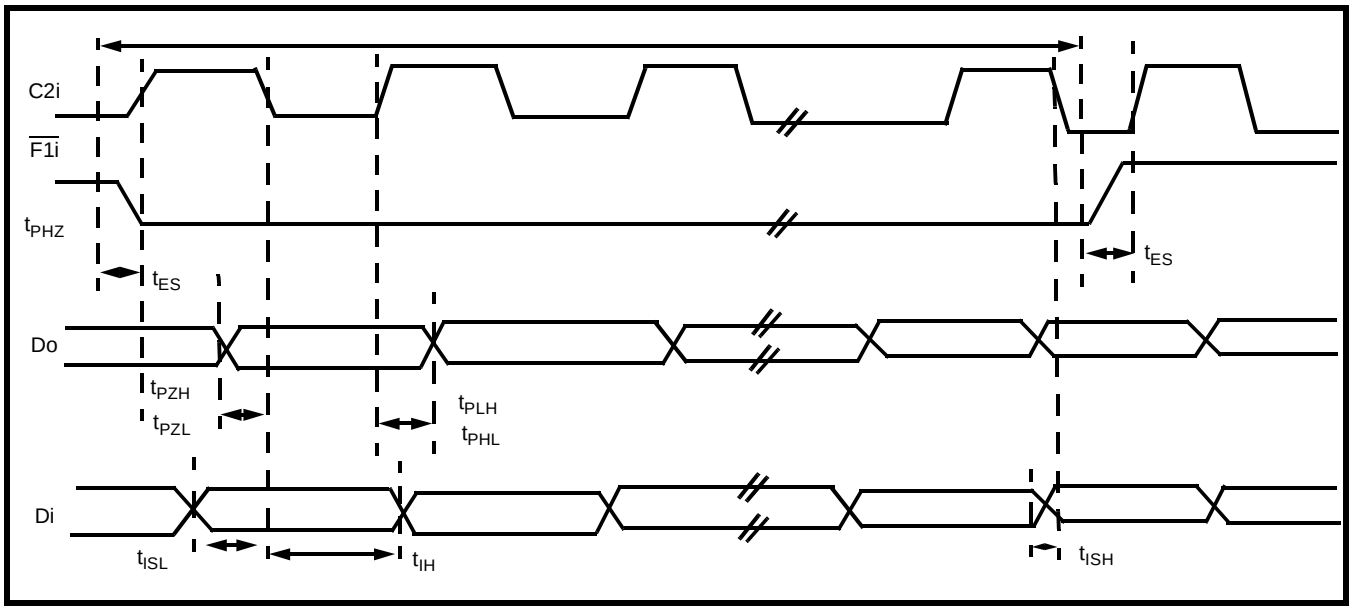

Figure 4a - Control Timing Diagram

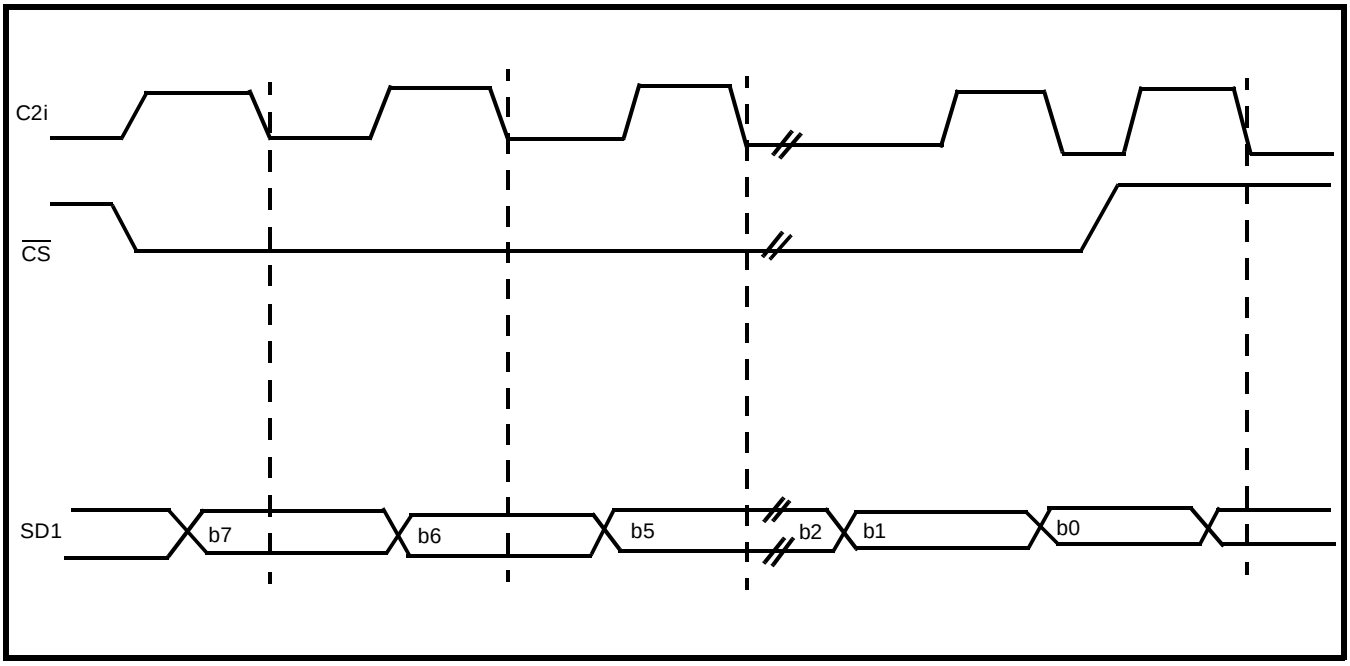

Figure 4b -Control Timing Diagram

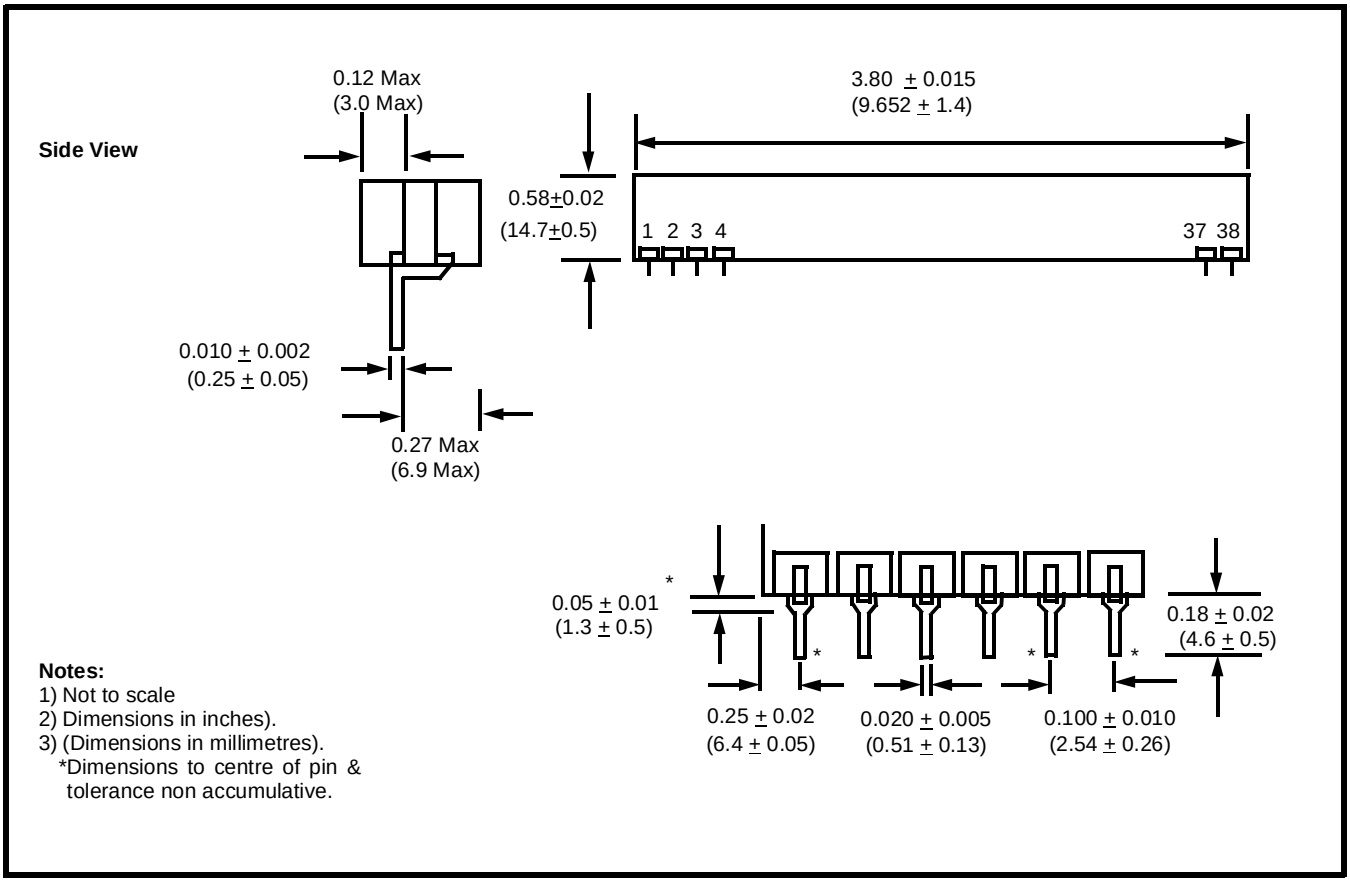

Figure 5 - Mechanical Data