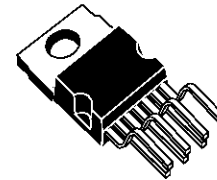


MONOLITHIC LAMP DIMMER

- HIGH EFFICIENCY DUE TO PWM CONTROL AND POWER DMOS DRIVER
- LOAD CONNECTED TO GROUND
- CURRENT LIMITATION
- OVER AND UNDERVOLTAGE PROTECTION
- ON CHIP THERMAL PROTECTION
- LIMITED AND PROGRAMMABLE OUTPUT VOLTAGE SLEW RATE
- OPEN GROUND PROTECTION
- VERY LOW STANDBY POWER CONSUMPTION
- LOAD DUMP PROTECTION
- MINIMIZED ELECTROMAGNETIC INTERFERENCE
- WIDE CHOICE IN PWM FREQUENCY RANGE
- LOAD POWER LIMITATION

MULTIPOWER BCD TECHNOLOGY

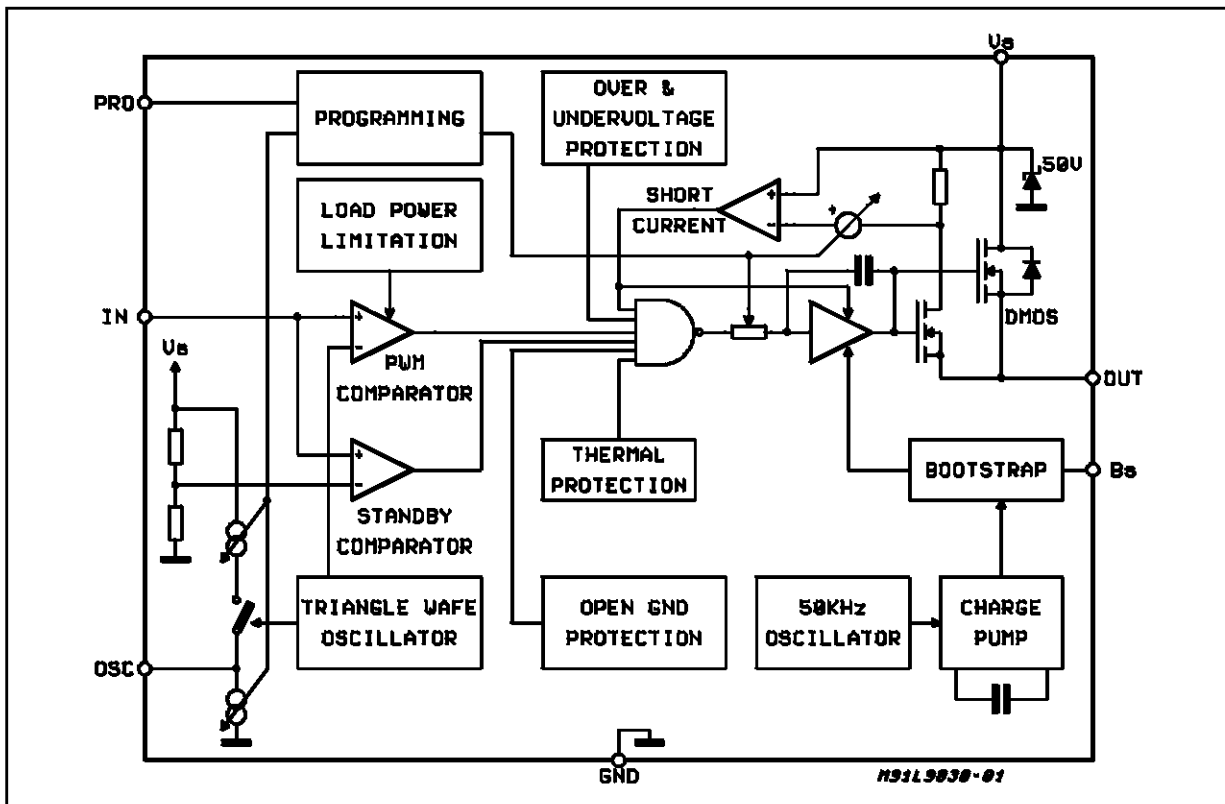


Heptawatt
ORDERING NUMBER: L9830

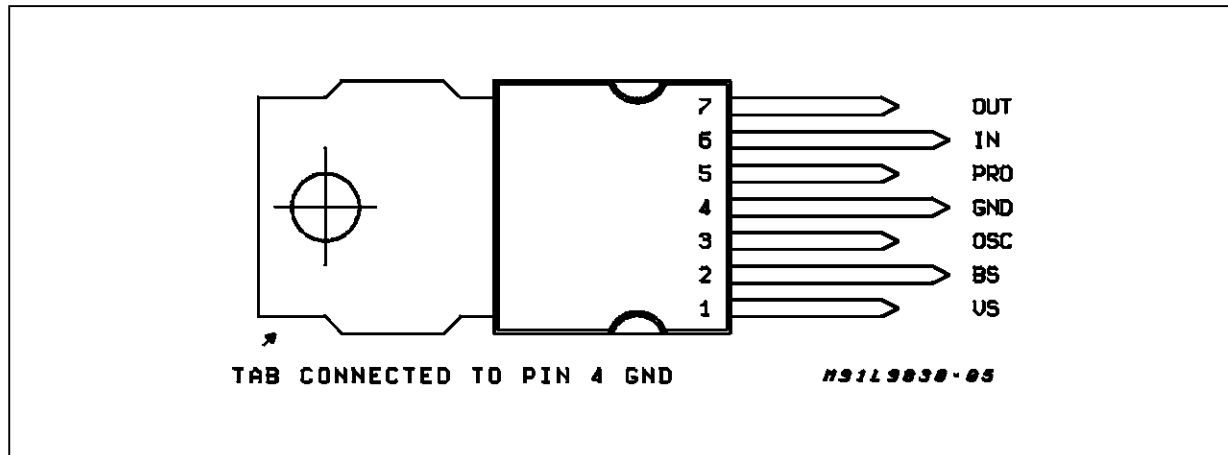
DESCRIPTION

The L9830 high side driver is a monolithic integrated circuit realized with Multipower BCD mixed technology to drive resistive or inductive loads in PWM mode with one side connected to ground.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



PIN FUNCTION

PIN	NAME	DESCRIPTION
1	V _S	Common supply connection also Drain of the power DMOS.
2	BS	A capacitor connected between this pin and the Source of the power DMOS pin Out gives the possibility to bootstrap the gate driving voltage of the power DMOS.
3	OSC	A capacitance C _T connected between GND and this terminal determines the PWM switching frequency.
4	GND	Common ground connection.
5	PRO	A resistor connected between this pin and GND provide the possibility to programming the output voltage slew rate, the PWM oscillator frequency and the short current value.
6	IN	Analog input for controlling the PWM ratio, related to V _S .
7	OUT	Source connection of the internal power DMOS.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _S	Supply Voltage	60	V
V _{DS}	Drain Source Voltage	60	V
V _{IN}	Input Voltage	-0.3V up to V _S +0.3V	
I _S	Supply Current	±0.2	A
I _{OR}	Output Reverse Current	-2	A
P _{tot}	Power Dissipation at T _{case} ≤ 75°C	37.5	W
T _{amb}	Operating Ambient Temperature Range	-40 to +85	°C
T _j	Operating Junction Temperature Range	-40 to 150	°C
T _{stg}	Storage Temperature	-65 to 150	°C

THERMAL DATA

Symbol	Description	Value	Unit
R _{th j-case}	Thermal Resistance Junction-case	Max 2	°C/W

ELECTRICAL CHARACTERISTICS ($6V \leq V_S \leq 16V$; $-40^\circ\text{C} \leq T_{\text{amb}} \leq 85^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{qo}	Operating Quiescent Current $I_{\text{qo}} = 11.3 \frac{V_S - 0.7V}{R_P} + 0.67\text{mA}$	$V_{\text{IN}} = V_S$ $R_P \rightarrow \infty$ $R_P = 30\text{K}\Omega$		2.4 8.5	6 18	mA mA
I_{qs}	Standby Current	$V_{\text{IN}} = 0$ $T_j \leq 100^\circ\text{C}$	0	200	600	μA
V_{INSB}	Input Standby High Threshold V_{IN}/V_S		0.1	0.15	0.2	
V_{INSBhys}	Input Standby Hysteresis		-350	-190	-50	mV
V_{INH}	Input High Threshold	$f_o \times t_{\text{on}} = 1$ $V_S \leq V_{\text{SLPL}}$	0.95 V_S		$V_S + 0.3V$	
I_{IN}	Input Current	$-0.3 \leq V_{\text{IN}} \leq V_S + 0.3V$		1	5	μA
V_{SL}	Low Supply Voltage Disable High Threshold		5	5.5	6	V
V_{SLhys}	Low Supply Voltage Disable Hysteresis		-300	-100	-50	mV
V_{SLPL}	Load Power Limitation Start Supply Voltage	$V_{\text{IN}} \geq V_{\text{INH}}$, $f_{\text{on}} \cdot t_{\text{on}} = 0.96$	12	13.0	17	V
V_{SH}	High Supply Voltage Disable High Threshold		16	17.8	20	V
V_{SHhys}	High Supply Voltage Disable Hysteresis		-350	-190	-50	mV
V_{SLD}	Load Dump Supply Voltage Threshold	$I_q = 50\text{mA}$	45	52	55	V
I_{CLD}	Load Dump Clamping Current	$V_S = 60V$	100	150	300	mA
T_{ST}	Thermal Shutdown Temperature		150	175	200	$^\circ\text{C}$
T_{SThys}	Thermal Shutdown Temperature Hysteresis		-50	-40	-30	$^\circ\text{C}$
K_{Ti}	Internal PWM Frequency Constant (without R_P)	$f_o = K_{\text{Ti}}/C_T$	1000	2000	3000	Hznf
K_{Te}	External PWM Frequency Constant	$f_o = \frac{1}{C_T R_P} K_{\text{Te}}$ $30\text{K}\Omega \leq R_P \leq 500\text{K}\Omega$	0.220	0.250	0.350	
I_{osi}	Internal Short Current Limitation (without R_P) (4)	$V_S = 12V$	3	6	9	A
I_{ose}	External Programmable Short Current Limit (30K $\Omega \leq R_P \leq 500\text{K}\Omega$) (3)	$V_S = 12V$, $R_P = 125\text{K}\Omega$	5	6	10	A
R_{DS}	Static Drain Source on Resistance	$V_S \geq 9V$, $I_o = 1A$		190	380	m Ω
S_i	Internal Fixed Output Voltage Slew Rate (without R_P) (1)	$V_S = 12V$; $5\Omega \leq R_L \leq 7\Omega$ $T_{\text{amb}} \leq 25^\circ\text{C}$	50 50	120 120	230 250	V/ms V/ms
S_e	External Programmable Output Voltage Slew Rate (30K $\Omega \leq R_P \leq 500\text{K}\Omega$) (2)	$V_S = 12V$, $R_P = 125\text{K}\Omega$ $R_L = 6\Omega$ $T_{\text{amb}} \leq 25^\circ\text{C}$	50 50	120 120	200 250	V/ms V/ms

Notes:

$$(1) S_i = V_S \cdot 11.16 \frac{1}{\text{ms}} - 7.26 \text{ V/ms}$$

$$(2) S_e = \frac{R_L}{R_P} \cdot \frac{V_S - 0.65V}{R_L + 0.32\Omega} \cdot 1.47 \cdot 10^6 \frac{V}{\text{msA}}$$

$$(3) I_{\text{OSP}} = (V_S - 0.6V) \cdot \frac{64260}{R_P}$$

$$(4) I_{\text{os}} = (V_S - 0.6V) \cdot 0.514 \frac{A}{V}$$

If R_P is not present in application an internal equivalent resistor can be inserted in the calculation with a typical value of $R_P = 125\text{K}\Omega$

FUNCTIONAL DESCRIPTION

To control the power of the load with a POWERMOS transistor in the switched mode, its gate must be driven with a PWM signal. The amplitude of the gate driving pulse must guarantee that the Power DMOS transistor will be completely saturated during the ON phase. To generate the necessary gate driving voltage a charge pump circuit is required. With this circuit a gate voltage of $2 \cdot (V_S - 1.5V) \leq V_S + 16V$ typically will be obtained.

The slope of the leading and trailing edge of the gate driving pulse is defined with an internal capacitor. The important criteria for the dimensioning of the output voltage slope are the electromagnetic radiation and the power dissipation of the Power DMOS. The typical value of the output pulse slope is in the range of 120V/ms to fulfill automotive radiation requirements.

The output pulse slope is directly related to the value of the supply voltage V_S and in a wide range programmable through the programming resistance R_P .

$$S = \frac{dV_{out}}{dt} = R_L \cdot \frac{dI_{load}}{dt} = \frac{R_L}{R_P} \cdot \frac{V_S - 0.65V}{R_L + 0.32\Omega} \cdot 1.47 \frac{10^6 V}{Ams}$$

The value of the gate voltage slope due to the POWERMOS parasitic capacitors must be in a relation to the charge pump performance. For fast gate voltage variation the bootstrap option can be used. The bootstrap capacitance should have a relation greater than 50 to the DMOS parasitic ca-

pacitors and should be in the range of

$$C_{BS} \geq 100nF$$

The switching frequency "fo" is defined with a triangle oscillator and it's programmed with the capacitor C_T , or C_T and R_P if a greater precision is required.

$$f_O = K_T/C_T \text{ (without } R_P)$$

$$f_O = \frac{1}{4C_T R_P} \text{ (with } R_P)$$

The modulation factor of the PWM driving signal of the external Power DMOS transistor is defined with the voltage level at the analog input. Fig. 1 shows the typical transfer curve giving the PWM factor as a function of the input/supply voltage ratio.

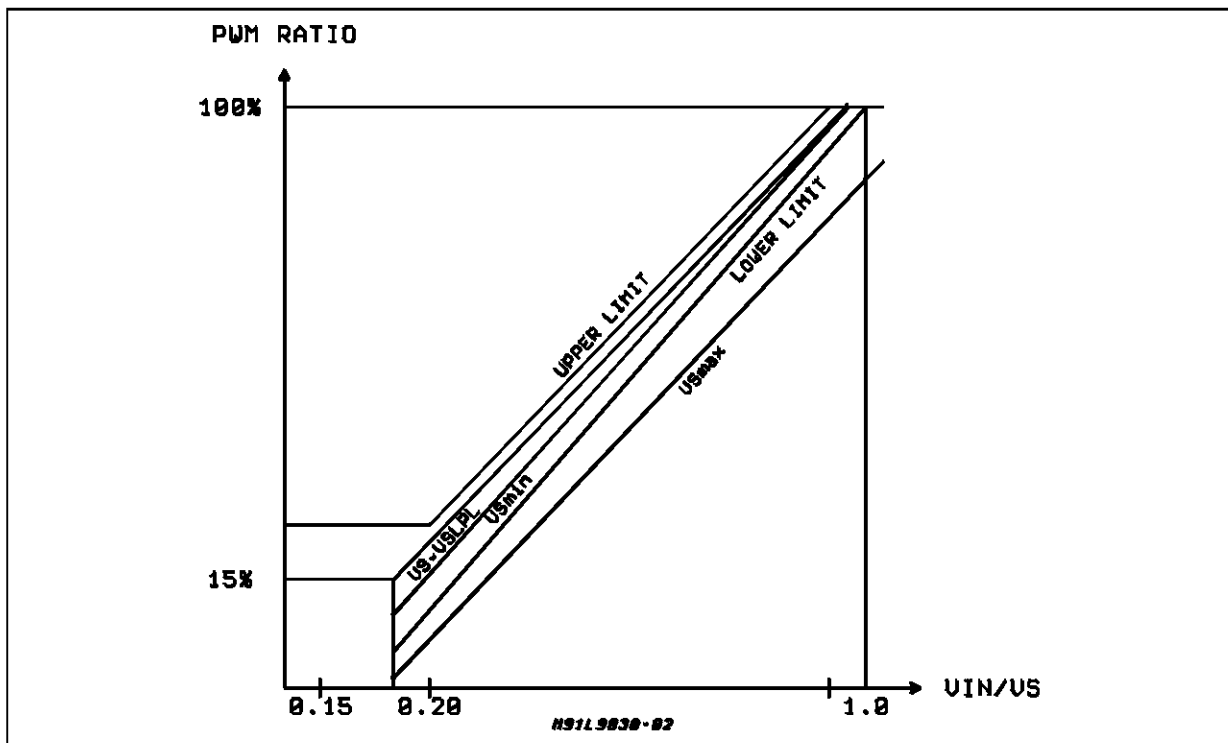
For higher supply voltage values, the power limitation circuitry will linearly reduce the PWM ratio to achieve a constant load power to extend the lamps life time.

The input voltage is referred to the supply voltage. The regulation of the PWM factor can be realized with a potentiometer connected to the supply voltage and the analog input, see the typical application circuit diagram.

The maximum load current in the short circuit condition is limited internally with a sense DMOS cell.

The value of the short current is a multiple of the programming current flowing through R_P or the internal fixed resistance. Therefore this short current

Figure 1: Transfer Characteristic



value is supply voltage dependent to achieve in any condition the lamp required warm up current which will be normally two or three times higher.

$$I_{OSe} = \frac{VS - 0.6V}{R_P} \cdot 64260$$

If the short current condition is detected the gate will be driven with a DC voltage which value is regulated to maintain the specified current. With this function the switch ON phase for each load will be speeded up.

The circuit features also a protection which allows to withstand high overvoltage for a limited time (load dump in automotive application). Above the V_{SH} threshold the gate driving of the POWER-

MOS transistor is switched OFF and the gate is held at the GND potential. When the V_{BAT} rises above the internal supply clamp voltage V_{SLD} the clamping diode becomes active with a serial resistance of R_{LD} and the gate voltage is floating with the GND potential. At this time the current flowing through the load is not limited. In this condition the load voltage can be calculated to

$$V_L = VS = V_{SLD} - V_{GS} \quad V_{GS} \ll V_{SLD}$$

This device is protected against temperature destruction through an internal power dissipation protection. The total power dissipation of the device can be calculated with:

for $V_{SL} \leq VS \leq V_{SLPL}$:

$$P_{tot} = VS^2 \cdot \left(\frac{R_{DS}}{(R_{DS} + R_L)^2} + \frac{f_o}{S} \cdot \left(1 - \frac{R_{DS}}{R_{DS} + R_L}\right) \cdot \left(1 - \frac{R_{DS}}{R_{DS} + R_L}\right) \cdot \left(1 + \frac{2VS}{R_{DS} + R_L}\right) \right)$$

and for $V_{SLPL} \leq VS \leq V_{SH}$:

$$P_{tot} = V_{SLPL}^2 \cdot \frac{R_{DS}}{(R_{DS} + R_L)} + \frac{VS^2 f_o}{S} \cdot \left(1 - \frac{R_{ON}^2}{R_{ON} + R_L}\right)$$

Figure 2: Total Power Dissipation Characteristic

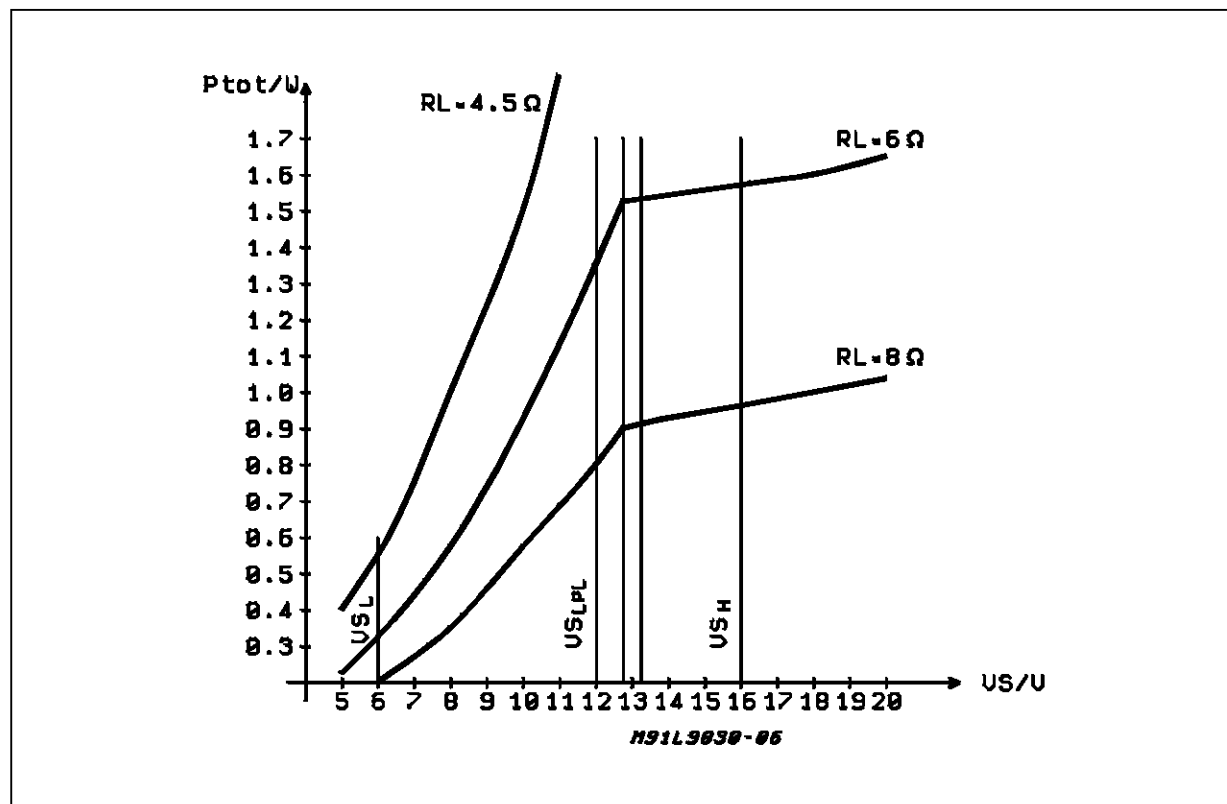


Figure 3: Application Circuit Diagram for Dashboard Dimming

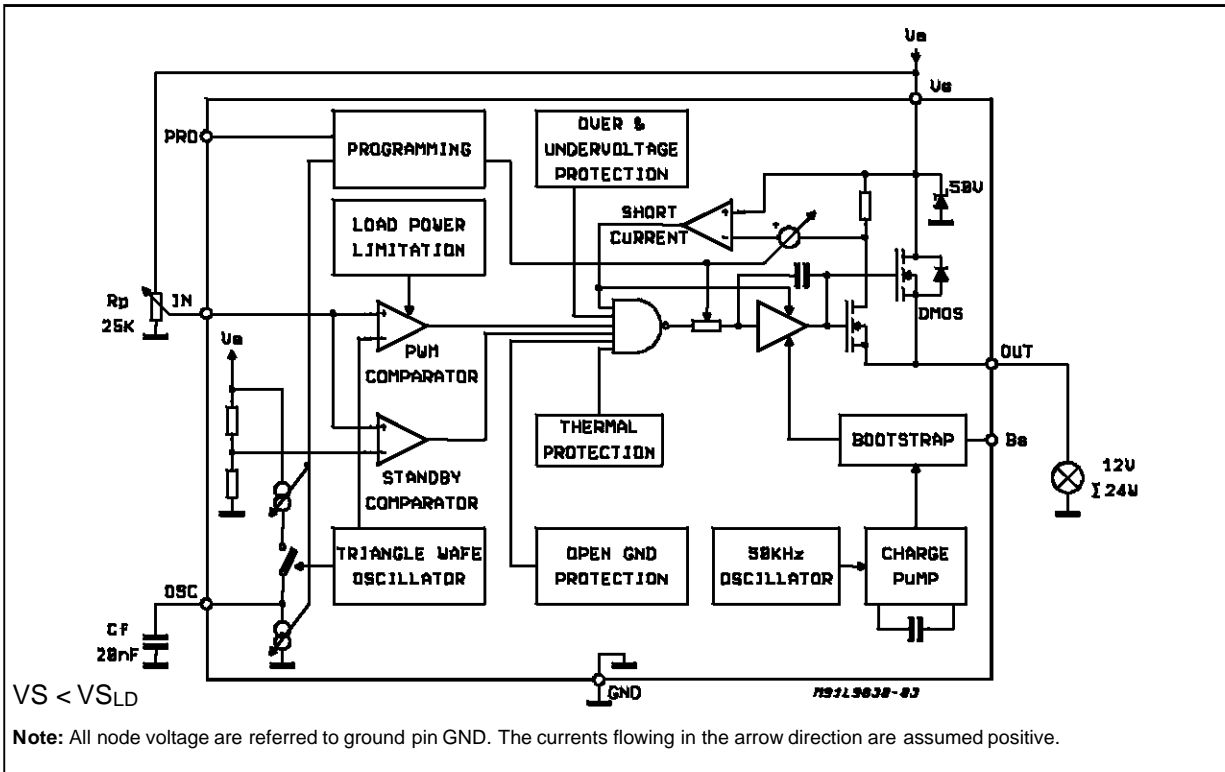
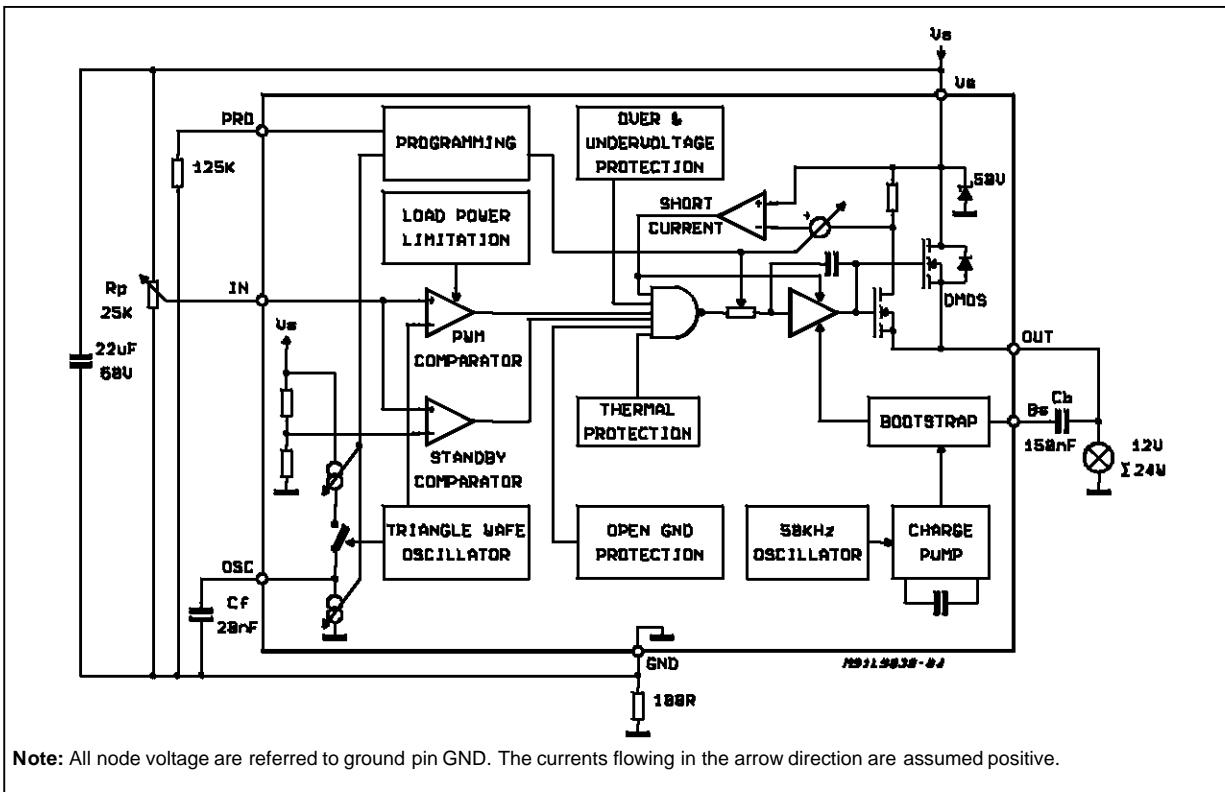
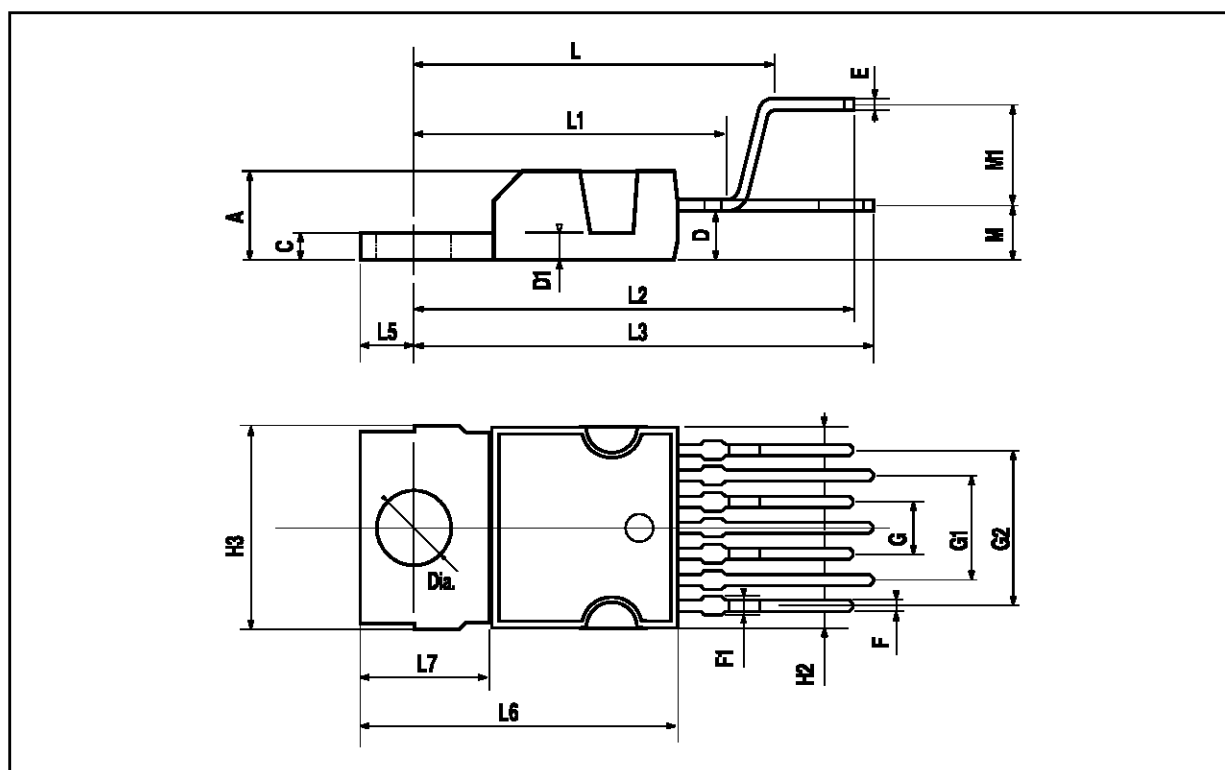


Figure 4: Application Circuit Diagram for Dashboard Dimming with Optimized Device Power Dissipation



HEPTAWATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152



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