

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT7540**

**Octal Schmitt trigger buffer/line driver; 3-state; inverting**

Product specification  
Supersedes data of March 1988  
File under Integrated Circuits, IC06

December 1990

# Octal Schmitt trigger buffer/line driver; 3-state; inverting

## 74HC/HCT7540

### FEATURES

- Inverting outputs
- Schmitt trigger action on all data inputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT7540 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7540 are octal Schmitt trigger inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $\overline{OE}_1$  and  $\overline{OE}_2$ .

A HIGH on  $\overline{OE}_n$  causes the outputs to assume a high impedance OFF-state.

The Schmitt trigger action in the data inputs transforms slowly changing input signals into sharply defined jitter-free output signals.

The "7540" is identical to the "540" but has hysteresis on the data inputs.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\overline{Y}_n$	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	11	16	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per buffer	notes 1 and 2	29	31	pF

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

### ORDERING INFORMATION

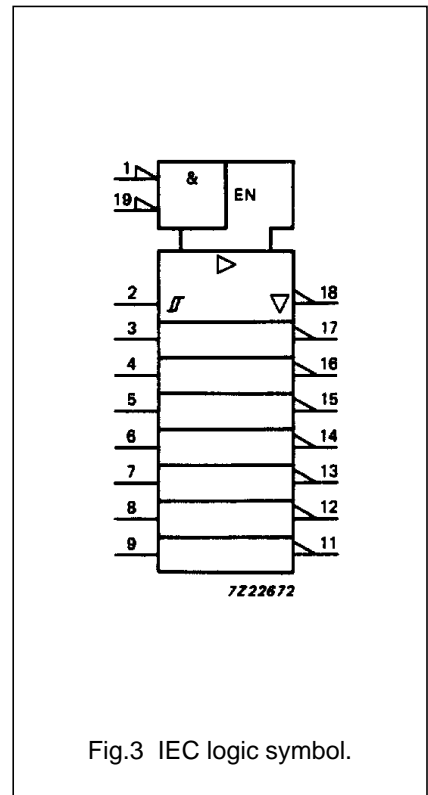
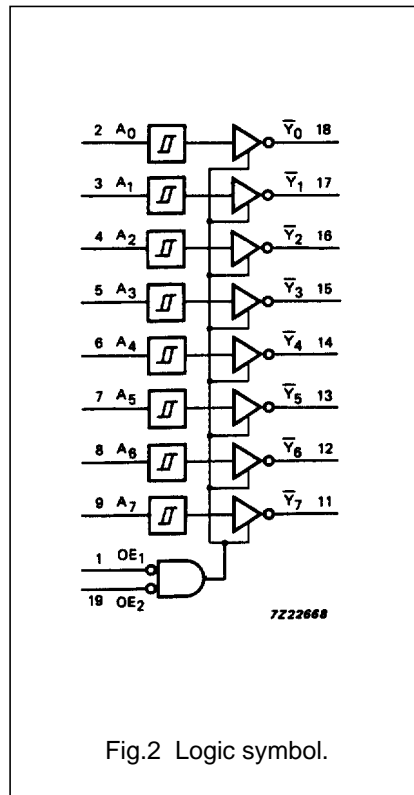
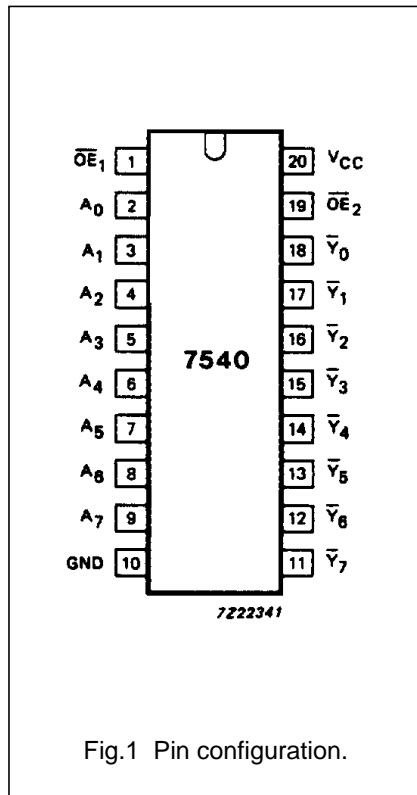
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Octal Schmitt trigger buffer/line driver;  
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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1, \overline{OE}_2$	output enable inputs (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A <sub>0</sub> to A <sub>7</sub>	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y}_0$ to $\overline{Y}_7$	bus outputs
20	V <sub>CC</sub>	positive supply voltage



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FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE}_1$	$\overline{OE}_2$	$A_n$	$\overline{Y}_n$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

Notes

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

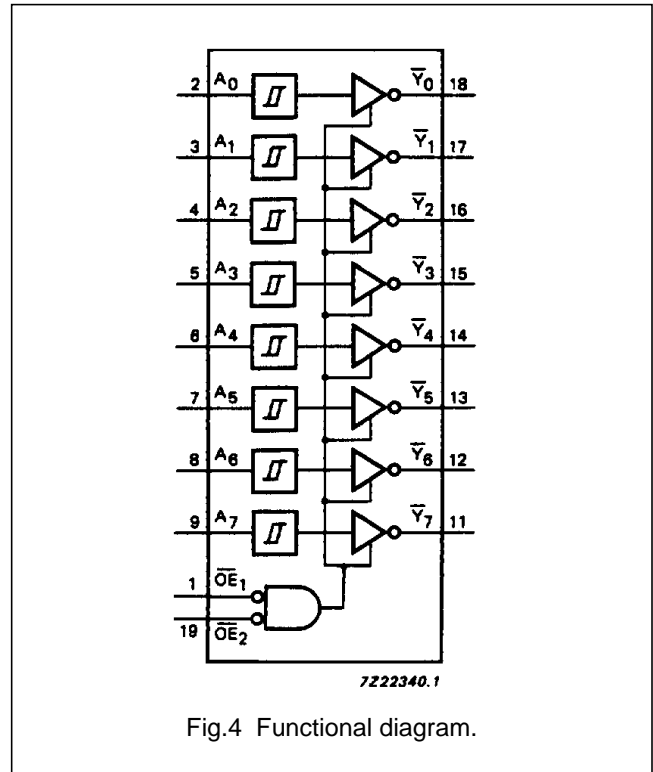


Fig.4 Functional diagram.

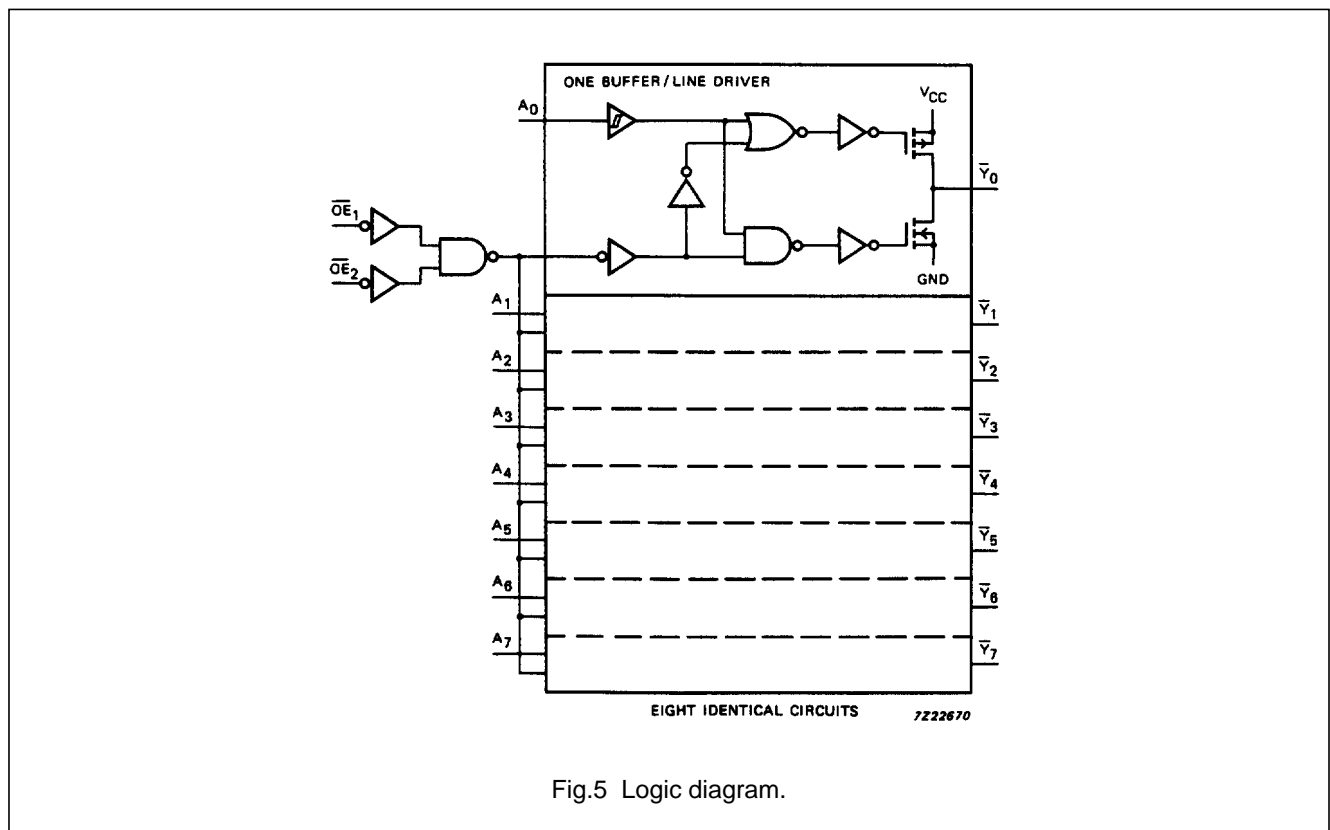


Fig.5 Logic diagram.

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Transfer characteristics are given below (not applicable for  $\overline{OE}_n$  inputs).

Output capability: bus driver

$I_{CC}$  category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $\overline{Y}_n$		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.8
$t_{PZH}/t_{PZL}$	3-state output enable time $\overline{OE}_n$ to $\overline{Y}_n$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.9
$t_{PHZ}/t_{PLZ}$	3-state output disable time $\overline{OE}_n$ to $\overline{Y}_n$		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.9
$t_{THL}/t_{TLH}$	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.8

## TRANSFER CHARACTERISTICS FOR 74HC

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$V_{T+}$	positive-going threshold			1.50 3.15 4.20		1.50 3.15 4.20		1.50 3.15 4.20	V	2.0 4.5 6.0	Figs 6 and 7
$V_{T-}$	negative-going threshold	0.30 1.35 1.80			0.30 1.35 1.80		0.30 1.35 1.80		V	2.0 4.5 6.0	Figs 6 and 7
$V_H$	hysteresis ( $V_{T+} - V_{T-}$ )	0.10 0.25 0.30	0.20 0.40 0.50		0.10 0.25 0.30		0.10 0.25 0.30		V	2.0 4.5 6.0	Figs 6 and 7

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Transfer characteristics are given below (not applicable for  $\overline{OE}_n$  inputs).

Output capability: bus driver

$I_{CC}$  category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD
$\overline{OE}_1$	1.30
$\overline{OE}_2$	1.30
$A_n$	0.20

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS	
		74HCT									$V_{CC}$ (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min	typ.	max.	min	max.	min.	max.				
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $\overline{Y}_n$		19	32		40		48	ns	4.5	Fig.8	
$t_{PZH}/t_{PZL}$	3-state output enable time $\overline{OE}_n$ to $\overline{Y}_n$		19	32		40		48	ns	4.5	Fig.9	
$t_{PHZ}/t_{PLZ}$	3-state output disable time $\overline{OE}_n$ to $\overline{Y}_n$		20	32		40		48	ns	4.5	Fig.9	
$t_{THL}/t_{TLH}$	output transition time		5	12		15		18	ns	4.5	Fig.8	

## TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS	
		74HCT									$V_{CC}$ (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min	typ.	max.	min	max.	min.	max.				
$V_{T+}$	positive-going threshold			2.0 2.1		2.0 2.1		2.0 2.1	V	4.5 5.5	Figs 6 and 7	
$V_{T-}$	negative-going threshold	0.70 0.80			0.64 0.74		0.60 0.70		V	4.5 5.5	Figs 6 and 7	
$V_H$	hysteresis ( $V_{T+} - V_{T-}$ )	0.17 0.17	0.23 0.23						V	4.5 5.5	Figs 6 and 7	

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TRANSFER CHARACTERISTIC WAVEFORMS

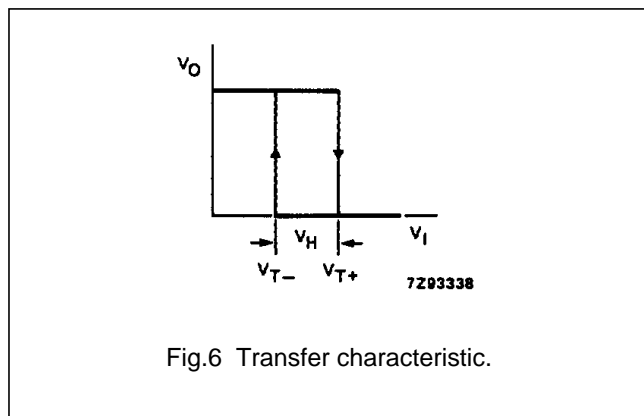


Fig.6 Transfer characteristic.

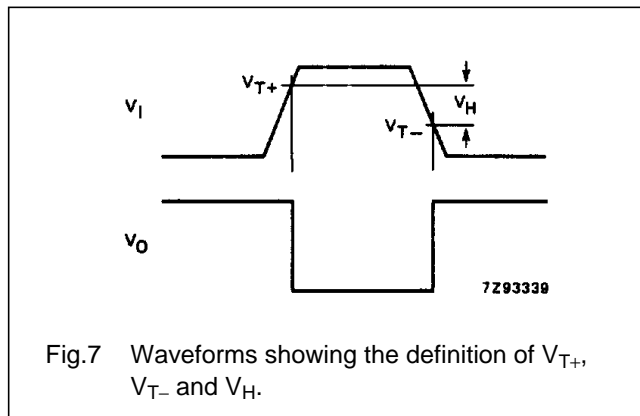


Fig.7 Waveforms showing the definition of  $V_{T+}$ ,  $V_{T-}$  and  $V_H$ .

AC WAVEFORMS

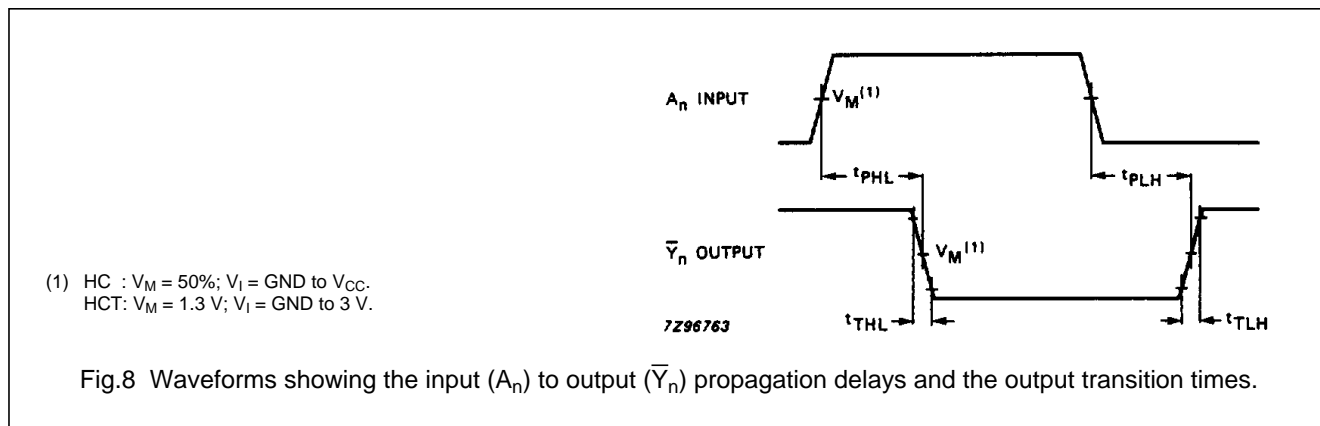


Fig.8 Waveforms showing the input ( $A_n$ ) to output ( $\bar{Y}_n$ ) propagation delays and the output transition times.

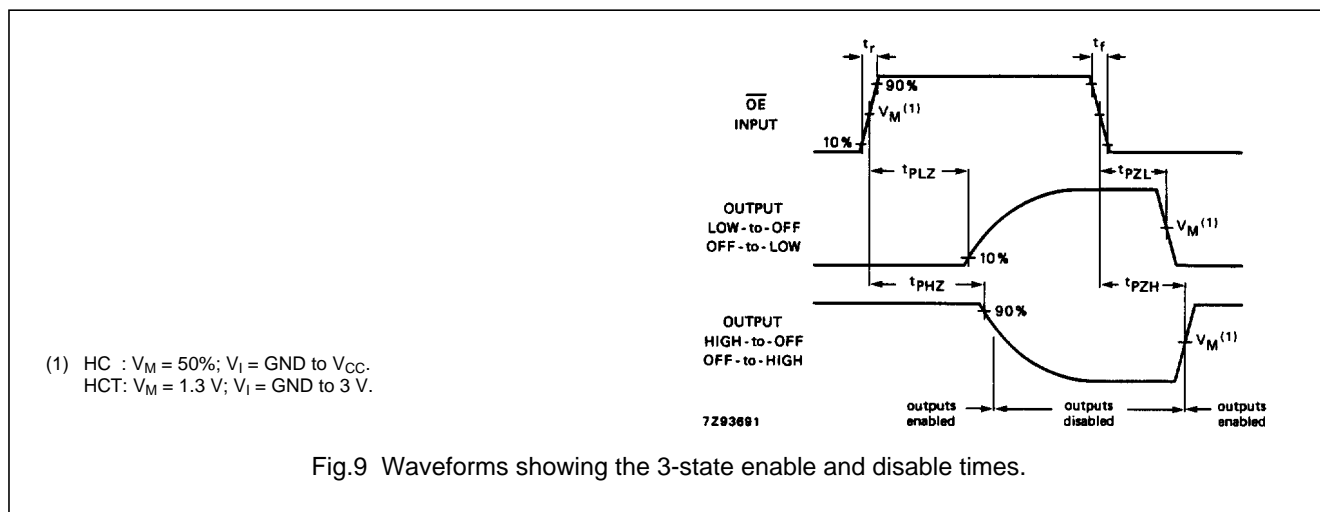


Fig.9 Waveforms showing the 3-state enable and disable times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

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Datasheets for electronics components.