

UT69RH051 Radiation-Hardened MicroController



FEATURES

- ❑ Three 16-bit timer/counters
 - High speed output
 - Compare/capture
 - Pulse width modulator
 - Watchdog timer capabilities
- ❑ 256 bytes of on-chip data RAM
- ❑ 32 programmable I/O lines
- ❑ 7 interrupt sources
- ❑ Programmable serial channel with:
 - Framing error detection
 - Automatic address recognition
- ❑ TTL and CMOS compatible logic levels
- ❑ 64K external data and program memory space
- ❑ MCS-51 fully compatible instruction set
- ❑ Flexible clock operation
 - 1Hz to 20MHz with external clock
 - 2MHz to 20MHz using internal oscillator with external crystal
- ❑ Radiation-hardened process and design; total dose irradiation testing MIL-STD-883 Method 1019
 - Total dose: 1.0E6 rads(Si)
 - Latchup immune
- ❑ Packaging options:
 - 40-pin 100-mil center DIP (0.600 x 2.00)
 - 44-lead 25-mil center Flatpack (0.670 x 0.800)
- ❑ Standard Microcircuit Drawing 5962-95638 available
 - QML Q & V compliant

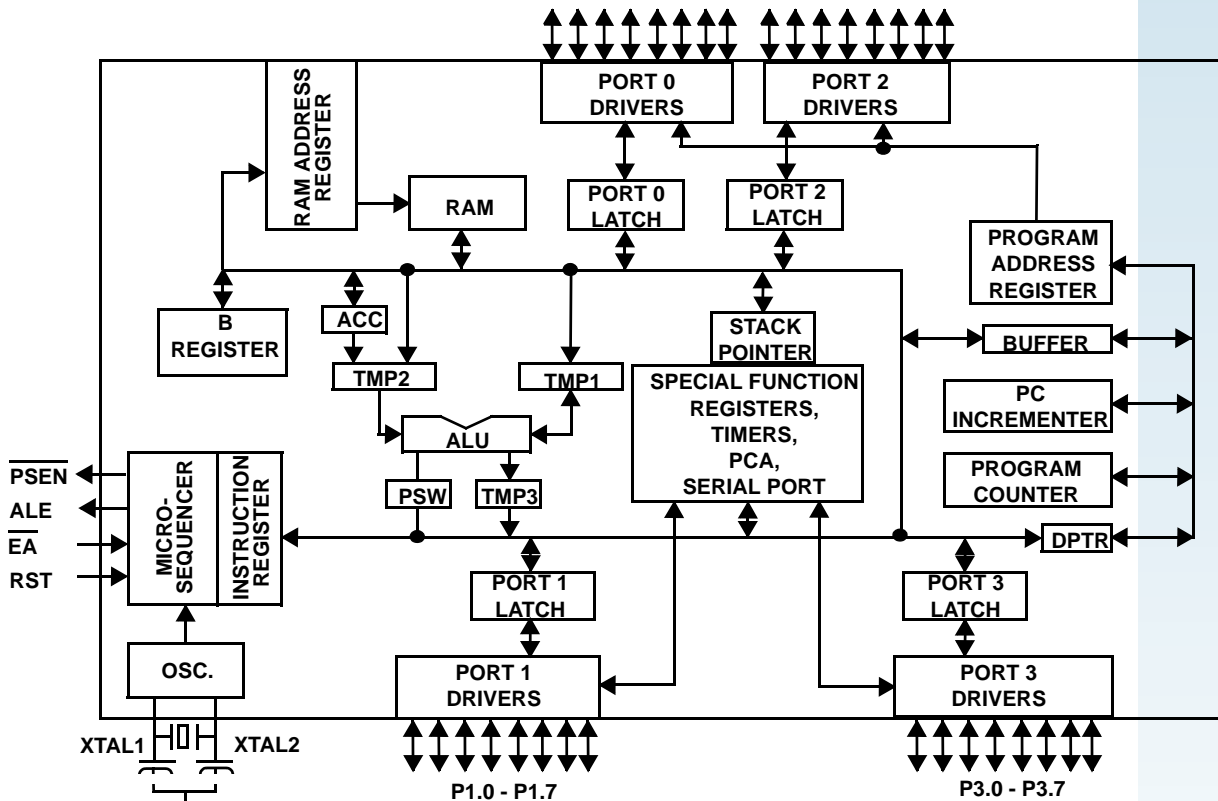


Figure 1. UT69RH051 MicroController Block Diagram

1.0 INTRODUCTION

The UT69RH051 is a radiation-tolerant 8-bit microcontroller that is pin equivalent to the MCS-51 industry standard microcontroller when in a 40-pin DIP. The UT69RH051's static design allows operation from 1Hz to 20MHz. This data sheet describes hardware and software interfaces to the UT69RH051.

2.0 SIGNAL DESCRIPTION

V_{DD}: +5V Supply voltage

V_{SS}: Circuit Ground

Port 0 (P0.0 - P0.7): Port 0 is an 8-bit port. Port 0 pins are used as the low-order multiplexed address and data bus during accesses to external program and data memory. Port 0 pins use internal pullups when emitting 1's and are TTL compatible.

Port 1 (P1.0 - P1.7): Port 1 is an 8-bit bidirectional I/O port with internal pullups. The output buffers can drive TTL loads. When the Port 1 pins have 1's written to them, they are pulled high by the internal pullups and can be used as inputs in this state. As inputs, any pins that are externally pulled low sources current because of the pullups. In addition, Port 1 pins have the alternate uses shown in table 1.

Port 2 (P2.0 - P2.7): Port 2 is an 8-bit port. Port 2 pins are used as the high-order address bus during accesses to external Program Memory and during accesses to external Data Memory that uses 16-bit addresses (i.e., MOVX@DPTR). Port 2 uses internal pullups when emitting 1's in this mode. During operations that do not require a 16-bit address, Port 2 emits the contents of the P2 Special Function Registers (SFR). The pins have internal pullups and drives TTL loads.

Port 3 (P3.0 - P3.7): Port 3 is an 8-bit bidirectional I/O port with internal pullups. The output buffers can drive TTL loads. When the Port 3 pins have 1's written to them, they are pulled high by the internal pullups and can be used as inputs in this state. As inputs, any pins that are externally pulled low sources current because of the pullups. In addition, Port 3 pins have the alternate uses shown in table 2.

Table 1. Port 1 Alternate Functions

| Port Pin | Alternate Name | Alternate Function |
|----------|----------------|--|
| P1.0 | T2 | External clock input to Timer/Counter 2 |
| P1.1 | T2EX | Timer/Counter 2 Capture/Reload trigger and direction control |
| P1.2 | ECI | External count input to PCA |
| P1.3 | CEX0 | External I/O for PCA capture/compare Module 0 |
| P1.4 | CEX1 | External I/O for PCA capture/compare Module 1 |
| P1.5 | CEX2 | External I/O for PCA capture/compare Module 2 |
| P1.6 | CEX3 | External I/O for PCA capture/compare Module 3 |
| P1.7 | CEX4 | External I/O for PCA capture/compare Module 4 |

Table 2. Port 3 Alternate Functions

| Port Pin | Alternate Name | Alternate Function |
|----------|--------------------------|-----------------------------------|
| P3.0 | RXD | Serial port input |
| P3.1 | TXD | Serial port output |
| P3.2 | $\overline{\text{INT0}}$ | External interrupt 0 |
| P3.3 | $\overline{\text{INT1}}$ | External interrupt 1 |
| P3.4 | T0 | External clock input for Timer 0 |
| P3.5 | T1 | External clock input for Timer 1 |
| P3.6 | $\overline{\text{WR}}$ | External Data Memory write strobe |
| P3.7 | $\overline{\text{RD}}$ | External Data Memory read strobe |

RST: Reset Input. A high on this input for 24 oscillator periods while the oscillator is running resets the device. All ports and SFRs reset to their default conditions. Internal data memory is undefined after reset. Program execution begins within 12 oscillator periods (one machine cycle) after the RST signal is brought low. RST contains an internal pulldown resistor to allow implementing power-up reset with only an external capacitor.

ALE: Address Latch Enable. The ALE output is a pulse for latching the low byte of the address during accesses to external memory. In normal operation, the ALE pulse is output every sixth oscillator cycle and may be used for external timing or clocking. However, during each access to external Data Memory (MOVX instruction), one ALE pulse is skipped.

PSEN: Program Store Enable. This active low signal is the read strobe to the external program memory. PSEN activates every sixth oscillator cycle except that two PSEN activations are skipped during external data memory accesses.

EA: External Access Enable. This pin should be strapped to V_{SS} (Ground) for the UT69RH051.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

2.1 Hardware/Software Interface

2.1.1 Memory

The UT69RH051 has a separate address space for Program and Data Memory. Internally, the UT69RH051 contains 256 bytes of Data Memory. It addresses up to 64Kbytes of external Data Memory and 64Kbytes of external Program Memory.

2.1.1.1 Program Memory

There is no internal program memory in the UT69RH051. All program memory is accessed as external through ports P0 and P2. The EA pin must be tied to V_{SS} (ground) to enable access to external locations 0000_H through 7FFF_H. Following reset, the UT69RH051 fetches the first instruction at address 0000h.

2.1.1.2 Data Memory

The UT69RH051 implements 256 bytes of internal data RAM. The upper 128 bytes of this RAM occupy a parallel address space to the SFRs. The CPU determines if the internal access to an address above 7F_H is to the upper 128 bytes of RAM or to the SFR space by the addressing mode of the instruction. If direct addressing is used, the access is to the SFR space. If indirect addressing is used, the access is to the internal RAM. Stack operations are indirectly addressed so the upper portion of RAM can be used as stack space. Figure 3 shows the organization of the internal Data Memory.

The first 32 bytes are reserved for four register banks of eight bytes each. The processor uses one of the four banks as its working registers depending on the RS1 and RS0 bits in the PSW SFR. At reset, bank 0 is selected. If four register banks are not required, use the unused banks as general purpose scratch pad memory. The next 16 bytes (128 bits) are individually bit addressable. The remaining bytes are byte addressable and can be used as general purpose scratch pad memory. For addresses 0 - 7F_H, use either direct or indirect addressing. For addresses larger than 7F_H, use only indirect addressing.

In addition to the internal Data Memory, the processor can access 64Kbytes of external Data Memory. The MOVX instruction accesses external Data Memory.

2.1.2 Special Function Registers

Table 3 contains the SFR memory map. Unoccupied addresses are not implemented on the device. Read accesses to these addresses will return unknown values and write accesses will have no effect.

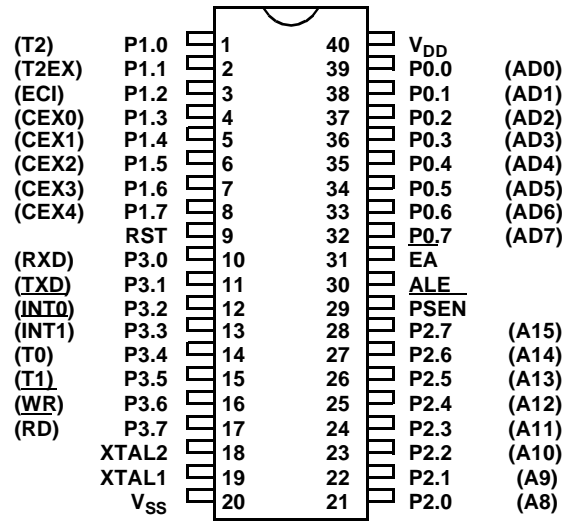


Figure 2a. UT69RH051 40-Pin DIP Connections

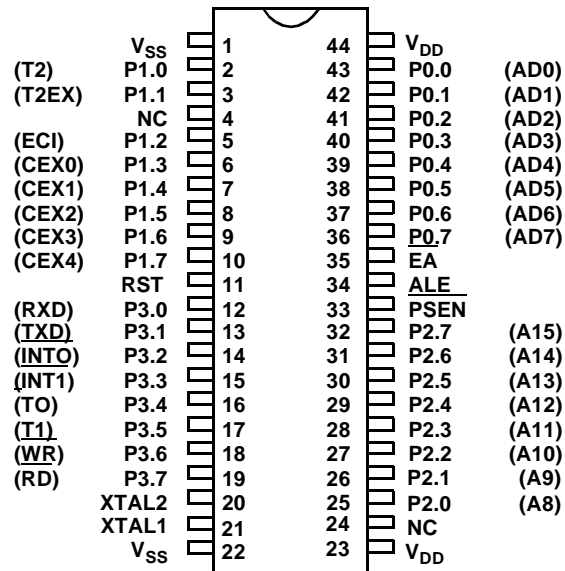


Figure 2b. UT69RH051 44-Pin Flatpack Connections

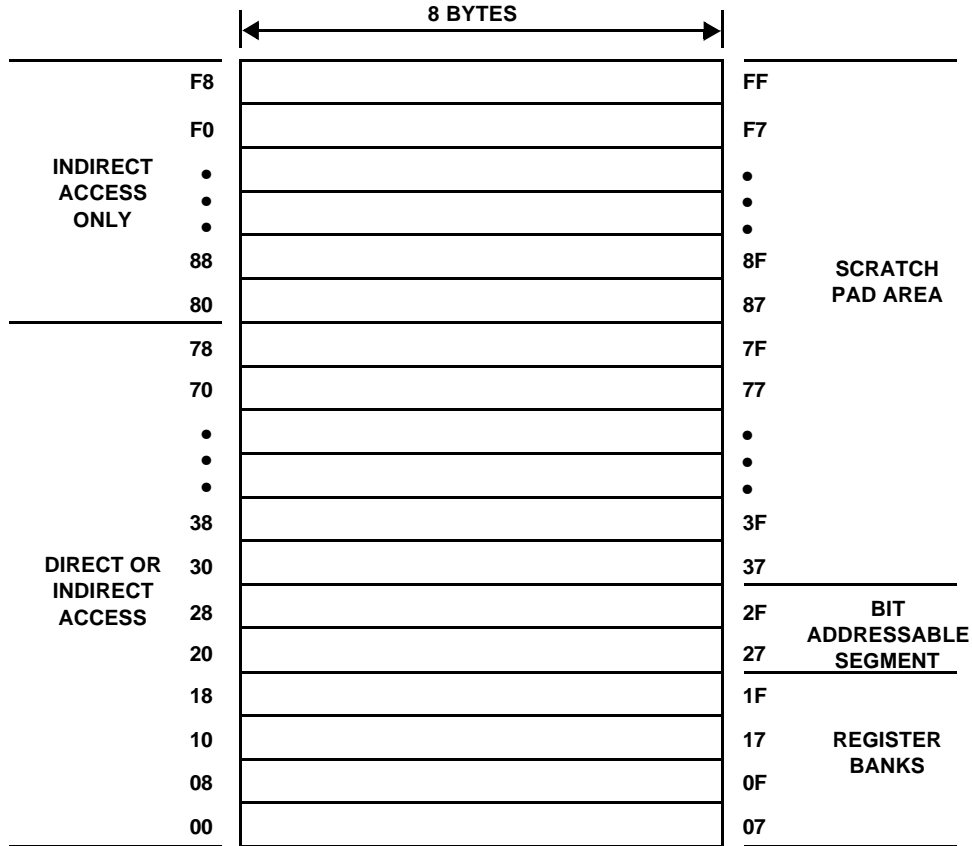


Figure 3. Internal Data Memory Organization

2.1.3 Reset

The reset input is the RST pin. To reset, hold the RST pin high for a minimum of 24 oscillator periods while the oscillator is running. The CPU generates an internal reset from the external signal. The port pins are driven to the reset state as soon as a valid high is detected on the RST pin.

While RST is high, $\overline{\text{PSEN}}$ and the port pins are pulled high; ALE is pulled low. All SFRs are reset to their reset values as shown in table 3. The internal Data Memory content is indeterminate.

The processor will begin operation one machine cycle after the RST line is brought low. A memory access occurs immediately after the RST line is brought low, but the data is not brought into the processor. The memory access repeats on the next machine cycle and actual processing begins at that time.

Table 3. SFR Memory Registers

| | | | | | | | | | |
|----|-------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|------------------|----|
| F8 | | CH 00000000 | CCAP0H XXXXXXXX | CCAP1H XXXXXXXX | CCAP2H XXXXXXXX | CCAP3H XXXXXXXX | CCAP4H XXXXXXXX | | FF |
| F0 | B 00000000 | | | | | | | | F7 |
| E8 | | CL 00000000 | CCAP0L XXXXXXXX | CCAP1L XXXXXXXX | CCAP2L XXXXXXXX | CCAP3L XXXXXXXX | CCAP4L XXXXXXXX | | EF |
| E0 | ACC 00000000 | | | | | | | | E7 |
| D8 | CCON 00X00000 | CMOD OOXXX000 | CCAPM0 X00000000 | CCAPM1 X00000000 | CCAPM2 X00000000 | CCAPM3 X00000000 | CCAPM4 X00000000 | | DF |
| D0 | PSW 00000000 | | | | | | | | D7 |
| C8 | T2CON 00000000 | T2MOD XXXXXXXX00 | RCAP2L 00000000 | RCAP2H 00000000 | TL2 00000000 | TH2 00000000 | | | CF |
| C0 | | | | | | | | | C7 |
| B8 | IP X0000000 | SADEN 00000000 | | | | | | | BF |
| B0 | P3 11111111 | | | | | | | IPH X00000000 | B7 |
| A8 | IE 00000000 | SADDR 00000000 | | | | | | | AF |
| A0 | P2 11111111 | | | | | | | | A7 |
| 98 | SCON 00000000 | SBUF XXXXXXXXXX | | | | | | | 9F |
| 90 | P1 11111111 | | | | | | | | 97 |
| 88 | TCON 00000000 | TMOD 00000000 | TL0 00000000 | TL1 00000000 | TH0 00000000 | TH1 00000000 | | | 8F |
| 80 | P0 11111111 | SP 00000111 | DPL 00000000 | DPH 00000000 | | | | PCON 00XX00XX | 87 |

Notes:

1. Values shown are the reset values of the registers.
2. X = undefined.

3.0 RADIATION HARDNESS

The UT69RH051 incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the

circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

RADIATION HARDNESS DESIGN SPECIFICATIONS ¹

| | | |
|-----------------------------------|---------|--------------------------------|
| Total Dose | 1.0E6 | rad(Si) |
| LET Threshold | 20 | MeV-cm ² /mg |
| Neutron Fluence | 1.0E14 | n/cm ² |
| Saturated Cross-Section (1Kx8) | 1E-4 | cm ² /device |
| Single Event Upset | 1.3E-7 | errors/device-day ² |
| Single Event Latchup ¹ | LET>126 | MeV-cm ² /mg |

Note:

1. Worst case temperature $T_A = +125^{\circ}\text{C}$.
2. Adams 90% worst case environment (geosynchronous).

4.0 ABSOLUTE MAXIMUM RATINGS ¹

(Referenced to V_{SS})

| SYMBOL | PARAMETER | LIMITS | UNITS |
|---------------|---|------------------------------|-----------------------------|
| V_{DD} | DC Supply Voltage | -0.5 to 7.0 | V |
| $V_{I/O}$ | Voltage on Any Pin | -0.5 to $V_{DD}+0.3\text{V}$ | V |
| T_{STG} | Storage Temperature | -65 to +150 | $^{\circ}\text{C}$ |
| P_D | Maximum Power Dissipation | 750 | mW |
| T_J | Maximum Junction Temperature | 175 | $^{\circ}\text{C}$ |
| Θ_{JC} | Thermal Resistance, Junction-to-Case ² | 10 | $^{\circ}\text{C}/\text{W}$ |
| I_I | DC Input Current | ± 10 | mA |

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012.

5.0 DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

$V_{DD} = 5.0V \pm 10\%$; $T_A = -55^\circ C < T_C < +125^\circ C$

| SYMBOL | PARAMETER | CONDITION | MINIMUM | MAXIMUM | UNIT |
|------------|---|--|---------|----------|---------|
| V_{IL} | Low-level Input Voltage | | | 0.8 | V |
| V_{IH} | High-level Input Voltage (except XTAL, RST) | | 2.0 | | V |
| V_{IH1} | High-level Input Voltage (XTAL) | | 3.85 | | V |
| V_{OL} | Low-level Output Voltage ¹ (Ports 1, 2 and 3) | $I_{OL} = 100\mu A$ | | 0.3 | V |
| | | $I_{OL} = 1.6mA$ | | 0.45 | V |
| | | $I_{OL} = 3.5mA$ | | 1.0 | V |
| V_{OL1} | Low-level Output Voltage ^{1,2} (Port 0, ALE, PSEN, PROG) | $I_{OL} = 200\mu A$ | | 0.3 | V |
| | | $I_{OL} = 3.2mA$ | | 0.45 | V |
| | | $I_{OL} = 7.0mA$ | | 1.0 | V |
| V_{OH} | High-level Output Voltage ³ (Ports 1, 2, and 3 ALE and PSEN) | $I_{OH} = -10\mu A$ | 4.2 | | V |
| | | $I_{OH} = -30\mu A$ | 3.8 | | V |
| | | $I_{OH} = -60\mu A$ | 3.0 | | V |
| V_{OH1} | High-level Output Voltage (Port 0 in External Bus Mode) | $I_{OH} = -200\mu A$ | 4.2 | | V |
| | | $I_{OH} = -3.2mA$ | 3.8 | | V |
| | | $I_{OH} = -7.0mA$ | 3.0 | | V |
| I_{IL} | Logical 0 Input Current (Ports 1, 2, and 3) | $V_{IN} = 0.0V$ | | -50 | μA |
| | | $V_{CC} = 5.5V$ | | -65 | |
| I_{IL} | Logical 0 Input Current (XTAL 1) | $V_{IN} = 0.0V$ $V_{CC} = 5.5V$ | | -65 | μA |
| I_{LI} | Input Leakage Current (Port 0) | $V_{IN} = 0.0V$ or V_{CC} | | ± 25 | μA |
| | | $V_{CC} = 5.5V$ | | ± 65 | |
| I_{LI} | Input Leakage Current (XTAL1) | $V_{IN} = 0.0V$ or V_{CC} $V_{CC} = 5.5V$ | | ± 65 | μA |
| C_{IO}^4 | Pin Capacitance | @ 1MHZ, 25°C | | 15 | pF |
| I_{DD} | Power Supply Current: | @ 16MHz | | 95 | mA |
| | | @ 20 MHz | | 120 | |

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883.

1. Under steady state (non-transient) conditions, I_{OL} must be limited externally as follows:

Maximum I_{OL} per port pin: 10mA

Maximum I_{OL} per 8-bit port- Port 0: 26mA

Ports 1, 2, & 3: 15mA

Maximum total I_{OL} for all output pins: 71mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1 to 0 transitions during bus operations. In applications where capacitance loading exceeds 100 pF, the noise pulse on the ALE may exceed 0.8V. In these cases, it may be desirable to qualify ALE with a schmitt trigger or use an address latch with a schmitt trigger strobe input.

3. Capacitive loading ports 0 and 2 cause the V_{OH} on ALE and \overline{PSEN} to drop below the $V_{DD}-0.3$ specification when the address lines are stabilizing.

4. Capacitance measured for initial qualification or design changes which may affect the value.

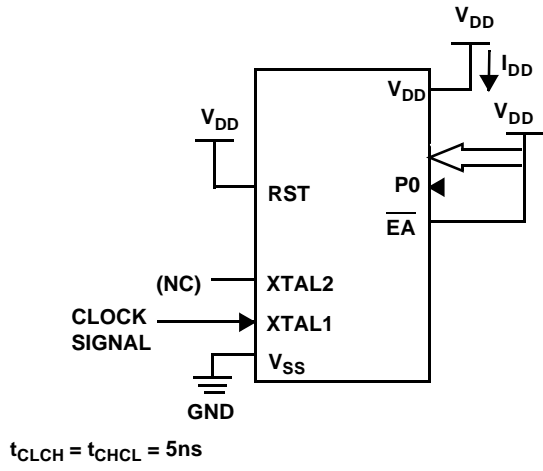


Figure 4. I_{DD} Test Condition, Active Mode
All other pins
disconnected

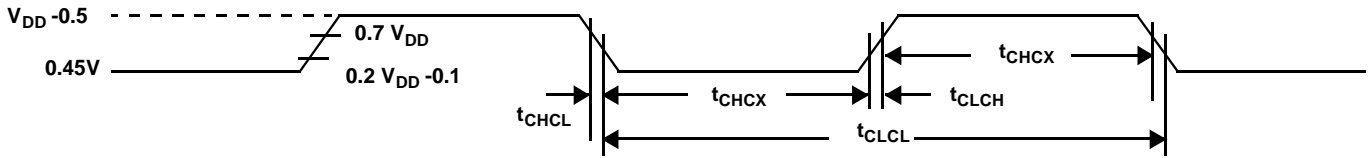


Figure 5. Clock Signal Waveform for I_{DD} Tests in Active and Idle Modes
 $t_{CLCH} = t_{CHCL} = 5ns$

6.0 AC CHARACTERISTICS READ CYCLE (Post-Radiation)*

($V_{DD} = 5.0V \pm 10\%$; $-55^{\circ}C < T_C < +125^{\circ}C$)

| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNIT |
|--------------|---|------------------|------------------|------|
| t_{CLCL} | Clock Period | 50 | | ns |
| $1/t_{CLCL}$ | Oscillator Frequency | | 20 | MHz |
| t_{LHLL} | ALE Pulse Width | $2 t_{CLCL}-40$ | | ns |
| t_{AVLL} | Address Valid to ALE Low | $t_{CLCL}-40$ | | ns |
| t_{LLAX}^1 | Address Hold after ALE Low | $t_{CLCL}-30$ | | ns |
| t_{LLIV} | ALE Low to Valid Instruction | | $4 t_{CLCL}-100$ | ns |
| t_{LLPL} | ALE Low to \overline{PSEN} Low | $t_{CLCL}-30$ | | ns |
| t_{PLPH} | \overline{PSEN} Pulse Width | $3 t_{CLCL}-45$ | | ns |
| t_{PLIV} | \overline{PSEN} Low to Valid Instruction In | | $3 t_{CLCL}-105$ | ns |
| t_{PXIX}^1 | Input Instruction Hold after \overline{PSEN} | 0 | | ns |
| t_{PXIZ}^1 | Input Instruction Float after \overline{PSEN} | | $t_{CLCL}-25$ | ns |
| t_{AVIV} | Address to Valid Instruction In | | $5 t_{CLCL}-105$ | ns |
| t_{PLAZ}^1 | \overline{PSEN} Low to Address Float | | 10 | ns |
| t_{RLRH} | \overline{RD} Pulse Width | $6 t_{CLCL}-100$ | | ns |
| t_{WLWH} | \overline{WR} Pulse Width | $6 t_{CLCL}-100$ | | ns |
| t_{RLDV} | \overline{RD} Low to Valid Data In | | $5 t_{CLCL}-165$ | ns |
| t_{RHDX}^1 | Data Hold After \overline{RD} High | 0 | | ns |
| t_{RHDZ}^1 | Data Float After \overline{RD} High | | $2 t_{CLCL}-60$ | ns |
| t_{LLDV} | ALE Low Valid Data In | | $8 t_{CLCL}-150$ | ns |
| t_{AVDV} | Address to Valid Data In | | $9 t_{CLCL}-165$ | ns |
| t_{LLWL} | ALE Low to \overline{RD} or \overline{WR} Low | $3 t_{CLCL}-50$ | $3 t_{CLCL}+50$ | ns |
| t_{AVWL} | Address Valid to \overline{WR} Low | $4 t_{CLCL}-130$ | | ns |
| t_{QVWX} | Data Valid Before \overline{WR} High | $t_{CLCL}-33$ | | ns |
| t_{WHQX} | Data Hold After \overline{WR} High | $t_{CLCL}-33$ | | ns |
| t_{QVWH} | Data Valid to \overline{WR} High | $7 t_{CLCL}-150$ | | ns |
| t_{RLAZ}^1 | \overline{RD} Low to Address Float | | 0 | ns |
| t_{WHLH} | \overline{RD} or \overline{WR} High to ALE High | $t_{CLCL}-40$ | $t_{CLCL}+40$ | ns |

Note:

* Post-radiation performance guaranteed at $25^{\circ}C$ per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

1. Guaranteed, but not tested.

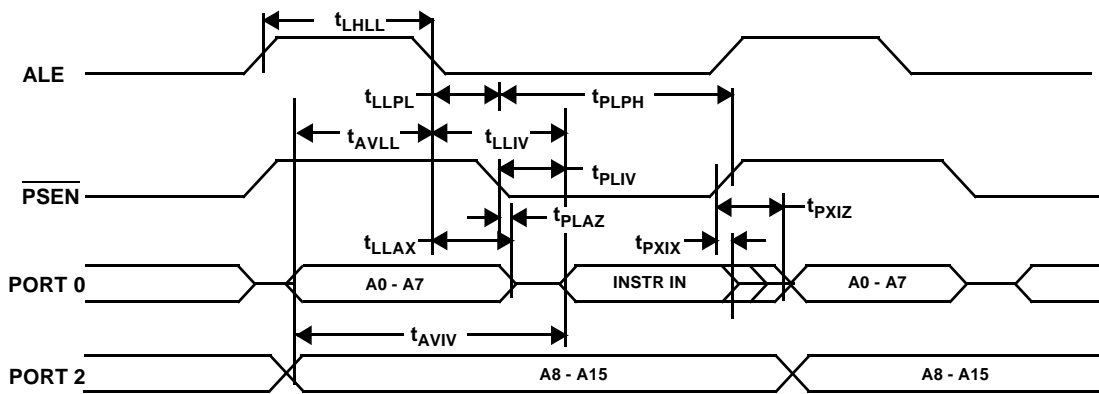


Figure 6. External Program Memory Read Timing Waveforms

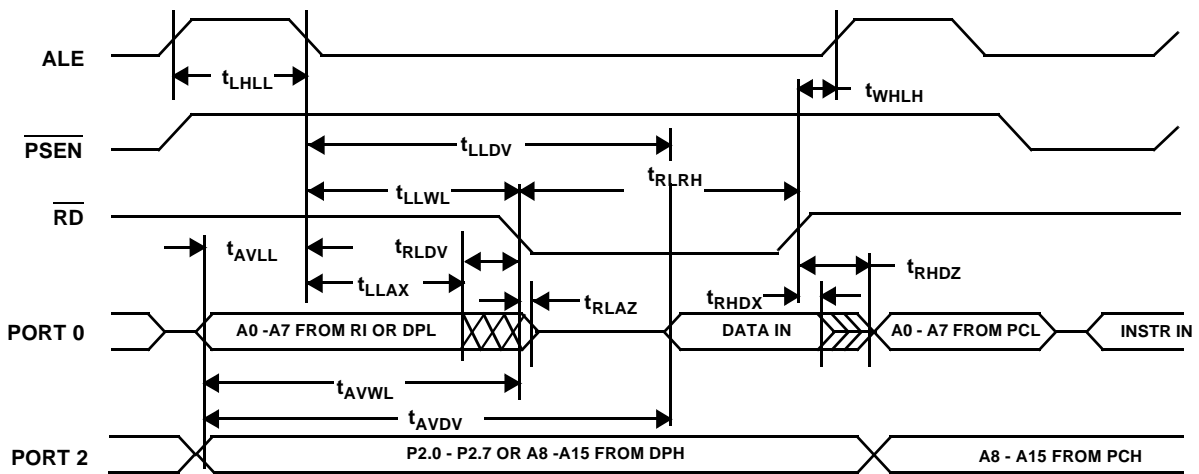


Figure 7. External Data Memory Read Cycle Waveforms

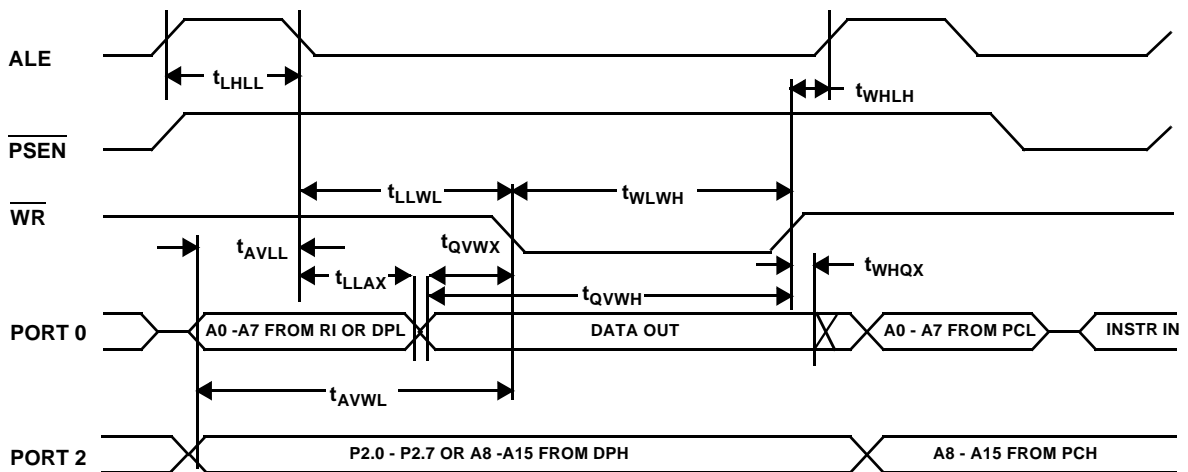


Figure 8. External Data Memory Write Cycle Waveforms

7.0 SERIAL PORT TIMING CHARACTERISTICS

($V_{DD} = 5.0V \pm 10\%$; $-55^{\circ}C < T_C < +125^{\circ}C$)

| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNIT |
|--------------|--|-------------------|-------------------|------|
| t_{XLXL}^1 | Serial Port Clock Period | $12 t_{CLCL}-10$ | $12 t_{CLCL}+10$ | ns |
| t_{QVXH} | Output Data Setup to Clock Rising Edge | $10 t_{CLCL}-133$ | | ns |
| t_{XHQX} | Output Data Hold after Clock Rising Edge | $2 t_{CLCL}-70$ | | ns |
| t_{XHDX}^1 | Input Data Hold after Clock Rising Edge | 0 | | ns |
| t_{XHDV} | Clock Rising Edge to Input Data Valid | | $10 t_{CLCL}-133$ | ns |

Note:

1. Guaranteed, but not tested.

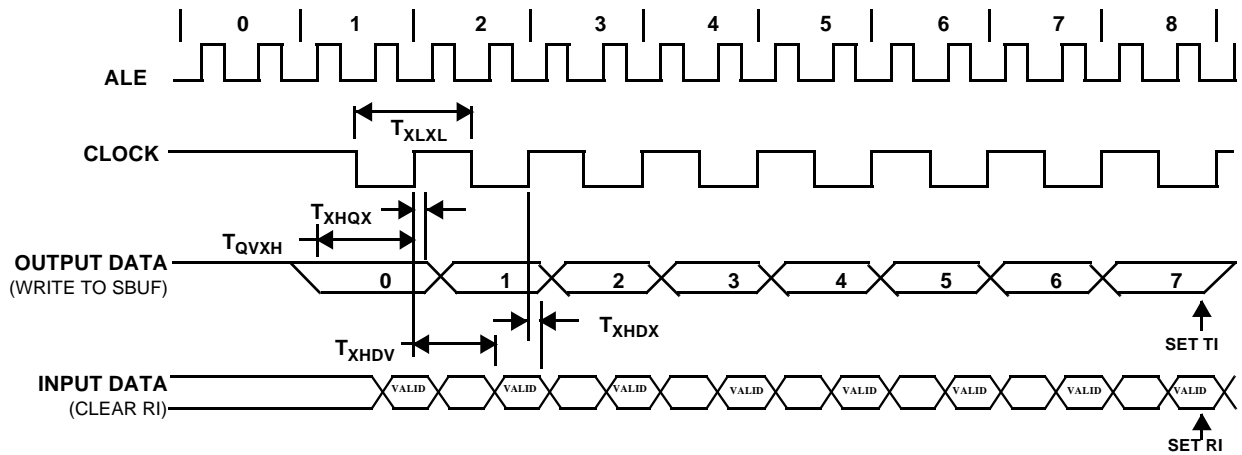


Figure 9. Serial Port Timing Waveforms

8.0 EXTERNAL CLOCK DRIVE TIMING CHARACTERISTICS

| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNIT |
|--------------|----------------------|---------|---------|------|
| $1/t_{CLCL}$ | Oscillator Frequency | | 20 | MHz |
| t_{CHCX} | High Time | 16 | | ns |
| t_{CLCX} | Low Time | 16 | | ns |
| t_{CLCH} | Rise Time | | 20 | ns |
| t_{CHCL} | Fall Time | | 20 | ns |

Note:

1. Guaranteed, but not tested.

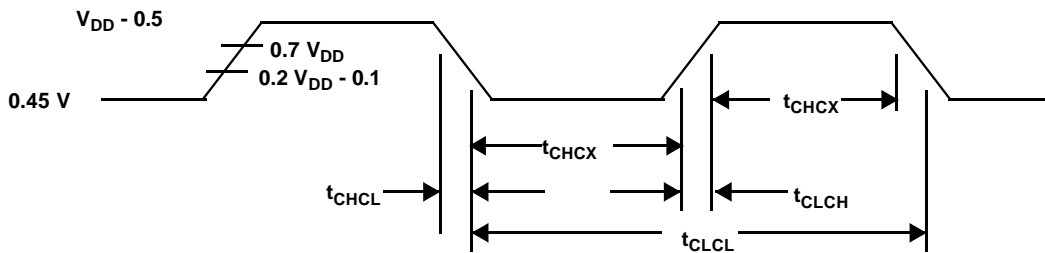


Figure 10. External Clock Drive Timing Waveforms

9.0 PACKAGING

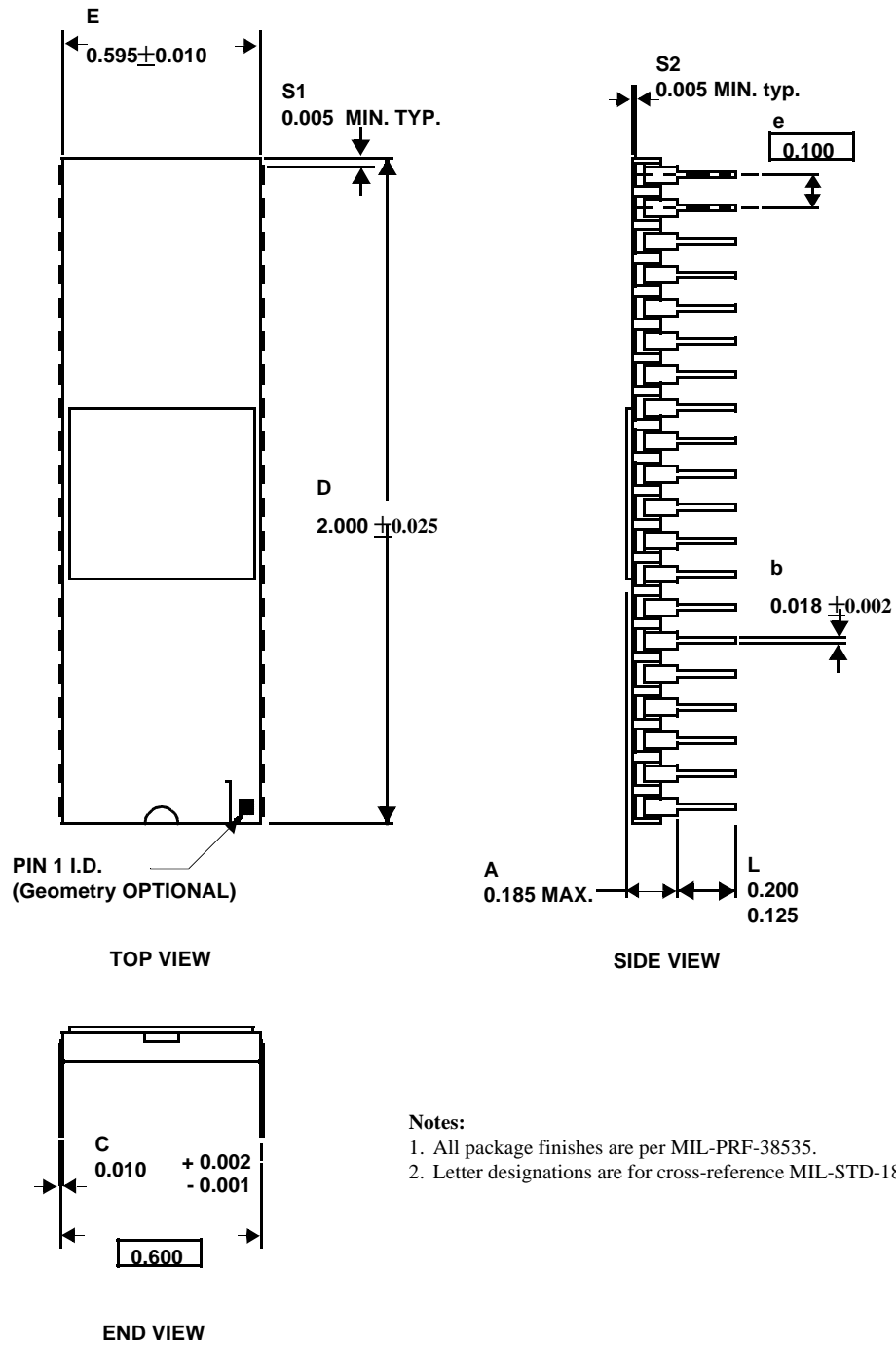
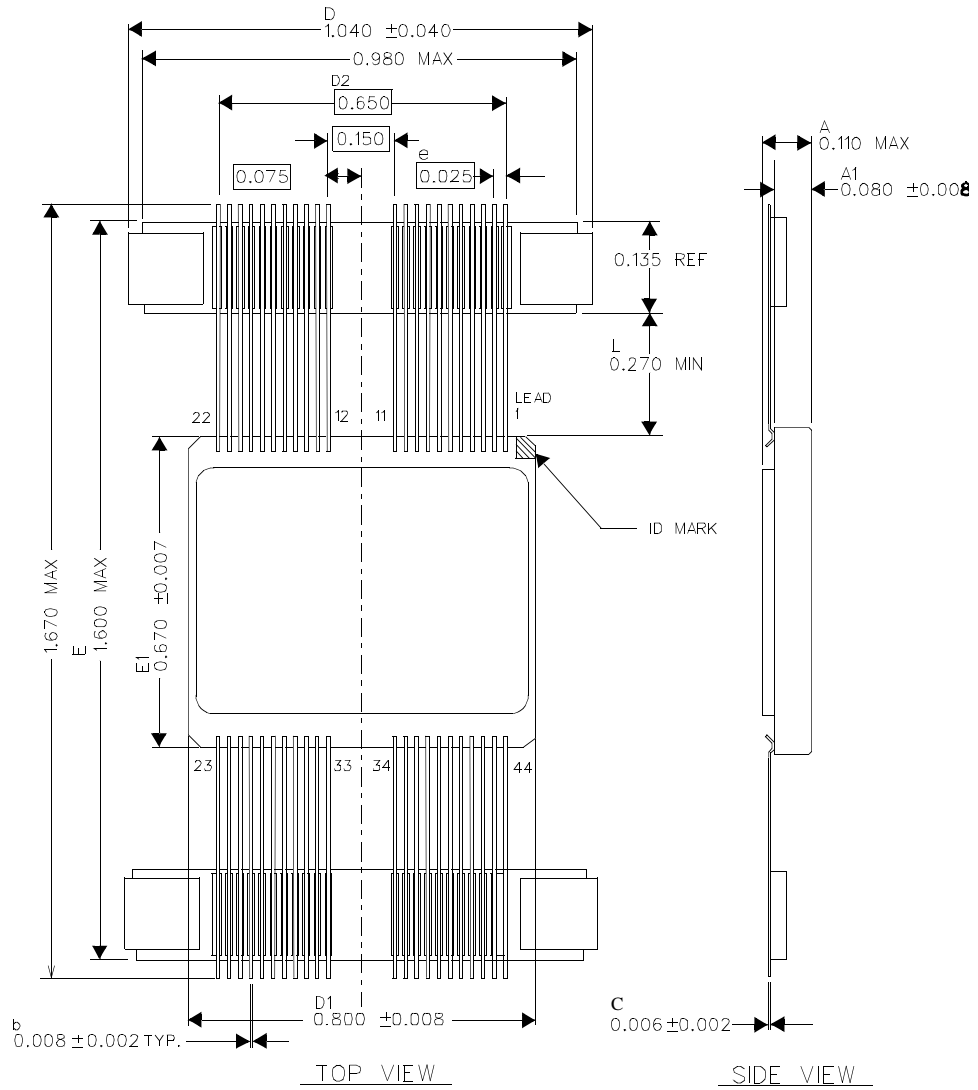


Figure 11. 40-pin Side-Brazed DIP



Notes:

1. All exposed metalized areas to be plated per MIL-PRF-38535.
2. Dimension letters refer to MIL-STD-1835.

Figure 12. 44-Lead Flatpack

APPENDIX A
Difference Between Industry Standard and UT69RH051

The areas in which the UT69RH051 differs from the industry standard will be covered in this section. In this discussion, industry standard will be used generically to refer to all speed grades including the 20MHz.

1.0 RESET

The UT69RH051 requires the RST input to be held high for at least 24 oscillator periods to guarantee the reset is completed in the chip. Also, the port pins are reset asynchronously as soon as the RST pin is pulled high. On the UT69RH051 all portions of the chip are reset synchronously when the RST pin is high during a rising edge of the input clock. When coming out of reset, the industry standard takes 1 to 2 machine cycles to begin driving ALE and PSEN immediately after the RST is removed, but the access during the first machine cycle after reset is ignored by the processor. The second cycle will repeat the access and processing will begin.

2.0 POWER SAVING MODES OF OPERATION

2.1 Idle Mode

Idle mode and the corresponding control bit in the PCON SFR have not been implemented in the UT69RH051. Setting the idle control bit has no effect.

2.2 Power Down Mode

Power down mode and the corresponding control bit in the PCON register have not been implemented in the UT69RH051. Setting the power down control bit has no effect. Also, the Power Off Flag in the PCON has not been implemented.

3.0 ON CIRCUIT EMULATION

The On Circuit Emulation mode of operation in the industry standard has not been implemented in the UT69RH051.

4.0 OPERATING CONDITIONS

The operating voltage range for the industry standard is $5V \pm 20\%$. The operating temperature range is 0°C to 70°C . On the UT69RH051, the operating voltage range is $5V \pm 10\%$. The operating temperature range is -55°C to $+125^{\circ}\text{C}$.

APPENDIX B

Impact of External Program ROM

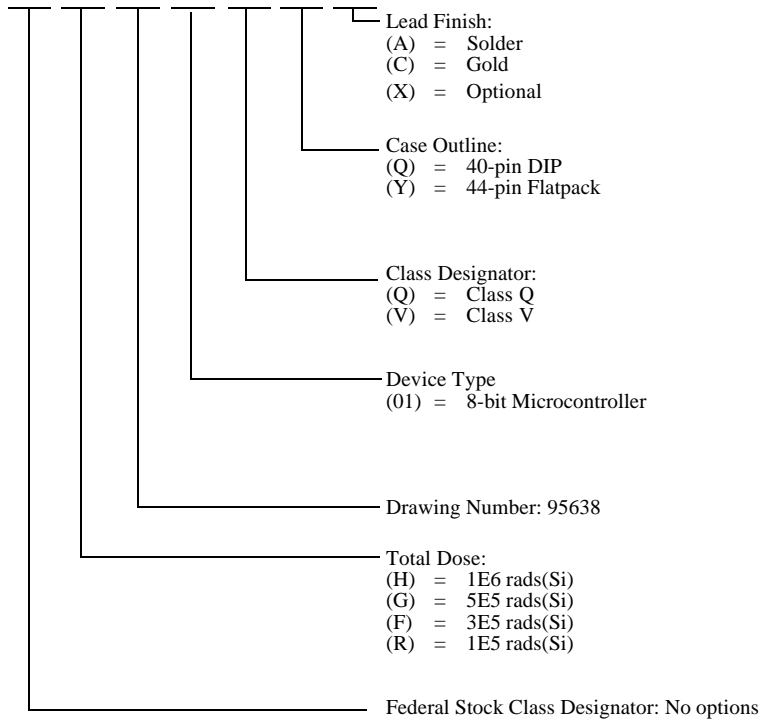
The 8051 family of microcontrollers, including the industry standards, use ports 0 and 2 to access external memory. In implementations with external program memory, these two ports

are dedicated to the program ROM interface and can not be used as Input/Output ports. The UT69RH051 uses external program ROM, so ports 0 and 2 will not be available for I/O.

ORDERING INFORMATION

UT69RH051 Microcontroller: SMD

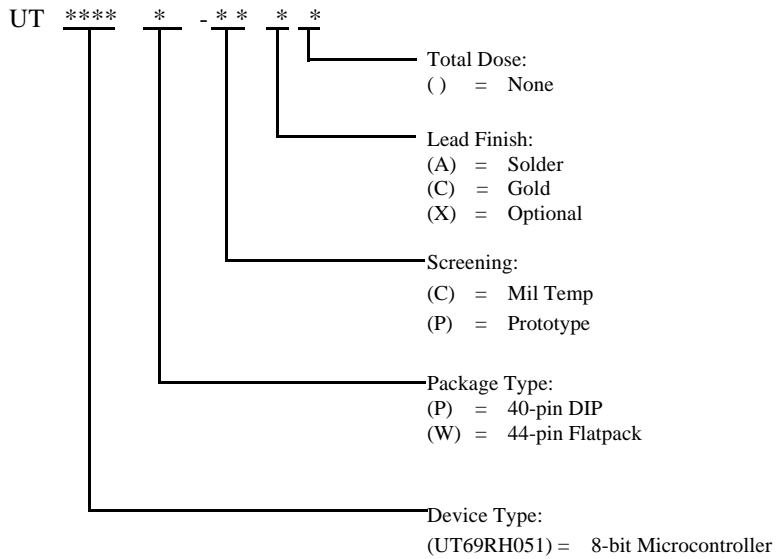
5962 * 95638 * * * *



Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

UT69RH051 Microcontroller



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Radiation characteristics are neither tested nor guaranteed and may not be specified.
4. Devices have prototype assembly and are tested at 25°C only. Radiation characteristics are neither tested nor guaranteed and may not be specified.

Notes