

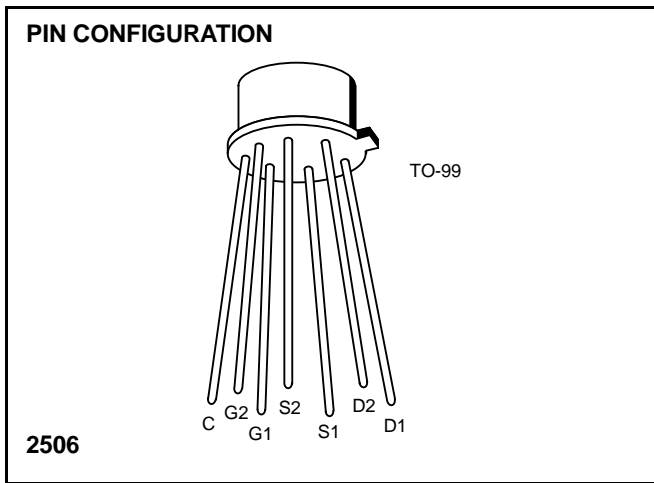
# Dual P-Channel Enhancement Mode MOSFET General Purpose Amplifier



## 3N190 / 3N191

### FEATURES

- Very High Input Impedance
- High Gate Breakdown 3N190-3N191
- Low Capacitance



### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Drain-Source or Drain-Gate Voltage (Note 1)	
3N190, 3N191	40V
Transient Gate-Source Voltage (Note 1 and 2)	$\pm 125\text{V}$
Gate-Gate Voltage	$\pm 80\text{V}$
Drain Current (Note 1)	50mA
Storage Temperature	$-65^\circ\text{C}$ to $+200^\circ\text{C}$
Operating Temperature	$-55^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	
One Side	300mW
Both Sides	525mW
Total Derating above $25^\circ\text{C}$	4.2mW/ $^\circ\text{C}$

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ORDERING INFORMATION

Part	Package	Temperature Range
3N190-91	Hermetic TO-99	$-55^\circ\text{C}$ to $+150^\circ\text{C}$
X3N190-91	Sorted Chips in Carriers	$-55^\circ\text{C}$ to $+150^\circ\text{C}$

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

SYMBOL	PARAMETER	3N190/91		UNITS	TEST CONDITIONS
		MIN	MAX		
$I_{GSSR}$	Gate Reverse Current		10	pA	$T_A = +125^\circ\text{C}$
$I_{GSSF}$	Gate Forward Current		-10		
			-25		
$BV_{DSS}$	Drain-Source Breakdown Voltage	-40		V	$I_D = -10\mu\text{A}$
$BV_{SDS}$	Source-Drain Breakdown Voltage	-40			$I_S = -10\mu\text{A}, V_{BD} = 0$
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0		$V_{DS} = -15\text{V}, I_D = -10\mu\text{A}$
		-2.0	-5.0		$V_{DS} = V_{GS}, I_D = -10\mu\text{A}$
$V_{GS}$	Gate Source Voltage	-3.0	-6.5		$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}$
$I_{DSS}$	Zero Gate Voltage Drain Current		-200		$V_{DS} = -15\text{V}$
$I_{SDS}$	Source Drain Current		-400		$V_{SD} = -15\text{V}, V_{DB} = 0$
$r_{DS(on)}$	Drain-Source on Resistance		300		ohms
$I_{D(on)}$	On Drain Current	-5.0	-30.0	mA	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}$

**ELECTRICAL CHARACTERISTICS** (Continued) ( $T_A = 25^\circ\text{C}$  and  $V_{BS} = 0$  unless otherwise specified)

SYMBOL	PARAMETER	3N190/91		UNITS	TEST CONDITIONS	
		MIN	MAX			
$g_{fs}$	Forward Transconductance (Note 3)	1500	4000	$\mu\text{S}$	$V_{DS} = -15\text{V}, I_D = -10\text{mA}$	$f = 1\text{kHz}$
$Y_{os}$	Output Admittance		300			$\text{pF}$
$C_{iss}$	Input Capacitance Output Shorted (Note 5)		4.5			
$C_{rss}$	Reverse Transfer Capacitance (Note 5)		1.0			
$C_{oss}$	Output Capacitance Input Shorted (Note 5)		3.0			

**SWITCHING CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  and  $V_{BS} = 0$  unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
$t_{d(on)}$	Turn On Delay Time		15	ns	$V_{DD} = -15\text{V}, I_D = -10\text{mA}, R_G = R_L = 1.4\text{k}\Omega$ (Note 5)
$t_r$	Rise Time		30		
$t_{off}$	Turn Off Time		50		

**MATCHING CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  and  $V_{BS} = 0$  unless otherwise specified) 3N188 and 3N190

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
$Y_{fs1} / Y_{fs2}$	Forward Transconductance Ratio	0.85	1.0		$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}, f = 1\text{kHz}$
$V_{GS1-2}$	Gate Source Threshold Voltage Differential		100	mV	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}$
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)		100	$\mu\text{V}/^\circ\text{C}$	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}, T = -55^\circ\text{C} \text{ to } +25^\circ\text{C}$
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)		100	$\mu\text{V}/^\circ\text{C}$	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}, T = +25^\circ\text{C} \text{ to } +125^\circ\text{C}$

- NOTES:**
1. Per transistor.
  2. Approximately doubles for every  $10^\circ\text{C}$  increase in  $T_A$ .
  3. Pulse test duration =  $300\mu\text{s}$ ; duty cycle  $\leq 3\%$ .
  4. Measured at end points,  $T_A$  and  $T_B$ .
  5. For design reference only, not 100% tested.