NEC

MOS INTEGRATED CIRCUIT

μPD160062

420-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALE)

DESCRIPTION

The μPD160062 is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scale. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules.

Because the output dynamic range is as large as V_{SS2} +0.1 V to V_{DD2} –0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity.

Assuring a clock frequency of 45 MHz when driving at 2.3 V, this driver is applicable to SXGA+ standard TFT-LCD panels.

FEATURES

- CMOS level input (2.3 to 3.6 V)
- 420 outputs
- Input of 6 bits (gray scale data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter (R-DAC)
- Logic power supply voltage (V_{DD1}) : 2.3 to 3.6 V
- Driver power supply voltage (V_{DD2}) : 8.0 to 9.0 V
- High-speed data transfer: f_{CLK} = 45 MHz (internal data transfer speed when operating at V_{DD1} = 2.3 V)
- Output dynamic range V_{SS2} +0.1 V to V_{DD2} –0.1 V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Input data inversion function (capable of controlling by each input port) (POL21, POL22)
- Current consumption control function (LPC, HPC, Bcont)
- Slim chip

ORDERING INFORMATION

Part Number	Package
μPD160062N-×××	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, please contact one of our sales representatives.

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Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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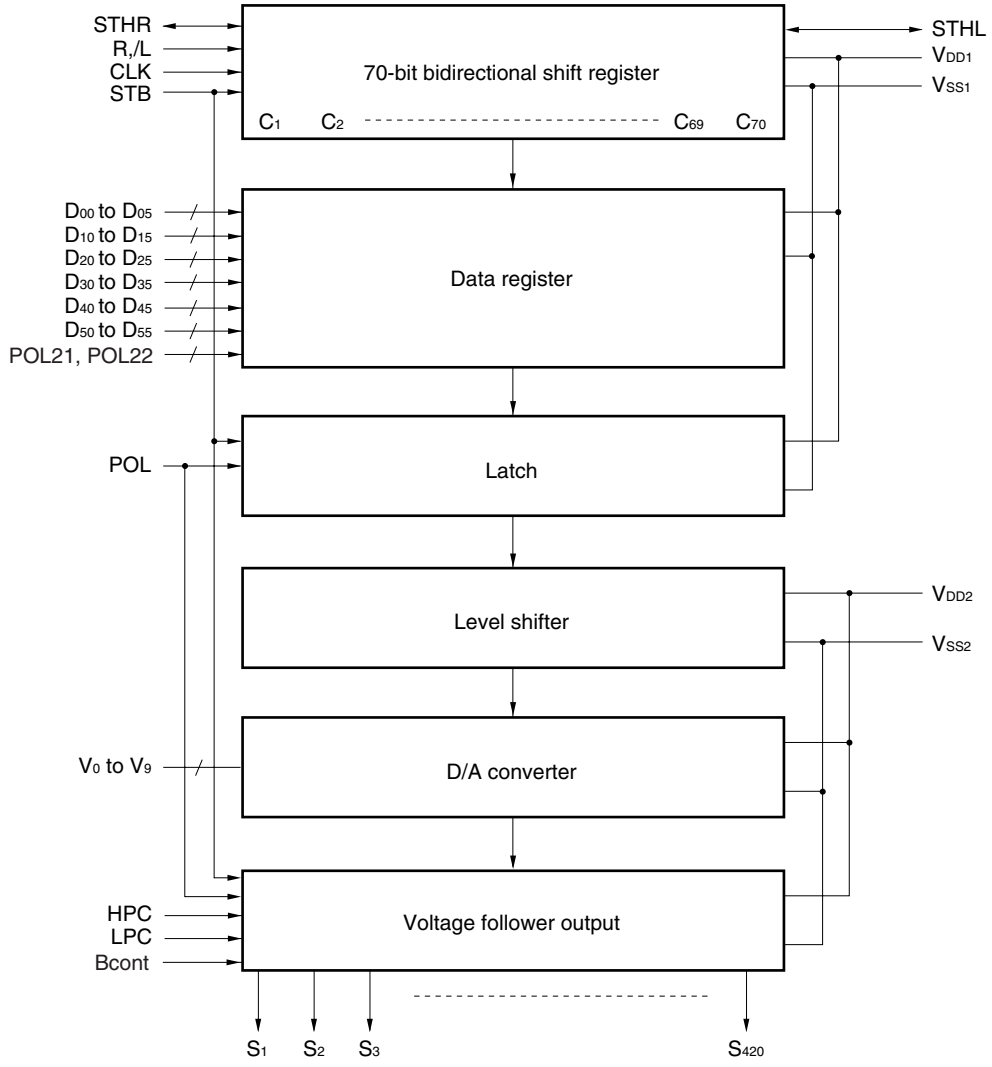
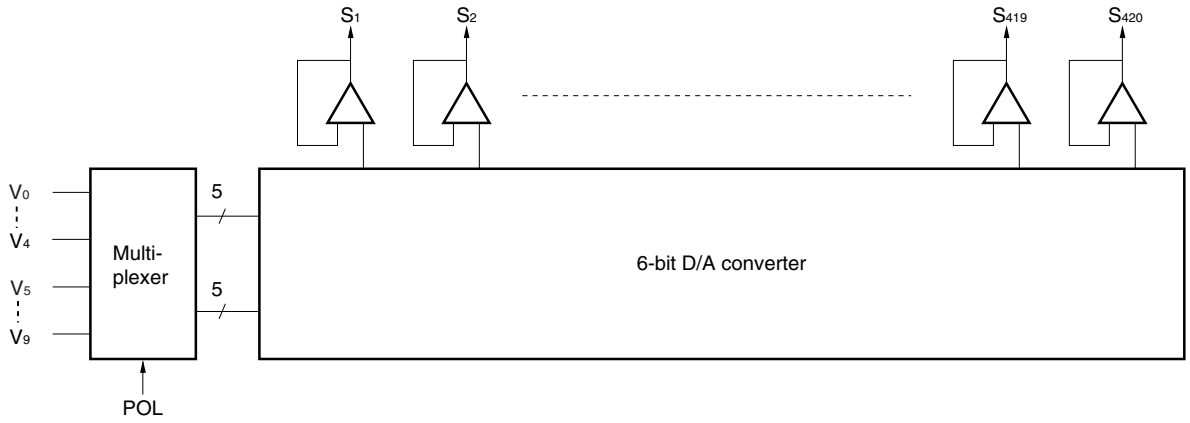
1. BLOCK DIAGRAM

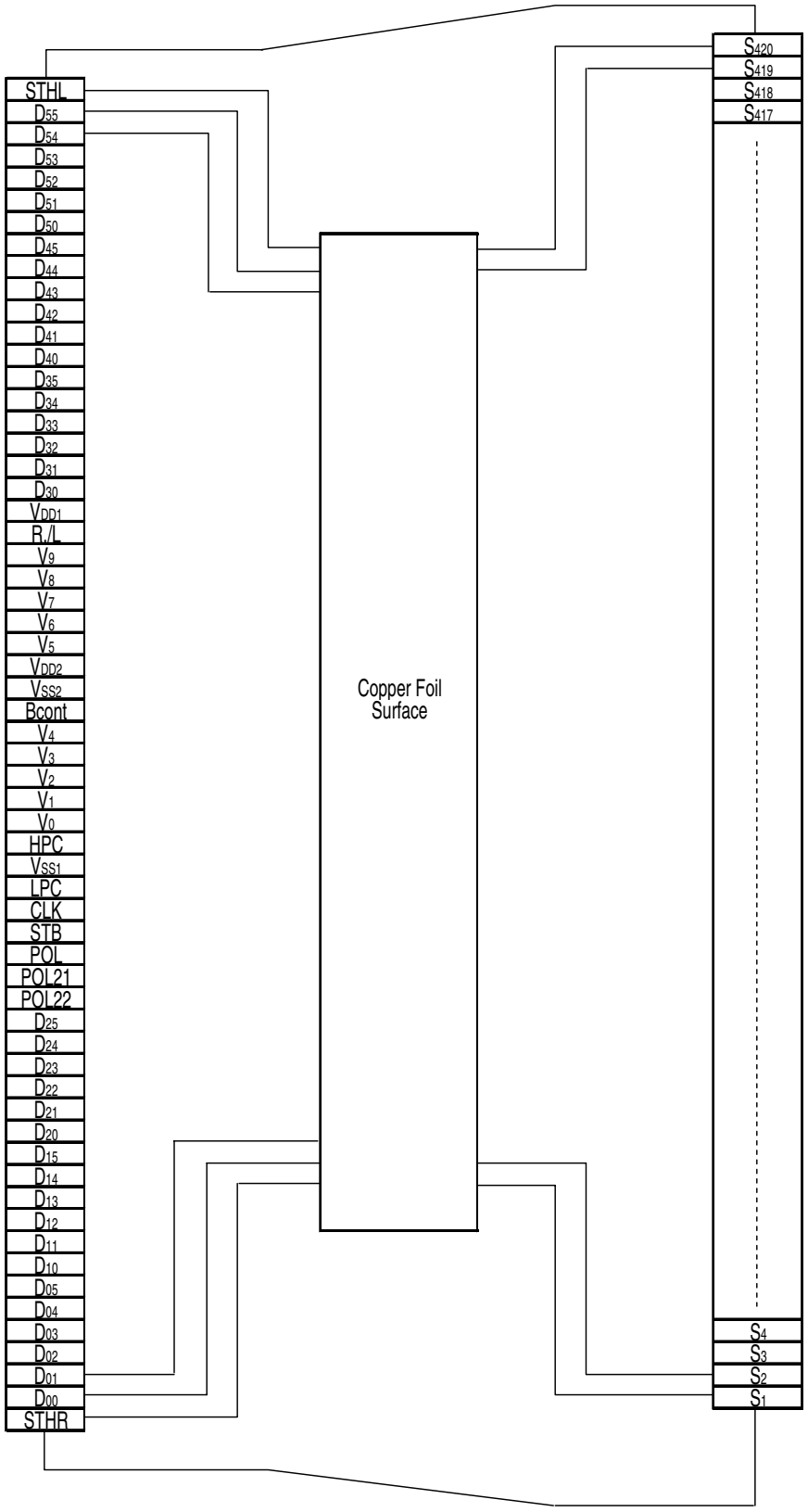


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD160062N-xxx: TCP) (Copper Foil Surface, Face-up)



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S_1 to S_{420}	Driver	Output	The D/A converted 64-gray-scale analog voltage is output.
D_{00} to D_{05} D_{10} to D_{15} D_{20} to D_{25} D_{30} to D_{35} D_{40} to D_{45} D_{50} to D_{55}	Display data	Input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X5}: MSB
R,/L	Shift direction control	Input	The shift direction control pin of shift register. The shift directions of the shift registers are as follows. R,/L = H (right shift) : STHR input, $S_1 \rightarrow S_{420}$, STHL output R,/L = L (left shift) : STHL input, $S_{420} \rightarrow S_1$, STHR output
STHR	Right shift start pulse	I/O	These refer to the start pulse I/O pins when driver ICs are connected in cascade. Fetching of display data starts when H is read at the rising edge of CLK. R,/L = H (right shift) : STHR input, STHL output R,/L = L (left shift) : STHL input, STHR output A H level should be input as the pulse of one cycle of the clock signal. If the start pulse input is more than 2 CLK, the first 1 CLK of the H level input is valid.
STHL	Left shift start pulse	I/O	
CLK	Shift clock	Input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 70th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. If 72 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch	Input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	Input	POL = L: The S_{2n-1} output uses V_0 to V_4 as the reference supply. The S_{2n} output uses V_5 to V_9 as the reference supply. POL = H: The S_{2n-1} output uses V_5 to V_9 as the reference supply. The S_{2n} output uses V_0 to V_4 as the reference supply. S_{2n-1} indicates the odd output and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL-STB}$) with respect to STB's rising edge.
POL21, POL22	Data inversion	Input	Data inversion can invert when display data is loaded. POL21: Invert/not invert of display data D_{00} to D_{05}, D_{10} to D_{15}, D_{20} to D_{25} POL22: Invert/not invert of display data D_{30} to D_{35}, D_{40} to D_{45}, D_{50} to D_{55} POL21, POL22 = H: Data inversion loads display data after inverting it. POL21, POL22 = L: Data inversion does not invert input data.
LPC	Low power control	Input	Controls the write function of the driver section by digitally controlling the bypass current of the output amplifier. Refer to **9. CURRENT CONSUMPTION CONTROL FUNCTION** for details. This pin is pulled up to the V_{DD1} power supply inside the IC.
HPC	High power control	Input	
Bcont	Bias control	Input	This pin can be used to finely control the bias current inside the output amplifier. Refer to **9. CURRENT CONSUMPTION CONTROL FUNCTION** for details. When this fine-control function is not required, leave this pin open.

(2/2)

Pin Symbol	Pin Name	I/O	Description
V_0 to V_9	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.1\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5\ V_{DD2}$ $0.5\ V_{DD2} \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1\ V$
V_{DD1}	Logic power supply	–	2.3 to 3.6 V
V_{DD2}	Driver power supply	–	8.0 to 9.0 V
V_{SS1}	Logic ground	–	Grounding
V_{SS2}	Driver ground	–	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down.

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also recommended between the γ-corrected power supply terminals (V_0, V_1, V_2, ···, V_9) and V_{SS2}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The μPD160062 incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel γ-compensated voltages to V_0' to V_{63}' and V_0" to V_{63}" is almost equivalent. For the 2 sets of five γ-compensated power supplies, V_0 to V_4 and V_5 to V_9, respectively, input gray scale voltages of the same polarity with respect to the common voltage. When fine gray scale voltage precision is not necessary, there is no need to connect a voltage follower circuit to the γ-compensated power supplies V_1 to V_3 and V_6 to V_8.

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of

$V_{DD2} - 0.1\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5\ V_{DD2}$

$0.5\ V_{DD2} \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1\ V$

Figures 5–2 shows γ-corrected power supply voltage and ladder resistors ratio and figure 5–3 shows the relationship between the input data and the output voltage.

Figure 5–1. Relationship between Input Data and γ-corrected Power Supplies

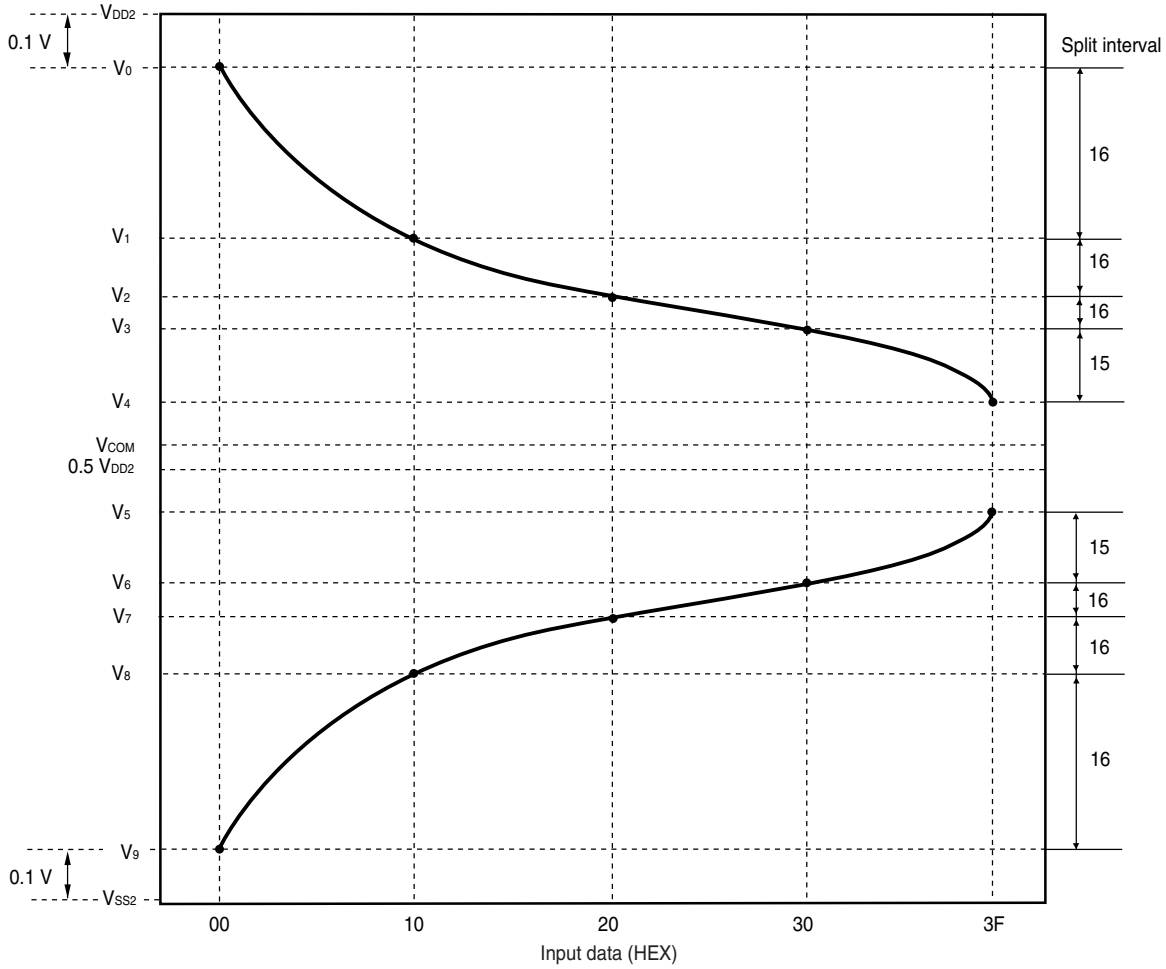
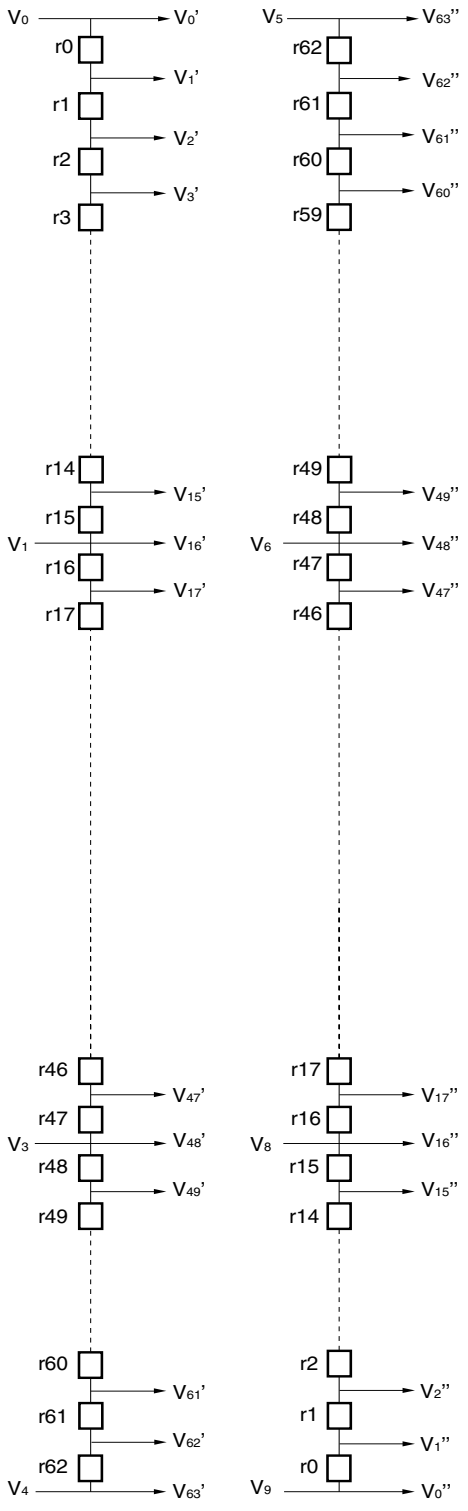


Figure 5–2. γ-corrected Voltages and Ladder Resistors Ratio



rn	Ratio 1	Ratio 2	Value (Ω)
r0	8.00	0.0505	544
r1	7.50	0.0473	510
r2	7.00	0.0442	476
r3	6.50	0.0410	442
r4	6.00	0.0379	408
r5	5.50	0.0347	374
r6	5.50	0.0347	374
r7	5.00	0.0315	340
r8	5.00	0.0315	340
r9	4.00	0.0252	272
r10	4.00	0.0252	272
r11	3.50	0.0221	238
r12	3.50	0.0221	238
r13	3.50	0.0221	238
r14	3.00	0.0189	204
r15	3.00	0.0189	204
r16	3.00	0.0189	204
r17	2.50	0.0158	170
r18	2.50	0.0158	170
r19	2.50	0.0158	170
r20	2.00	0.0126	136
r21	2.00	0.0126	136
r22	2.00	0.0126	136
r23	1.50	0.0095	102
r24	1.50	0.0095	102
r25	1.50	0.0095	102
r26	1.50	0.0095	102
r27	1.00	0.0063	68
r28	1.00	0.0063	68
r29	1.00	0.0063	68
r30	1.00	0.0063	68
r31	1.00	0.0063	68
r32	1.00	0.0063	68
r33	1.00	0.0063	68
r34	1.00	0.0063	68
r35	1.00	0.0063	68
r36	1.00	0.0063	68
r37	1.00	0.0063	68
r38	1.00	0.0063	68
r39	1.00	0.0063	68
r40	1.00	0.0063	68
r41	1.00	0.0063	68
r42	1.00	0.0063	68
r43	1.00	0.0063	68
r44	1.00	0.0063	68
r45	1.00	0.0063	68
r46	1.00	0.0063	68
r47	1.00	0.0063	68
r48	1.00	0.0063	68
r49	1.00	0.0063	68
r50	1.00	0.0063	68
r51	1.00	0.0063	68
r52	1.00	0.0063	68
r53	1.50	0.0095	102
r54	1.50	0.0095	102
r55	1.50	0.0095	102
r56	2.00	0.0126	136
r57	2.00	0.0126	136
r58	2.50	0.0158	170
r59	2.50	0.0158	170
r60	3.00	0.0189	204
r61	5.00	0.0315	340
r62	8.00	0.0505	544
Total resistance			10778
Minimum resistance value			68

Remark The resistance ratio1 is a relative ratio in the case of setting the minimum resistance value to 1.
The resistance ratio2 is a relative ratio in the case of setting the total resistance to 1.

Caution There is no connection between V_4 and V_5 terminal in the chip.

Figure 5–3. Relationship between Input Data and Output Voltage (POL21, POL22 = L)

(Output Voltage 1) V_{DD2} –0.1 V ≥ V_0 > V_1 > V_2 > V_3 > V_4 ≥ 0.5 V_{DD2}

(Output Voltage 2) 0.5 V_{DD2} ≥ V_5 > V_6 > V_7 > V_8 > V_9 ≥ V_{SS2} +0.1 V

Input Data	Output Voltage 1		Output Voltage 2	
00H	$V_{0'}$	V_0	$V_{0''}$	V_9
01H	$V_{1'}$	$V_1+(V_0-V_1)\times 4930/5474$	$V_{1''}$	$V_9+(V_8-V_9)\times 544/5474$
02H	$V_{2'}$	$V_1+(V_0-V_1)\times 4420/5474$	$V_{2''}$	$V_9+(V_8-V_9)\times 1054/5474$
03H	$V_{3'}$	$V_1+(V_0-V_1)\times 3944/5474$	$V_{3''}$	$V_9+(V_8-V_9)\times 1530/5474$
04H	$V_{4'}$	$V_1+(V_0-V_1)\times 3502/5474$	$V_{4''}$	$V_9+(V_8-V_9)\times 1972/5474$
05H	$V_{5'}$	$V_1+(V_0-V_1)\times 3094/5474$	$V_{5''}$	$V_9+(V_8-V_9)\times 2380/5474$
06H	$V_{6'}$	$V_1+(V_0-V_1)\times 2720/5474$	$V_{6''}$	$V_9+(V_8-V_9)\times 2754/5474$
07H	$V_{7'}$	$V_1+(V_0-V_1)\times 2346/5474$	$V_{7''}$	$V_9+(V_8-V_9)\times 3128/5474$
08H	$V_{8'}$	$V_1+(V_0-V_1)\times 2006/5474$	$V_{8''}$	$V_9+(V_8-V_9)\times 3468/5474$
09H	$V_{9'}$	$V_1+(V_0-V_1)\times 1666/5474$	$V_{9''}$	$V_9+(V_8-V_9)\times 3808/5474$
0AH	$V_{10'}$	$V_1+(V_0-V_1)\times 1394/5474$	$V_{10''}$	$V_9+(V_8-V_9)\times 4080/5474$
0BH	$V_{11'}$	$V_1+(V_0-V_1)\times 1122/5474$	$V_{11''}$	$V_9+(V_8-V_9)\times 4352/5474$
0CH	$V_{12'}$	$V_1+(V_0-V_1)\times 884/5474$	$V_{12''}$	$V_9+(V_8-V_9)\times 4590/5474$
0DH	$V_{13'}$	$V_1+(V_0-V_1)\times 646/5474$	$V_{13''}$	$V_9+(V_8-V_9)\times 4828/5474$
0EH	$V_{14'}$	$V_1+(V_0-V_1)\times 408/5474$	$V_{14''}$	$V_9+(V_8-V_9)\times 5066/5474$
0FH	$V_{15'}$	$V_1+(V_0-V_1)\times 204/5474$	$V_{15''}$	$V_9+(V_8-V_9)\times 5270/5474$
10H	$V_{16'}$	V_1	$V_{16''}$	V_8
11H	$V_{17'}$	$V_2+(V_1-V_2)\times 1666/1870$	$V_{17''}$	$V_8+(V_7-V_8)\times 204/1870$
12H	$V_{18'}$	$V_2+(V_1-V_2)\times 1496/1870$	$V_{18''}$	$V_8+(V_7-V_8)\times 374/1870$
13H	$V_{19'}$	$V_2+(V_1-V_2)\times 1326/1870$	$V_{19''}$	$V_8+(V_7-V_8)\times 544/1870$
14H	$V_{20'}$	$V_2+(V_1-V_2)\times 1156/1870$	$V_{20''}$	$V_8+(V_7-V_8)\times 714/1870$
15H	$V_{21'}$	$V_2+(V_1-V_2)\times 1020/1870$	$V_{21''}$	$V_8+(V_7-V_8)\times 850/1870$
16H	$V_{22'}$	$V_2+(V_1-V_2)\times 884/1870$	$V_{22''}$	$V_8+(V_7-V_8)\times 986/1870$
17H	$V_{23'}$	$V_2+(V_1-V_2)\times 748/1870$	$V_{23''}$	$V_8+(V_7-V_8)\times 1122/1870$
18H	$V_{24'}$	$V_2+(V_1-V_2)\times 646/1870$	$V_{24''}$	$V_8+(V_7-V_8)\times 1224/1870$
19H	$V_{25'}$	$V_2+(V_1-V_2)\times 544/1870$	$V_{25''}$	$V_8+(V_7-V_8)\times 1326/1870$
1AH	$V_{26'}$	$V_2+(V_1-V_2)\times 442/1870$	$V_{26''}$	$V_8+(V_7-V_8)\times 1428/1870$
1BH	$V_{27'}$	$V_2+(V_1-V_2)\times 340/1870$	$V_{27''}$	$V_8+(V_7-V_8)\times 1530/1870$
1CH	$V_{28'}$	$V_2+(V_1-V_2)\times 272/1870$	$V_{28''}$	$V_8+(V_7-V_8)\times 1598/1870$
1DH	$V_{29'}$	$V_2+(V_1-V_2)\times 204/1870$	$V_{29''}$	$V_8+(V_7-V_8)\times 1666/1870$
1EH	$V_{30'}$	$V_2+(V_1-V_2)\times 136/1870$	$V_{30''}$	$V_8+(V_7-V_8)\times 1734/1870$
1FH	$V_{31'}$	$V_2+(V_1-V_2)\times 68/1870$	$V_{31''}$	$V_8+(V_7-V_8)\times 1802/1870$
20H	$V_{32'}$	V_2	$V_{32''}$	V_7
21H	$V_{33'}$	$V_3+(V_2-V_3)\times 1020/1088$	$V_{33''}$	$V_7+(V_6-V_7)\times 68/1088$
22H	$V_{34'}$	$V_3+(V_2-V_3)\times 952/1088$	$V_{34''}$	$V_7+(V_6-V_7)\times 136/1088$
23H	$V_{35'}$	$V_3+(V_2-V_3)\times 884/1088$	$V_{35''}$	$V_7+(V_6-V_7)\times 204/1088$
24H	$V_{36'}$	$V_3+(V_2-V_3)\times 816/1088$	$V_{36''}$	$V_7+(V_6-V_7)\times 272/1088$
25H	$V_{37'}$	$V_3+(V_2-V_3)\times 748/1088$	$V_{37''}$	$V_7+(V_6-V_7)\times 340/1088$
26H	$V_{38'}$	$V_3+(V_2-V_3)\times 680/1088$	$V_{38''}$	$V_7+(V_6-V_7)\times 408/1088$
27H	$V_{39'}$	$V_3+(V_2-V_3)\times 612/1088$	$V_{39''}$	$V_7+(V_6-V_7)\times 476/1088$
28H	$V_{40'}$	$V_3+(V_2-V_3)\times 544/1088$	$V_{40''}$	$V_7+(V_6-V_7)\times 544/1088$
29H	$V_{41'}$	$V_3+(V_2-V_3)\times 476/1088$	$V_{41''}$	$V_7+(V_6-V_7)\times 612/1088$
2AH	$V_{42'}$	$V_3+(V_2-V_3)\times 408/1088$	$V_{42''}$	$V_7+(V_6-V_7)\times 680/1088$
2BH	$V_{43'}$	$V_3+(V_2-V_3)\times 340/1088$	$V_{43''}$	$V_7+(V_6-V_7)\times 748/1088$
2CH	$V_{44'}$	$V_3+(V_2-V_3)\times 272/1088$	$V_{44''}$	$V_7+(V_6-V_7)\times 816/1088$
2DH	$V_{45'}$	$V_3+(V_2-V_3)\times 204/1088$	$V_{45''}$	$V_7+(V_6-V_7)\times 884/1088$
2EH	$V_{46'}$	$V_3+(V_2-V_3)\times 136/1088$	$V_{46''}$	$V_7+(V_6-V_7)\times 952/1088$
2FH	$V_{47'}$	$V_3+(V_2-V_3)\times 68/1088$	$V_{47''}$	$V_7+(V_6-V_7)\times 1020/1088$
30H	$V_{48'}$	V_3	$V_{48''}$	V_6
31H	$V_{49'}$	$V_4+(V_3-V_4)\times 2278/2346$	$V_{49''}$	$V_6+(V_5-V_6)\times 68/2346$
32H	$V_{50'}$	$V_4+(V_3-V_4)\times 2210/2346$	$V_{50''}$	$V_6+(V_5-V_6)\times 136/2346$
33H	$V_{51'}$	$V_4+(V_3-V_4)\times 2142/2346$	$V_{51''}$	$V_6+(V_5-V_6)\times 204/2346$
34H	$V_{52'}$	$V_4+(V_3-V_4)\times 2074/2346$	$V_{52''}$	$V_6+(V_5-V_6)\times 272/2346$
35H	$V_{53'}$	$V_4+(V_3-V_4)\times 2006/2346$	$V_{53''}$	$V_6+(V_5-V_6)\times 340/2346$
36H	$V_{54'}$	$V_4+(V_3-V_4)\times 1904/2346$	$V_{54''}$	$V_6+(V_5-V_6)\times 442/2346$
37H	$V_{55'}$	$V_4+(V_3-V_4)\times 1802/2346$	$V_{55''}$	$V_6+(V_5-V_6)\times 544/2346$
38H	$V_{56'}$	$V_4+(V_3-V_4)\times 1700/2346$	$V_{56''}$	$V_6+(V_5-V_6)\times 646/2346$
39H	$V_{57'}$	$V_4+(V_3-V_4)\times 1564/2346$	$V_{57''}$	$V_6+(V_5-V_6)\times 782/2346$
3AH	$V_{58'}$	$V_4+(V_3-V_4)\times 1428/2346$	$V_{58''}$	$V_6+(V_5-V_6)\times 918/2346$
3BH	$V_{59'}$	$V_4+(V_3-V_4)\times 1258/2346$	$V_{59''}$	$V_6+(V_5-V_6)\times 1088/2346$
3CH	$V_{60'}$	$V_4+(V_3-V_4)\times 1088/2346$	$V_{60''}$	$V_6+(V_5-V_6)\times 1258/2346$
3DH	$V_{61'}$	$V_4+(V_3-V_4)\times 884/2346$	$V_{61''}$	$V_6+(V_5-V_6)\times 1462/2346$
3EH	$V_{62'}$	$V_4+(V_3-V_4)\times 544/2346$	$V_{62''}$	$V_6+(V_5-V_6)\times 1802/2346$
3FH	$V_{63'}$	V_4	$V_{63''}$	V_5

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits × 2 RGBs (6 dots)

Input width: 36 bits (2-pixel data)

(1) R,/L = H (right shift)

Output	S_1	S_2	S_3	S_4	···	S_{419}	S_{420}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

(2) R,/L = L (left shift)

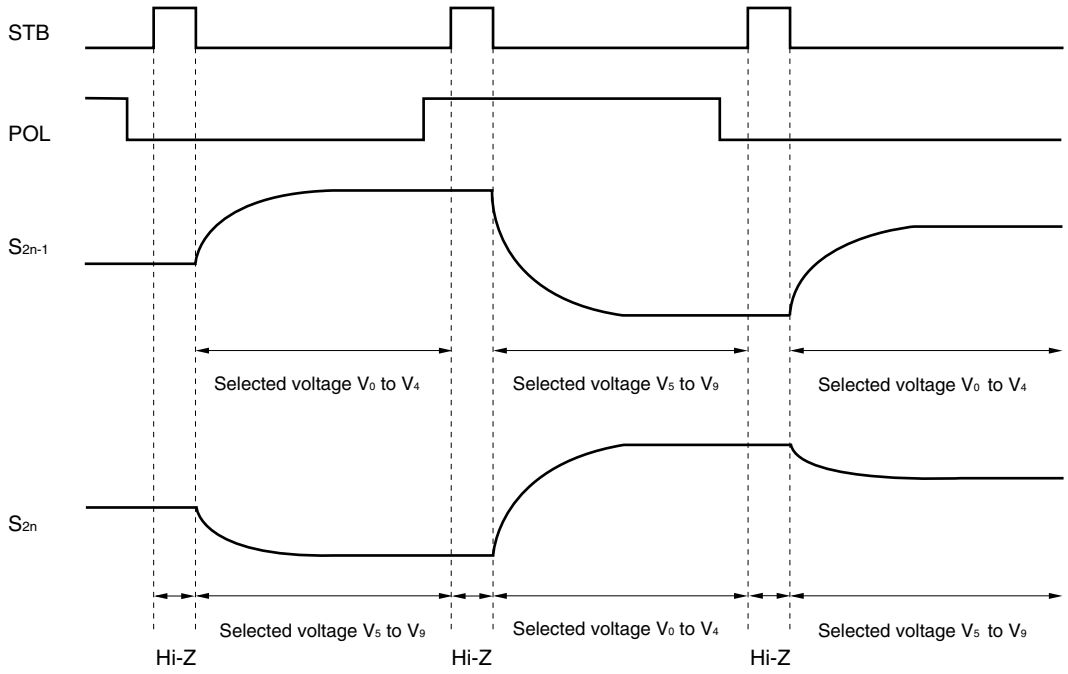
Output	S_1	S_2	S_3	S_4	···	S_{419}	S_{420}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

POL	S_{2n-1} Note	S_{2n} Note
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

Note S_{2n-1} (odd output), S_{2n} (even output)

7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



Remark Hi-Z: High impedance

8. RELATIONSHIP BETWEEN STB, CLK AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

Figure 8–1. Output Circuit Block Diagram

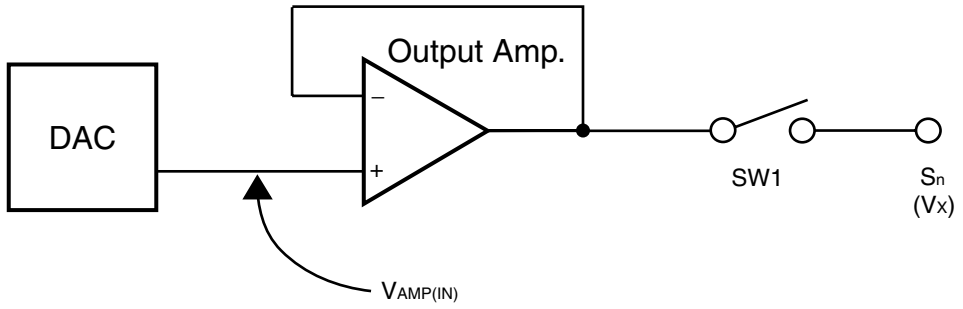
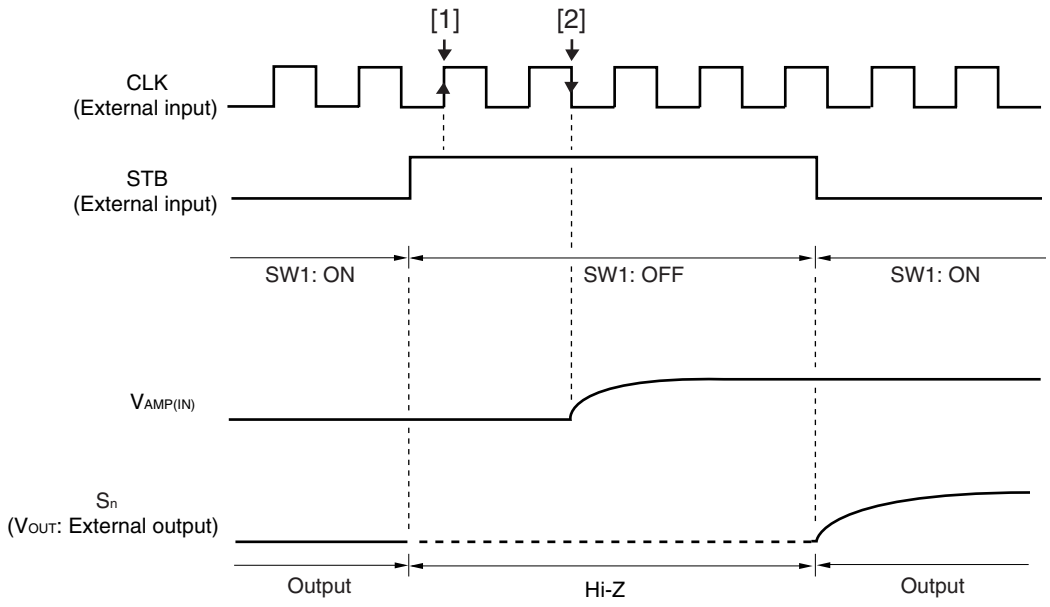


Figure 8–2. Output Circuit Timing Waveform



Remarks 1. STB = L: SW1 = ON, STB = H: SW1 = OFF

2. STB = H is acknowledged at timing [1] .

3. The display data latch is completed at timing [2] and the input voltage ($V_{AMP(IN)}$: gray-scale level voltage) of the output amplifier changes.

9. CURRENT CONSUMPTION CONTROL FUNCTION

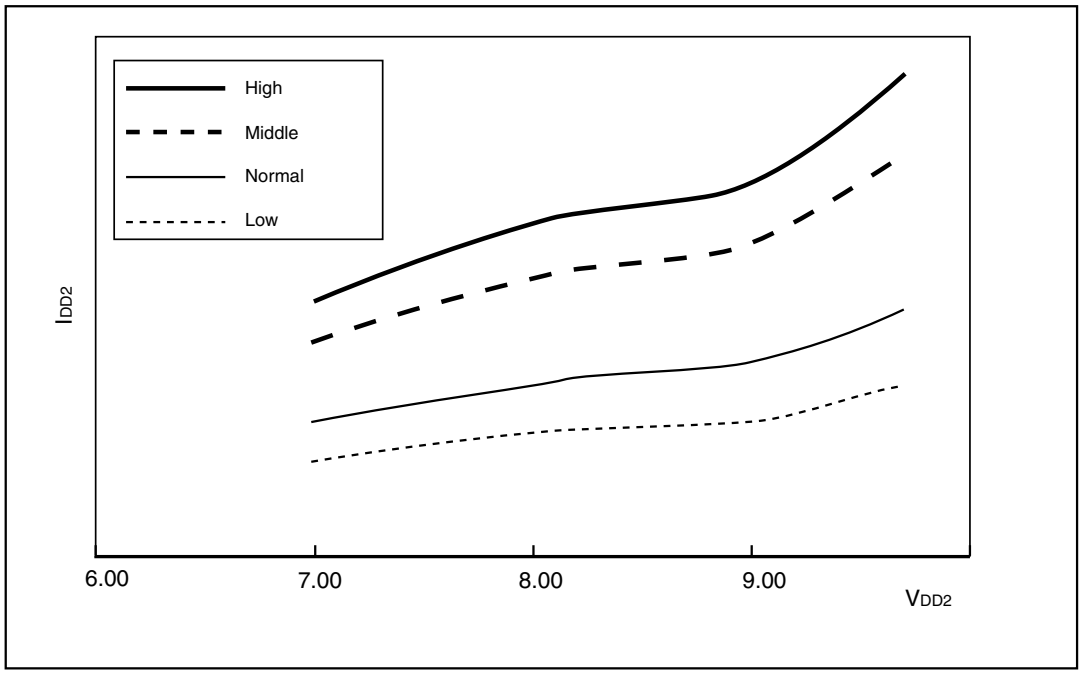
The μPD160062 has a power control function which can switch the bias current of the output amplifier between four levels and a bias control function (Bcont) which can be used to finely control the bias current.

< Power control function (LPC, HPC) >

The bias current of the output amplifier can be switched between four levels using LPC (Low Power Control) pins and HPC (High Power Control) pins (show in below table).

Power Mode	LPC	HPC
High	L	L
Middle	H or open	L
Normal	L	H or open
Low	H or open	H or open

Following graph shows the relationship between each power modes and bias current.

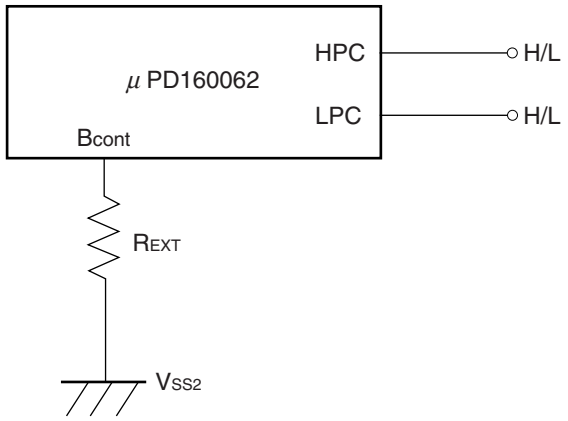


Remark This relationship is founded on results of simulation and don't assuring a characteristics of this product.

< Bias Current Control Function (Bcont) >

It is possible to fine-control the current consumption by using the bias current control function (Bcont pin). When using this function, connect this pin to the stabilized ground potential (V_{SS2}) via an external resistor (R_{EXT}). When not using this function, leave this pin open.

Figure 9–1. Bias Current Control Function (Bcont)



Refer to the table below for the percentage of current regulation when using the bias current control function.

Table 9–1. Current Consumption Regulation Percentage Compared to Normal Mode (V_{DD1} = 3.3 V, V_{DD2} = 8.7 V)

R_{EXT} (kΩ)	Current Consumption Regulation Percentage (%)	
	LPC = L	LPC = H/open
∞ (Open)	100	65
50	110	70
20	115	80
10	120	85

Remark The above current consumption regulation percentages are founded on results of simulation and don't assuring a characteristics of this product.

Caution Because the power and bias-current control functions control the bias current in the output amplifier and regulate the over-all current consumption of the driver IC, when this occurs, the characteristics of the output amplifier will simultaneously change. Therefore, when using these functions, be sure to sufficiently evaluate the picture quality.

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +4.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +10.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} +0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} +0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} +0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} +0.5	V
Operating Ambient Temperature	T_A	–10 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution Product qualify may suffer if the absolute maximum rating is exceeded even momentarily for any parameter/ That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		2.3		3.6	V
Driver Part Supply Voltage	V_{DD2}		8.0	8.5	9.0	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V
γ-corrected Voltage	V_0 to V_4		0.5 V_{DD2}		V_{DD2} –0.1	V
	V_5 to V_9		V_{SS2} +0.1		0.5 V_{DD2}	V
Driver Part Output Voltage	V_O		V_{SS2} +0.1		V_{DD2} –0.1	V
Maximum Clock Frequency	f_{CLK}	V_{DD1} = 2.3 V			45	MHz

Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 8.0 to 9.0 V, V_{SS1} = V_{SS2} = 0 V, unless otherwise specified, power mode = normal, Bcont = open.)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{IL}				±1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA	V_{DD1} –0.1			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA			0.1	V
γ-corrected Resistance	R_γ	V_{DD2} = 8.5 V, V_0 to V_4 = V_5 to V_9 = 4.0 V	5.4	10.8	21.6	kΩ
Driver Output Current	I_{VOH}	V_X = 7.0 V, V_{OUT} = 6.5 V Note			–30	μA
	I_{VOL}	V_X = 1.0 V, V_{OUT} = 1.5 V Note	30			μA
Output Voltage Deviation	ΔV_O	T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 8.5 V, V_{OUT} = 2.0 V, 4.25 V, 6.5 V		±7	±20	mV
Output swing difference deviation	ΔV_{P-P}			±2	±15	mV
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1}		1.0	6.5	mA
Driver Part Dynamic Current Consumption	I_{DD2}	V_{DD2}, with no load		3.0	6.5	mA

Note V_X refers to the output voltage of analog output pins S_1 to S_{420}. V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{420}.

Cautions 1. f_{STB} = 64 kHz, f_{CLK} = 40 MHz

2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

3. Refers to the current consumption per driver when cascades are connected under the assumption of SXGA+ single-sided mounting (10 units).

Switching Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 8.0 to 9.0 V, V_{SS1} = V_{SS2} = 0 V, unless otherwise specified, power mode = normal, Bcont = open.)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 10 pF		10	20	ns
Driver Output Delay Time	t_{PLH2}	C_L = 75 pF, R_L = 5 kΩ		2.5	5	μs
	t_{PLH3}			5	8	μs
	t_{PHL2}			2.5	5	μs
	t_{PHL3}			5	8	μs
Input Capacitance	C_{I1}	STHR (STHL) excluded, T_A = 25°C			10	pF
	C_{I2}	STHR (STHL), T_A = 25°C			10	pF

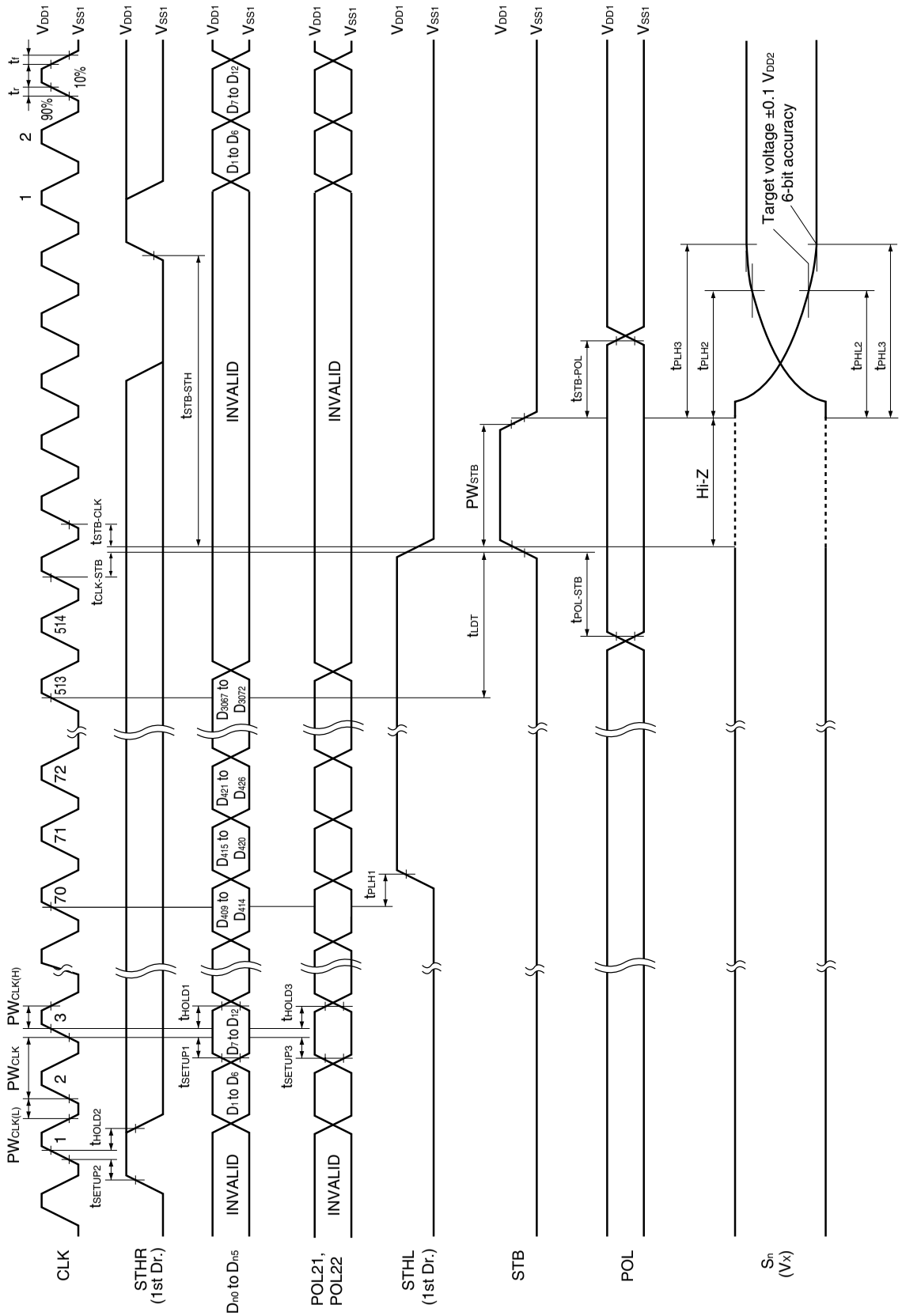
Timing Requirement (T_A = –10 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{SS1} = 0 V, $t_r = t_f$ = 5.0 ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		22			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		4			ns
Data Setup Time	t_{SETUP1}		4			ns
Data Hold Time	t_{HOLD1}		0			ns
Start Pulse Setup Time	t_{SETUP2}		4			ns
Start Pulse Hold Time	t_{HOLD2}		0			ns
POL21, POL22 Setup Time	t_{SETUP3}		4			ns
POL21, POL22 Hold Time	t_{HOLD3}		0			ns
STB Pulse Width	PW_{STB}		2			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↑	6			ns
STB-CLK Time	$t_{STB-CLK}$	STB ↑ → CLK ↑	9			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↑ → STHR(STHL) ↑	2			CLK
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	–5			ns
STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↓ or ↑	6			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

Switching characteristics waveform (R/L = H)

Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



11. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for soldering conditions of the μPD160062.

For more details, refer to the **Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html).**

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

μPD160062N-×××: TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds, pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C, pressure 3 to 8 kg/cm^2, time 3 to 5 seconds. Real bonding 165 to 180°C, pressure 25 to 45 kg/cm^2, time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.