SPI-Bus: Improving Noise Immunity

Prepared by: Fred Zlotnick ON Semiconductor



http://onsemi.com

TECHNICAL NOTE

should be remembered that the '14' in logic series, provides a Schmitt input, but also inverts the signal, so the software needs to take that into account.

When it comes to communicating over a serial bus, there are three main methods, SPI, Microwire and I^2C . The choice is not always easy to make, and often the designer must use whichever hardware is available on his microcontroller or peripherals. Art Eck¹ claims that of the three common interfaces, SPI is easiest to write code for, and is the fastest protocol. Some of the drawbacks to the SPI interface are the use of edge triggering and that the SPI bus is more susceptible to high levels of noise.

Often, the noise in the system is not under the direct control of the designer. Eck suggests the use of Schmitt triggers to help with the sensitivity of the system to noise. The problem for many system designers, is that previously, a set of Schmitt devices consisted of 6 triggers in a 14-pin package. Even a package like a the TSSOP-14 occupied a great deal of space. Often just one or two gates placed in the proper spot on a circuit board could correct many potential problems and speed up the system. ON Semiconductor is now offering a dual Schmitt device in an SC-70/SC-88A package that occupies only 4.5 mm² of board space and costs approximately \$0.20 each, in volumes of 10,000 or more. The NL27WZ14DFT2 is a dual Schmitt Inverter, manufactured in 0.6 µm CMOS technology that can improve noise immunity of any system. The device can be placed right near the serial device and provide noise immunity by its hysteresis on both data and clock lines. It

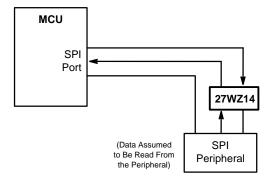


Figure 1. NL27WZ14 Replaces Larger Schmitt Trigger

In the event that a DSP or MCU is operating at a voltage level different from the peripheral, the gates offer the additional feature of being OVT (over-voltage-tolerant) and can interface any combination from 1.8 V to 5.0 V with no additional hardware. In Figure 1, the SPI peripheral is assumed MISO (Master In, Slave Out), with the MCU being the master. Data is going from the peripheral to the MCU, while the clock is directed from the MCU to the SPI device.

1- Art Eck, Serial Interface for Embedded Design, Circuit Cellar Online - Jan., 2000

<u>Notes</u>

ON Semiconductor and without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of thers. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada

Finone: 303–675–2175 of 800–344–3860 Toll Free USA/Canada Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center 4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031 Phone: 81–3–5740–2700 Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.