Product Preview

2-Input AND Gate

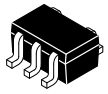
MC74HC1G08

The MC74HC1G08 is a high speed CMOS 2–input AND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent LSTTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74HC1G08 output drive current is 1/2 compared to MC74HC series.

- High Speed: t_{PD} = 7ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 1μA (Max) at T_A = 25°C
- High Noise Immunity
- Balanced Propagation Delays (tpLH = tpHL)
- Output Drive Capability: 5 LSTTL
- Symmetrical Output Impedance (I_{OH} = I_{OL} = 2mA)
- ESD Performance: HBM > 2000V; MM > 200V



DF SUFFIX
5–LEAD SOT–353 PACKAGE
SC–88A
CASE 419A–01

PROPOSED DT SUFFIX
5–LEAD TSSOP PACKAGE
TSOP5
CASE TBD

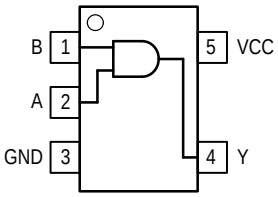


Figure 1. Pinout (Top View)

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

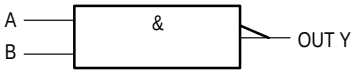
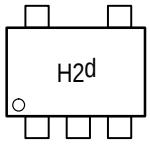


Figure 2. Logic Symbol



Pin 1
d = Date Code

Marking Diagram

DEVICE ORDERING INFORMATION

	Device Nomenclature							
Device Order Number	**Motorola Circuit Indicator**	**Temp Range Identifier**	**Technology**	**Device Function**	**Package Suffix**	**Tape and Reel Suffix**	**Package Type**	**Tape and Reel Size**
MC74HC1G08DFT1	MC	74	HC1G	08	DF	T1	SC–88A	7–Inch/3000 Unit
MC74HC1G08DTT1	MC	74	HC1G	08	DT	T1	TSOP5	7–Inch/3000 Unit

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS*

Characteristics		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +7.0	V
DC Input Voltage		V_{IN}	–0.5 to V_{CC} + 0.5	V
DC Output Voltage		V_{OUT}	–0.5 to V_{CC} + 0.5	V
Input Diode Current		I_{IK}	±20	mA
Output Diode Current	(V_{OUT} < GND; V_{OUT} > V_{CC})	I_{OK}	±20	mA
DC Output Current, per Pin		I_{OUT}	±12.5	mA
DC Supply Current, V_{CC} and GND		I_{CC}	±25	mA
Power dissipation in still air	SC–88A† TSOP5†	P_D	200 450	mW
Lead temperature, 1 mm from case for 10 s		T_L	260	°C
Storage temperature		T_{stg}	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C
— TSOP5 Package: –6 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	6.0	V
DC Input Voltage		V_{IN}	0.0	V_{CC}	V
DC Output Voltage		V_{OUT}	0.0	V_{CC}	V
Operating Temperature Range		T_A	–55	+125	°C
Input Rise and Fall Time	V_{CC} = 2.0V V_{CC} = 3.0V V_{CC} = 4.5V V_{CC} = 6.0V	t_r , t_f	0 0 0 0	1000 600 500 400	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.20			1.5 2.1 3.15 4.20		1.5 2.1 3.15 4.20		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 6.0			0.5 0.9 1.35 1.80		0.5 0.9 1.35 1.80		0.5 0.9 1.35 1.80	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -20\mu A$	2.0 3.0 4.5 6.0	1.9 2.9 4.4 5.9	2.0 3.0 4.5 6.0		1.9 2.9 4.4 5.9		1.9 2.9 4.4 5.9		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -2mA$ $I_{OH} = -2.6mA$	 4.5 6.0	 4.18 5.68	 4.31 5.80		 4.13 5.63		 4.08 5.58		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 20\mu A$	2.0 3.0 4.5 6.0		0.0 0.0 0.0 0.0	0.1 0.1 0.1 0.1		0.1 0.1 0.1 0.1		0.1 0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 2mA$ $I_{OL} = 2.6mA$	 4.5 6.0		 0.17 0.18	 0.26 0.26		 0.33 0.33		 0.40 0.40	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 6.0V or GND	0 to 6.0			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	6.0			1.0		10		40	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input $t_r = t_f$ = 6.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$T_A \le 125°C$ Min	$T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A or B to Y	V_{CC} = 5.0V	C_L = 15 pF		7.0	15		20		25	ns
		V_{CC} = 2.0V V_{CC} = 3.0V V_{CC} = 4.5V V_{CC} = 6.0V	C_L = 50 pF		48 24 12 9.0	100 40 20 17		125 50 25 21		155 90 35 26	
t_{TLH}, t_{THL}	Output Transition Time	V_{CC} = 5.0V	C_L = 15 pF		5.0	10		15		20	ns
		V_{CC} = 2.0V V_{CC} = 3.0V V_{CC} = 4.5V V_{CC} = 6.0V	C_L = 50 pF		50 22 14 12	125 35 25 21		155 45 31 26		200 60 38 32	
C_{IN}	Maximum Input Capacitance				5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	10	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

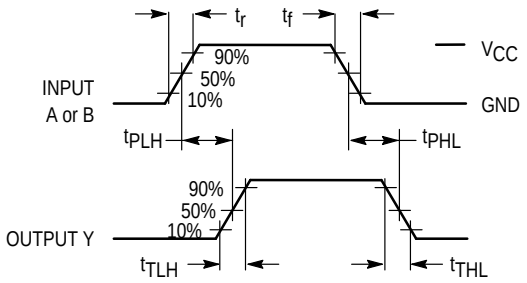
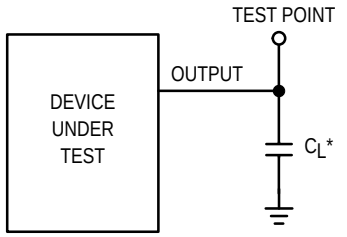


Figure 3. Switching Waveforms

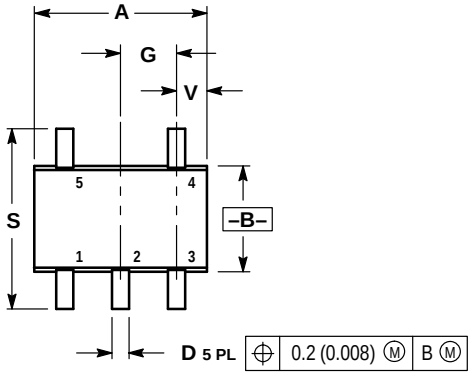


* Includes all probe and jig capacitance

Figure 4. Test Circuit

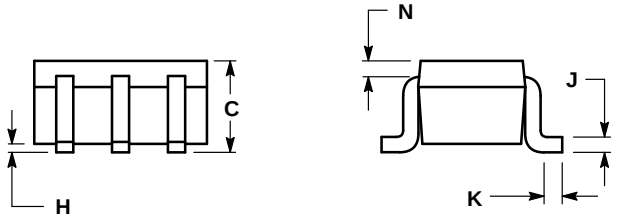
OUTLINE DIMENSIONS

DF SUFFIX
5–LEAD SOT–353 PACKAGE
SC–88A
CASE 419A–01
ISSUE B

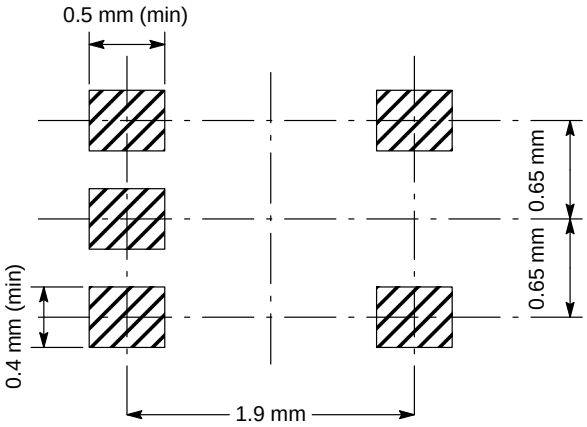


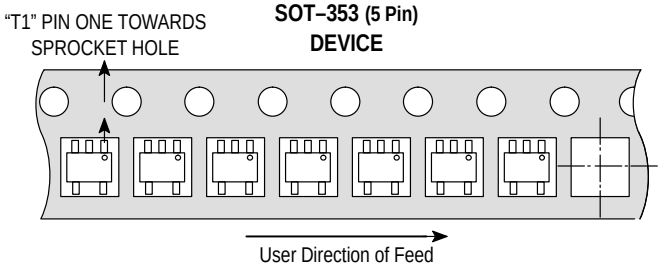
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	—	0.004	—	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

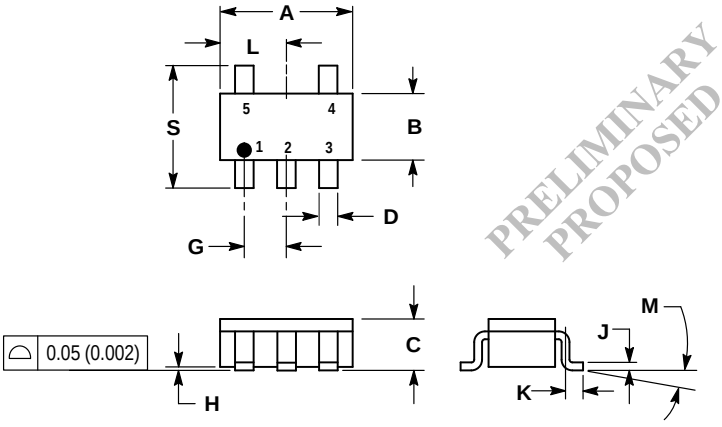


SOT–353





PROPOSED DT SUFFIX
5–LEAD TSSOP PACKAGE
TSOP5
CASE TBD
ISSUE TBD

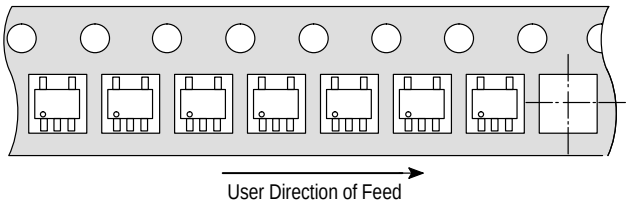


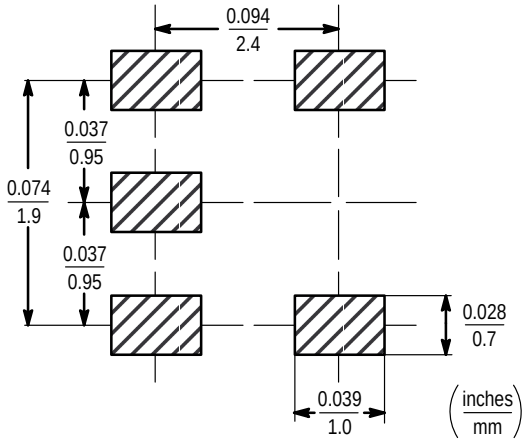
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181

DO NOT DESIGN WITH THESE DIMENSIONS – PRELIMINARY

TSOP5 (5 Pin)
DEVICE





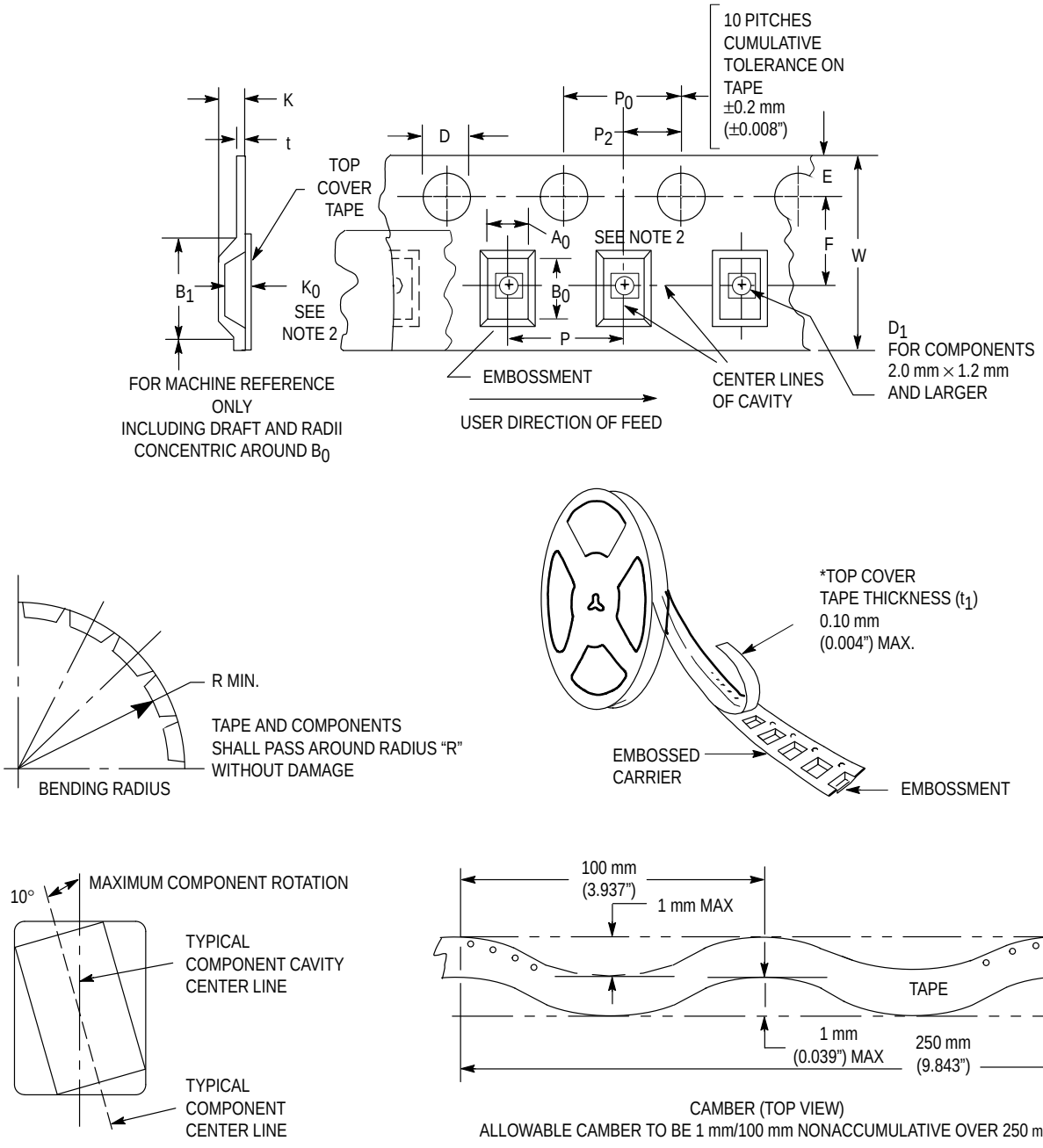


Figure 5. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.35 mm (0.171")	1.5 +0.1/ –0.0 mm (0.059 +0.004/ –0.0")	1.0 mm Min (0.039")	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/ –0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

1. Metric Dimensions Govern–English are in parentheses for reference only.
2. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

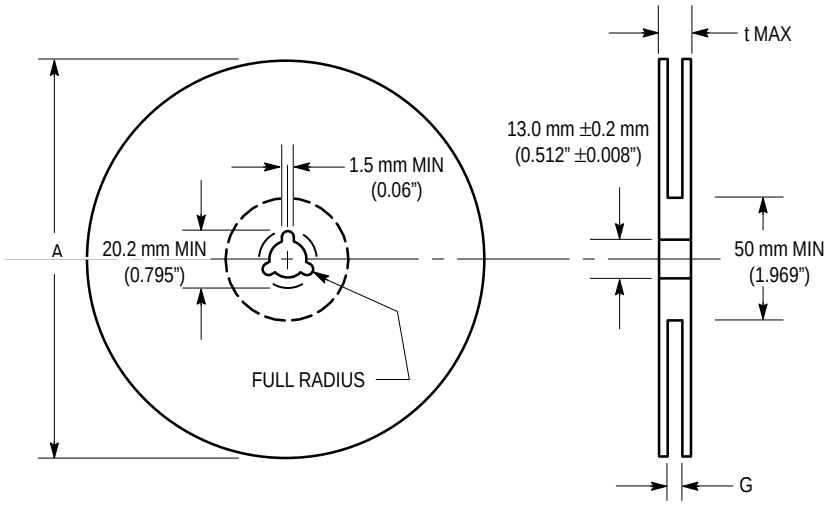


Figure 6. Reel Dimensions

REEL DIMENSIONS

Tape Size	A Max	G	t Max
8 mm	330 mm (13")	8.400 mm, +1.5 mm, –0.0 (0.33", +0.059", –0.00)	14.4 mm (0.56")

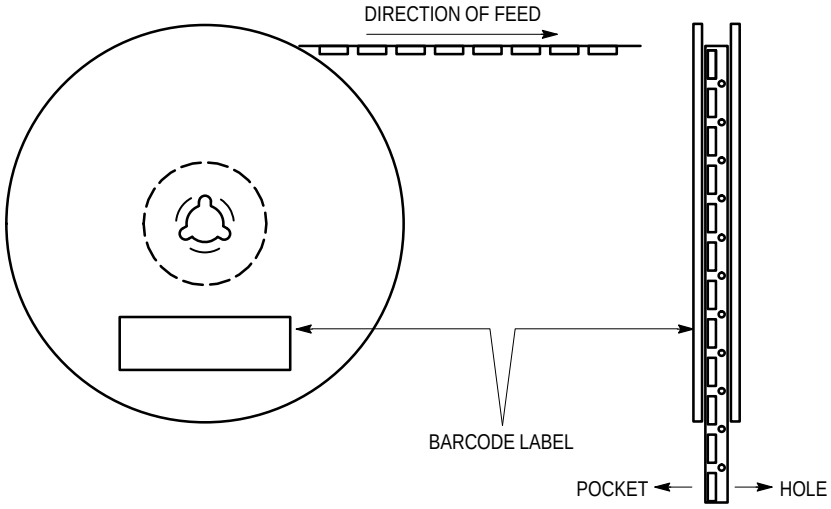


Figure 7. Reel Winding Direction

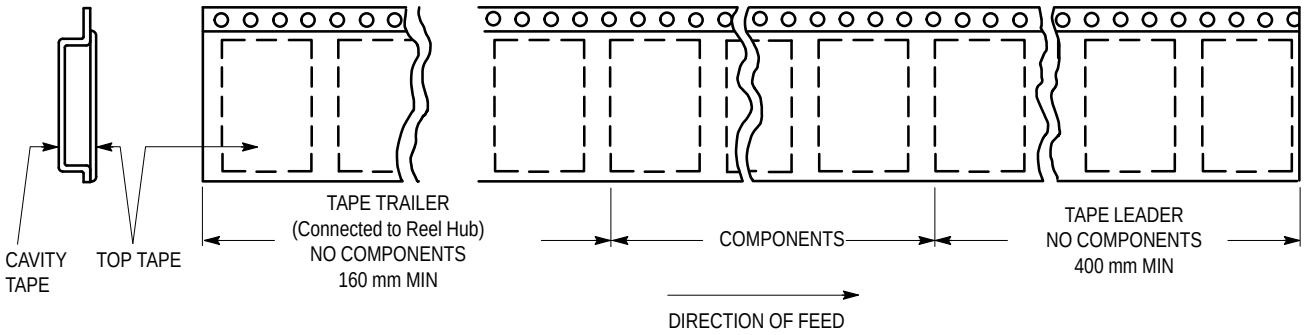


Figure 8. Tape Ends for Finished Goods

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