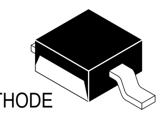
MBRM120LT3

Designer's™ Data Sheet

Surface Mount Schottky Power Rectifier

POWERMITE® Power Surface Mount Package

SCHOTTKY BARRIER RECTIFIER
1.0 AMPERES
20 VOLTS



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The Schottky Powermite employs the Schottky Barrier principle with a barrier metal and epitaxial construction that produces optimal forward voltage drop–reverse current tradeoff. The advanced packaging techniques provide for a highly efficient micro miniature, space saving surface mount Rectifier. With its unique heatsink design, the Powermite has the same thermal performance as the SMA while being 50% smaller in footprint area, and delivering one of the lowest height profiles, < 1.1 mm in the industry. Because of its small size, it is ideal for use in portable and battery powered products such as cellular and cordless phones, chargers, notebook computers, printers, PDAs and PCMCIA cards. Typical applications are ac/dc and dc–dc converters, reverse battery protection, and "Oring" of multiple supply voltages and any other application where performance and size are critical.

Features:

- Low Profile — Maximum Height of 1.1 mm
- Small Footprint — Footprint Area of 8.45 mm2
- Low V_F Provides Higher Efficiency and Extends Battery Life
- Supplied in 12 mm Tape and Reel — 12,000 Units per Reel
- Low Thermal Resistance with Direct Thermal Path of Die on Exposed Cathode Heat Sink

Mechanical Characteristics:

- Powermite is JEDEC Registered as D0–216AA
- Case: Molded Epoxy
- Epoxy Meets UL94, VO at 1/8″
- Weight: 62 mg (approximately)
- Device Marking: BCF
- Lead and Mounting Surface Temperature for Soldering Purposes. 260°C Maximum for 10 Seconds

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	V
Average Rectified Forward Current (At Rated V_R, T_C = 135°C)	I_O	1.0	A
Peak Repetitive Forward Current (At Rated V_R, Square Wave, 100 kHz, T_C = 135°C)	I_{FRM}	2.0	A
Non–Repetitive Peak Surge Current (Non–Repetitive peak surge current, halfwave, single phase, 60 Hz)	I_{FSM}	50	A
Storage Temperature	T_{stg}	–55 to 150	°C
Operating Junction Temperature	T_J	–55 to 125	°C
Voltage Rate of Change (Rated V_R, T_J = 25°C)	dv/dt	10,000	V/µs

THERMAL CHARACTERISTICS

Thermal Resistance – Junction–to–Lead (Anode) (1) Thermal Resistance – Junction–to–Tab (Cathode) (1) Thermal Resistance – Junction–to–Ambient (1)	R_{tjl} R_{tjtab} R_{tja}	35 23 277	°C/W

(1) Mounted with minimum recommended pad size, PC Board FR4, See Figures 9 & 10.

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Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Rev 1

ELECTRICAL CHARACTERISTICS

Maximum Instantaneous Forward Voltage (2), See Figure 2	V_F	T_J = 25°C	T_J = 85°C	V
(I_F = 0.1 A) (I_F = 1.0 A) (I_F = 3.0 A)		0.34 0.45 0.65	0.26 0.415 0.67	
Maximum Instantaneous Reverse Current, See Figure 4	I_R	T_J = 25°C	T_J = 85°C	mA
(V_R = 20 V) (V_R = 10 V)		0.40 0.10	25 18	

(2) Pulse Test: Pulse Width ≤ 250 µs, Duty Cycle ≤ 2%.

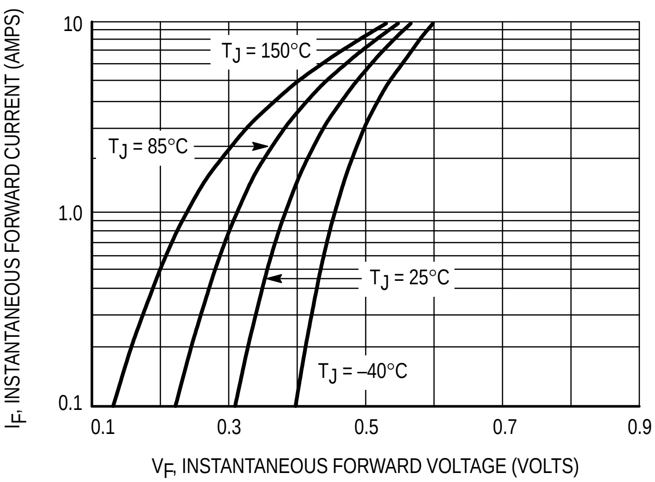


Figure 1. Typical Forward Voltage

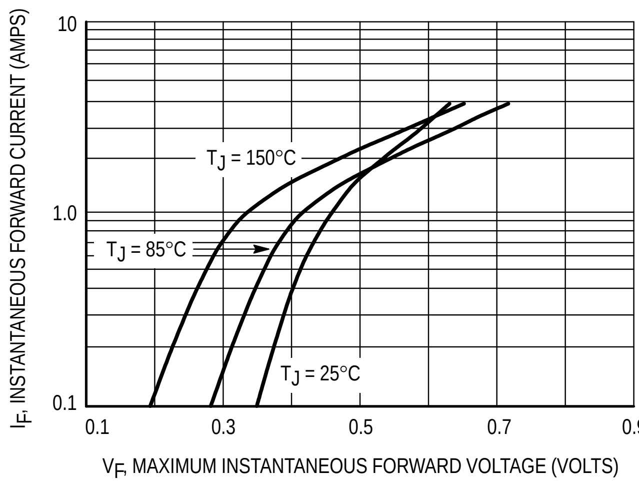


Figure 2. Maximum Forward Voltage

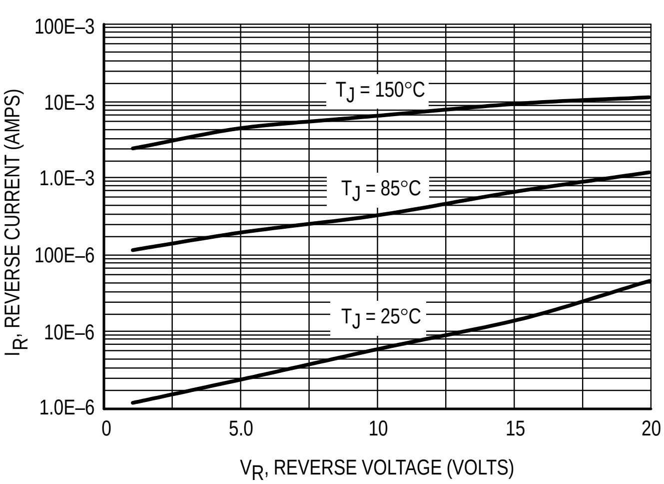


Figure 3. Typical Reverse Current

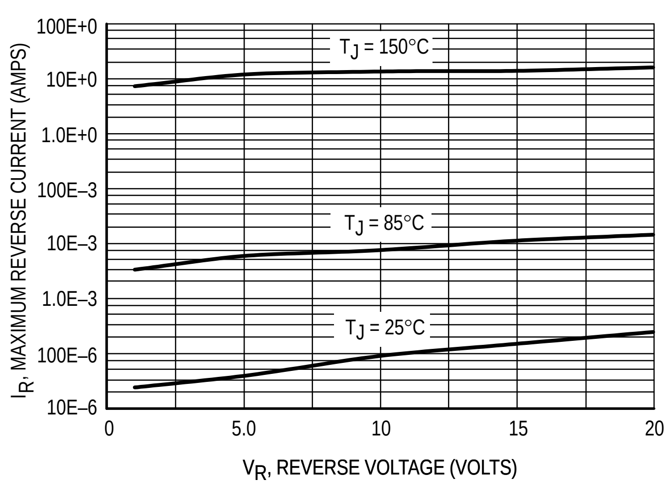


Figure 4. Maximum Reverse Current

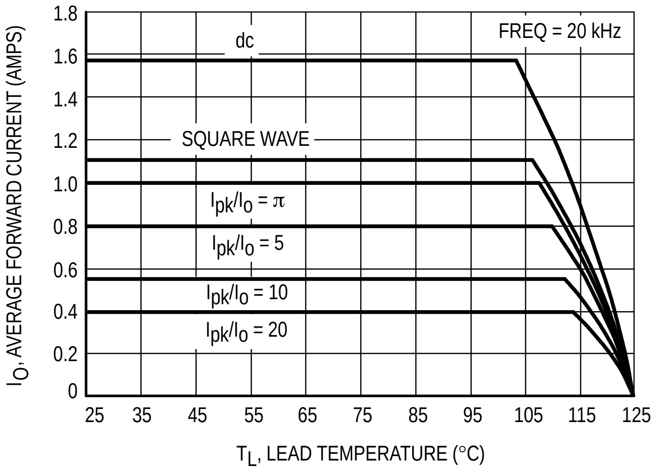


Figure 5. Current Derating

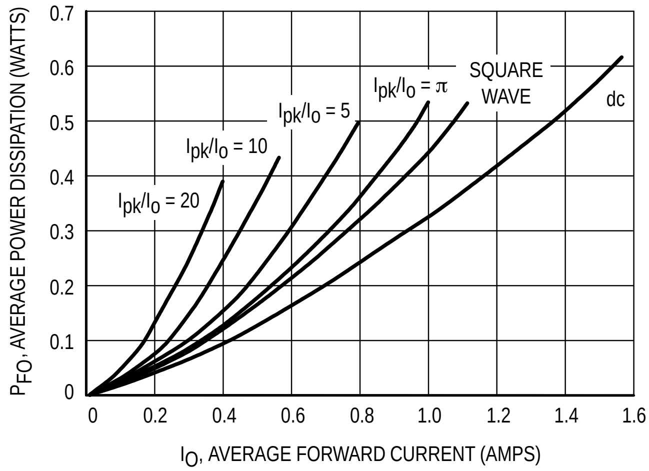


Figure 6. Forward Power Dissipation

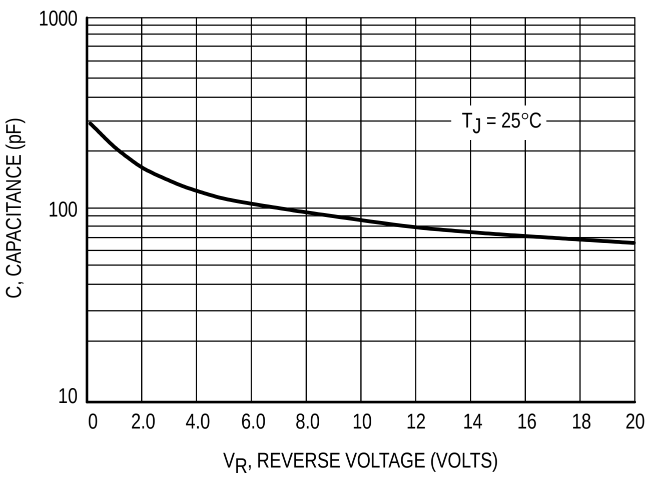


Figure 7. Capacitance

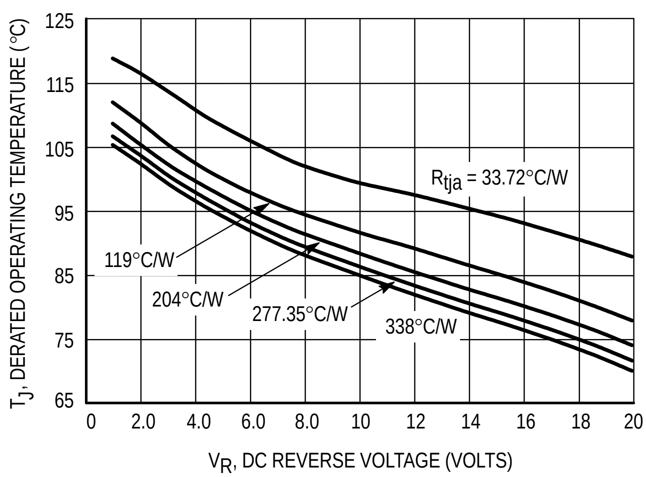


Figure 8. Typical Operating Temperature Derating*

* Reverse power dissipation and the possibility of thermal runaway must be considered when operating this device under any reverse voltage conditions. Calculations of T_J therefore must include forward and reverse power effects. The allowable operating T_J may be calculated from the equation: $T_J = T_{Jmax} - r(t)(Pf + Pr)$ where

r(t) = thermal impedance under given conditions,
Pf = forward power dissipation, and
Pr = reverse power dissipation

This graph displays the derated allowable T_J due to reverse bias under DC conditions only and is calculated as $T_J = T_{Jmax} - r(t)Pr$, where r(t) = Rthja. For other power applications further calculations must be performed.

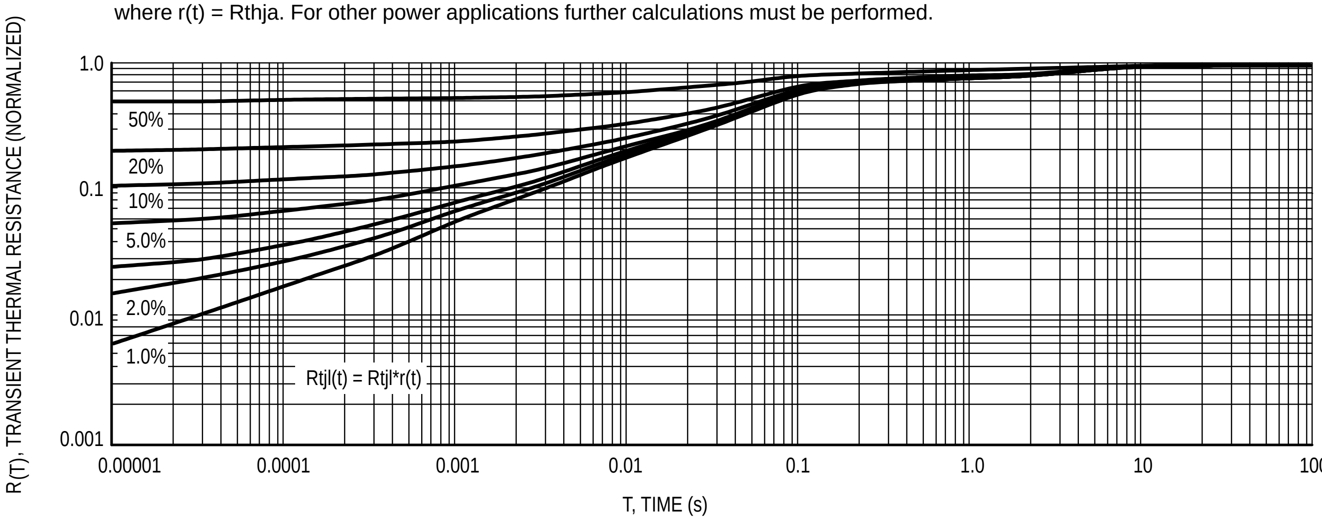


Figure 9. Thermal Response Junction to Lead

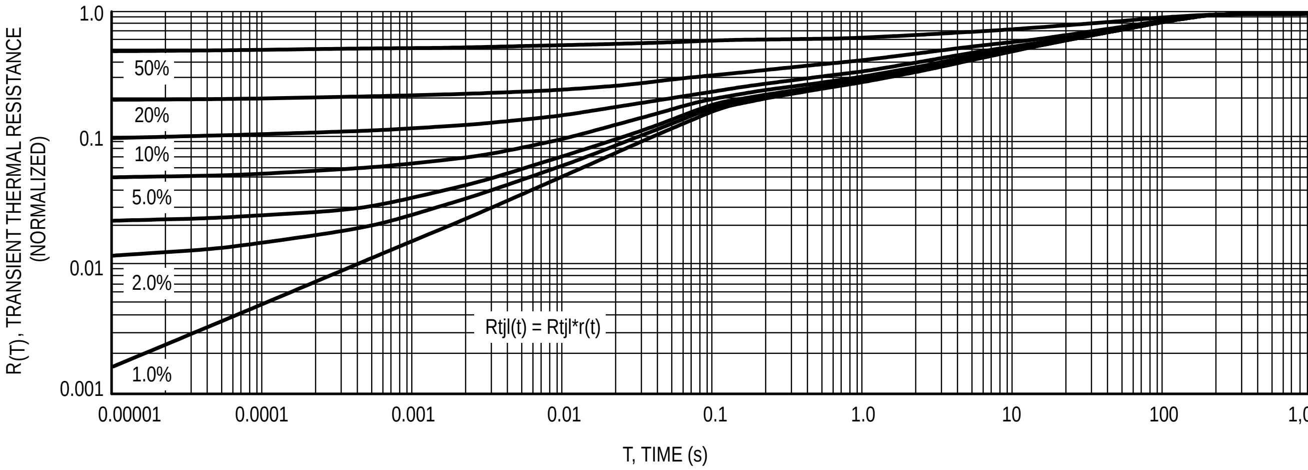
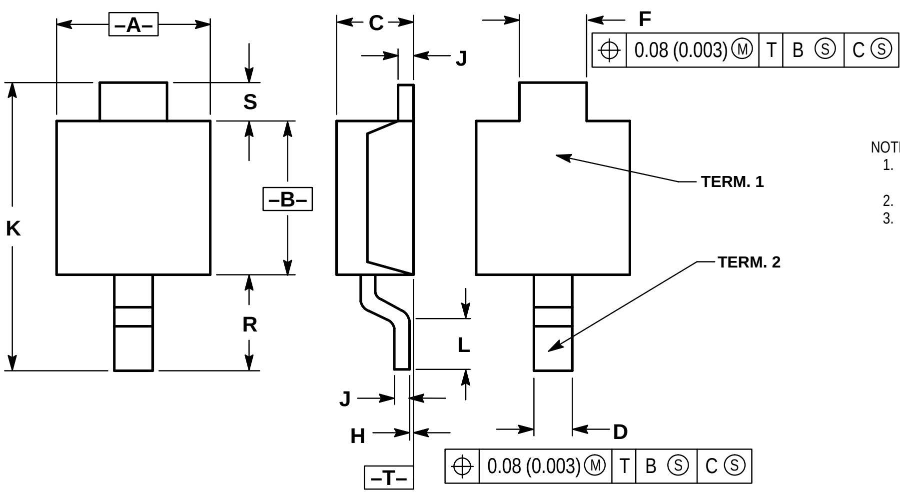


Figure 10. Thermal Response Junction to Ambient

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.75	2.05	0.069	0.081
B	1.75	2.18	0.069	0.086
C	0.85	1.15	0.033	0.045
D	0.40	0.69	0.016	0.027
F	0.70	1.00	0.028	0.039
H	–0.05	+0.10	–0.002	+0.004
J	0.10	0.25	0.004	0.010
K	3.60	3.90	0.142	0.154
L	0.50	0.80	0.020	0.031
R	1.20	1.50	0.047	0.059
S	0.50 REF		0.019 REF	

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