

SANYO

No. 2076D

LC6520C, 6522C, LC6520H, 6522H**Single-Chip 4-Bit Microcomputers for
Medium/Large-Scale Control-Oriented Applications**

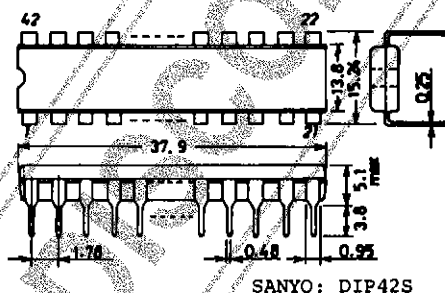
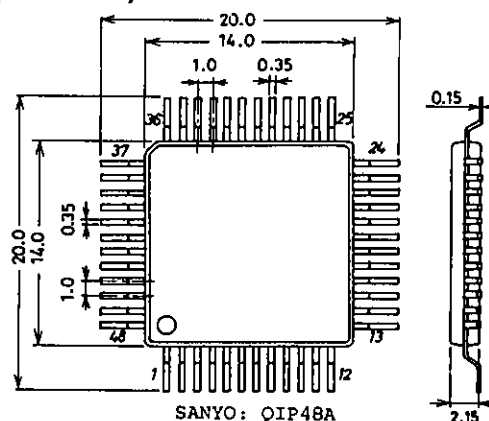
The LC6520C/H are single-chip 4-bit microcomputers that contain a 4K-byte ROM, 1K-bit RAM, have 42 pins, and are fabricated using CMOS process technology. Besides 8 input/output common ports of 32 pins and an input port of 4 pins, the LC6520C/H have specific ports that are used to provide the interrupt function, 4-bit/8-bit serial input/output function, and burst pulse output function. All output ports are of the open drain type with a withstand voltage of 15 V and a drive current of 20 mA and have the option of containing a pull-up resistance bitwise.

The LC6520C/H are the same as our LC6500 series in the basic architecture of the CPU and the instruction set, but are made more powerful in the stack level and the cycle time.

The LC6522C/H are the same as the LC6520C/H, except that they contain a 2k-byte ROM, 512-bit RAM.

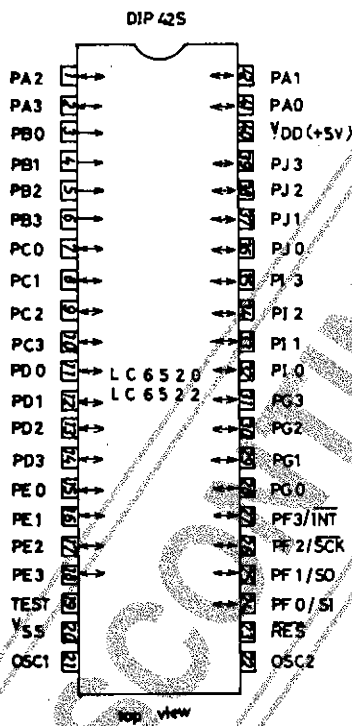
Features

- Instruction set with 80 instructions (Common to the LC6500 series)
- ROM/RAM
 - : 4096 bytes/1024 bits (LC6520C/H)
 - : 2048 bytes/512 bits (LC6522C/H)
- Instruction cycle time: 6 μ s (C version, $V_{DD} = 3$ to 5.5V)
2.77 μ s (C version, $V_{DD} = 4$ to 5.5V)
9.92 μ s (H version, $V_{DD} = 4.5$ to 5.5V)
- Serial input/output interface x 1 (4 bits/8 bits program-selectable)
- I/O ports
 - Input port: 4 pins
 - Input/output common ports: 32 pins
 - Input/output withstand voltage: 15 V max (all input/output ports)
 - Output current: 20 mA max (all output ports)
 - Pull-up resistance: May be contained bitwise by option. (All output ports)
 - Output level during reset: For ports C, D, output (H or L) during reset may be specified portwise by option.

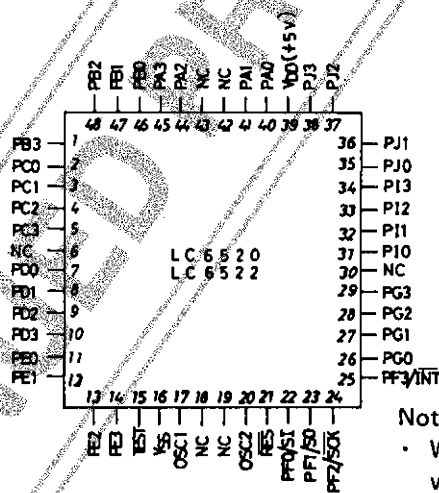
Package Dimensions 3025B-D42S1C
(unit: mm)**Package Dimensions 3052A-Q48A1C**
(unit: mm)

- Interrupt function
Timer interrupt: 1
INT pin or serial I/O interrupt: 1
- Stack level: 8 levels (common with interrupt)
- Timer: 4-bit prescaler + 8-bit programmable timer
- Burst pulse (64 x cycle time, duty 50%) output function
- Oscillator option
Circuit mode: Ceramic mode, RC mode, external clock mode (200 kHz to 4.2 MHz)
(Xtal OSC constants are being checked.)
Predivider option: 1/1, 1/3, 1/4
- Standby function: Standby function provided by the HALT instruction
- Supply Voltage: 3 to 5.5 V (C version)
4.5 to 5.5 V (H version)
- Package: DIP42 shrink type, QIP48

Pin Assignment



QIP48



Note)

- When mounting the QIP version on the board, do not dip it in solder.
- Nothing must be connected to NC pin.

Pin Name

- OSC1, OSC2: RC, ceramic resonator, or X'tal for OSC
- INT: Interrupt
- RES: Reset
- PA0-3: Input/output common port
- PB0-3: Input port
- PC0-3: Input/output common port
- PD0-3: Input/output common port
- PE0-3: Input/output common port
- PF0-3: Input/output common port
- PG0-3: Input/output common port
- PI0-3: Input/output common port
- PJ0-3: Input/output common port
- SCK: Serial Input/output port
- SO: Serial Input/output port
- SI: Serial Input/output port
- TEST: Test

Pin Description

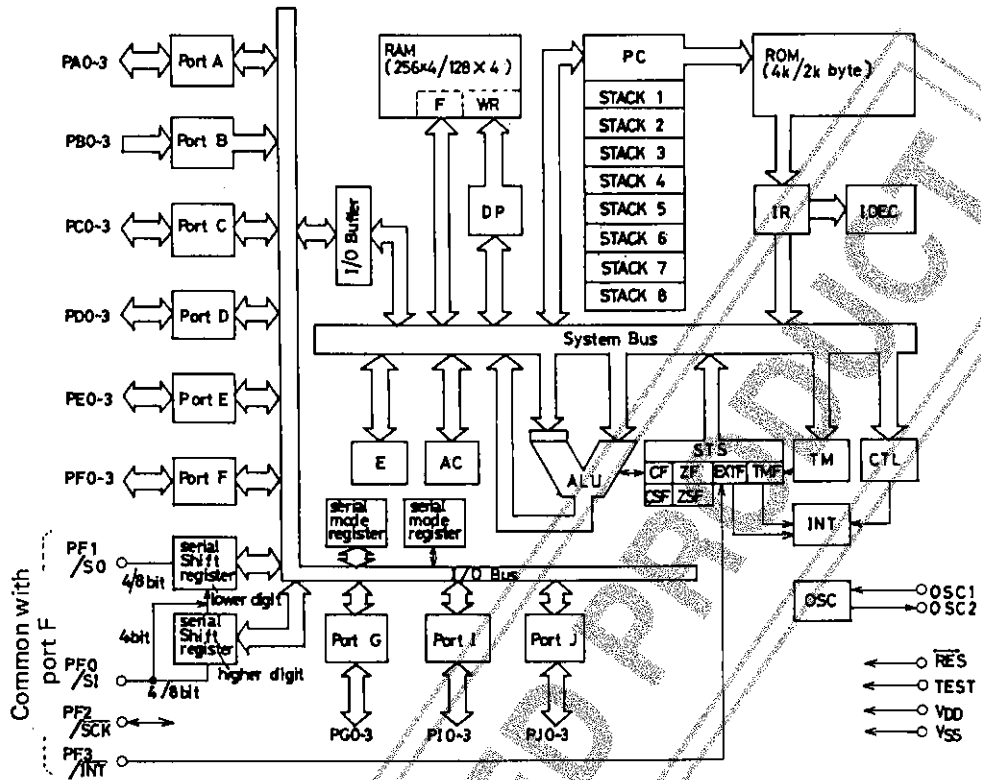
Pin Name	Pins	I/O	Functions	Options	During Reset
VDD VSS	1 1		Power supply		
OSC1	1	Input	<ul style="list-style-type: none"> Pin for externally connecting R, C or a ceramic resonator for system clock generation 	<ol style="list-style-type: none"> External clock input 2-pin RC OSC 2-pin ceramic resonator OSC 	
OSC2	1	Output	<ul style="list-style-type: none"> For the external clock mode, the OSC2 pin is open. 	<ol style="list-style-type: none"> Predivider option <ol style="list-style-type: none"> No. predivider 1/3 predivider 1/4 predivider 	
PA0 PA1 PA2 PA3	4	Input/output	<ul style="list-style-type: none"> Input/output common port A0 to 3. <ul style="list-style-type: none"> 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instructions) Single-bit set/reset (SPB, RPB instructions) Standby is controlled by the PA3 (or PA0 to 3). The PA3 (or PA0 to 3) pin must be free from chattering during the HALT instruction execution cycle. 	<ol style="list-style-type: none"> Open drain type output With pull-up resistance (1), (2): Specified bit by bit.	<ul style="list-style-type: none"> "H" output (Output Nch transistor OFF)
PB0 PB1 PB2 PB3	4	Input	<ul style="list-style-type: none"> Input Port B0 to 3. <ul style="list-style-type: none"> 4-bit input (IP instruction) Single-bit decision (BP, BNP instructions) 		
PC0 PC1 PC2 PC3	4	Input/output	<ul style="list-style-type: none"> Input/output common port C0 to 3. The functions are the same as for the PA0 to 3. (Note) Output ("H" or "L") during reset may be specified by option. (Note) No standby control function is provided.	<ol style="list-style-type: none"> Open drain type output With pull-up resistance Output during reset: "H" Output during reset: "L" <ul style="list-style-type: none"> (1), (2): Specified bit by bit. (3), (4): Specified in a group of 4 bits. 	<ul style="list-style-type: none"> "H" output "L" output (Option-selectable)
PD0 PD1 PD2 PD3	4	Input/output	<ul style="list-style-type: none"> Input/output common port D0 to 3. The functions, options are the same as for the PC0 to 3. 	Same as for the PC0 to 3.	Same as for the PC0 to 3.
PE0 PE1 PE2 PE3	4	Input/output	<ul style="list-style-type: none"> Input/output common port E0 to 3. <ul style="list-style-type: none"> 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instructions) Single-bit set/reset (SPB, RPB instructions) PE0: With burst pulse (64T_{cyc}) output function 	<ol style="list-style-type: none"> Open drain type output With pull-up resistance (1), (2): Specified bit by bit.	<ul style="list-style-type: none"> "H" output (Output Nch transistor OFF)

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Pin Name	Pins	I/O	Functions	Options	During Reset
PF ₀ /SI PF ₁ /SO PF ₂ / $\overline{\text{SCK}}$ PF ₃ / $\overline{\text{INT}}$	4	Input/output	<ul style="list-style-type: none"> Input/output port F₀ to 3 The functions, options are the same as for the PE₀ to 3. However, no burst pulse output function is provided. PF₀ to 3: Also used for serial interface, $\overline{\text{INT}}$ input. Program-selectable. 4 bits/8 bits of serial input/output: Program-selectable SI: Serial input port SO: Serial output port SCK: Serial clock input/output $\overline{\text{INT}}$: Interrupt request input 	Same as for the PE ₀ to 3.	Same as for the PE ₀ to 3. Serial port: Disable Interrupt source: $\overline{\text{INT}}$
PG ₀ PG ₁ PG ₂ PG ₃	4	Input/output	<ul style="list-style-type: none"> Input/output common port G₀ to 3 The functions, options are the same as for the PE₀ to 3. However, no burst pulse output function is provided. 	Same as for the PE ₀ to 3.	Same as for the PE ₀ to 3.
PI ₀ PI ₁ PI ₂ PI ₃	4	Input/output	<ul style="list-style-type: none"> Input/output common port I₀ to 3 The functions, options are the same as for the PG₀ to 3. 	Same as for the PG ₀ to 3.	Same as for the PG ₀ to 3.
PJ ₀ PJ ₁ PJ ₂ PJ ₃	4	Input/output	<ul style="list-style-type: none"> Input/output common port J₀ to 3 The functions, options are the same as for the PG₀ to 3. 	Same as for the PG ₀ to 3.	Same as for the PG ₀ to 3.
$\overline{\text{RES}}$	1	Input	<ul style="list-style-type: none"> System reset input For power-up reset, C is connected externally. For reset start, "L" level is applied for 4 clock cycles or more. 		
TEST	1	Input	<ul style="list-style-type: none"> LSI test pin Normally connected to V_{SS} 		

System Block Diagram



- | | | | |
|------|---------------------------|----------|---------------------------------|
| RAM: | Data memory | ROM: | Program memory |
| F: | Flag | PC: | Program counter |
| WR: | Working register | INT: | Interrupt control |
| AC: | Accumulator | IR: | Instruction register |
| ALU: | Arithmetic and logic unit | I.DEC: | Instruction decoder |
| DP: | Data pointer | CF, CSF: | Carry flag, carry save flag |
| E: | E register | ZF, ZSF: | Zero flag, zero save flag |
| CTL: | Control register | EXTF: | External interrupt request flag |
| OSC: | Oscillator | TMF: | Internal interrupt request flag |
| TM: | Timer | | |
| STS: | Status register | | |

DISCONTINUED

Oscillator Circuit Option

Option Name	Circuit	Conditions, etc.
1. External Clock		<ul style="list-style-type: none"> Input: Schmitt type
2. 2-pin RC OSC		<ul style="list-style-type: none"> Input: Schmitt type
3. Ceramic Resonator OSC		

• Predivider Option

Option Name	Circuit	Conditions, etc.
1. No predivider		<ul style="list-style-type: none"> Applicable to all of 3 OSC options. The OSC frequency, external clock do not exceed 1444 kHz. (LC6520C, LC6522C) The OSC frequency, external clock do not exceed 4330 kHz. (LC6520H, LC6522H) Refer to Table of OSC, Predivider Option (Table 2).
2. 1/3 predivider		<ul style="list-style-type: none"> Applicable to only 2 options of external clock, ceramic resonator OSC. The OSC frequency, external clock do not exceed 4330 kHz. Refer to Table of OSC, Predivider Option (Table-2).
3. 1/4 predivider		<ul style="list-style-type: none"> Applicable to only 2 options of external clock, ceramic resonator OSC. The OSC frequency, external clock do not exceed 4330 kHz. Refer to table of OSC, Predivider Option (Table 2).

Options of Ports C, D Output Level during Reset

For input/output common ports C, D, either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output during reset: "H" level	All of 4 bits of ports C, D
2. Output during reset: "L" level	All of 4 bits of ports C, D

Options of Port Output Configuration

For each input/output-common port, either of the following two output configurations may be selected by option (bitwise).

Option Name	Circuit	Conditions, etc.
1. Open drain type output		
2. Output with pull-up resistance		

DISCONTINUED PRODUCT

Development Support

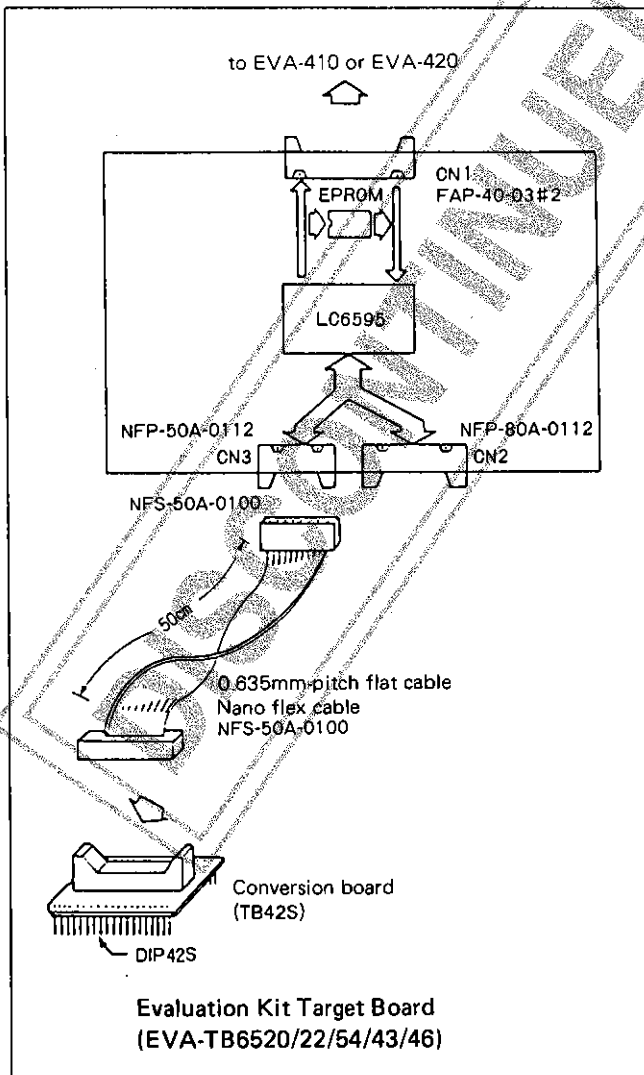
The following are available to support the LC6520, LC6522 program development.

- (1) User's Manual
"LC6554 Series User's Manual" No. E21B. (Issued in December, 1987)
- (2) Development Tool Manual
For the EVA-410 system, refer to the description of Development Support Tools in "LC6554 Series User's Manual". For the EVA-800 system, refer to "EVA-800-LC6554 Series Development Tool Manual".
- (3) Development Tools
 - 1) For program development (EVA-410 system)
 - i. MS-DOS host computer system (Note 1)
 - ii. MS-DOS base cross assembler (LC65S.EXE)
 - iii. Evaluation kit (EVA-410C or EVA-420)
 - iv. Evaluation kit target board (EVA-TB6520/22/54/43/46), evaluation chip (LC6595)
 - 2) For program evaluation
 - i. Piggyback (LC65PG20/22), with socket for conversion of number of piggyback pins

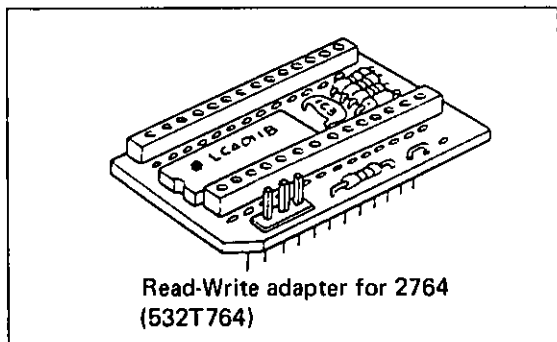
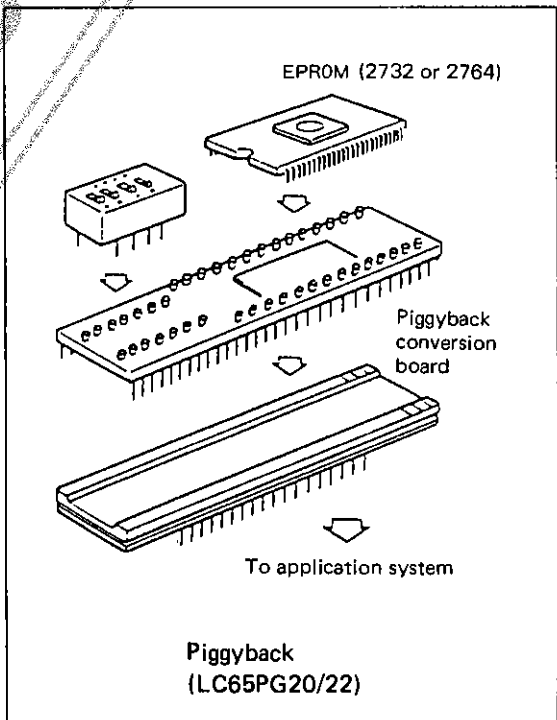
Note. For notes on program evaluation, do not fail to refer to "5-3-1. Notes on when evaluating programs for the LC6520/22" in "LC6554 Series User's Manual".

Appearance of Application Development Tools

EVA-410 System



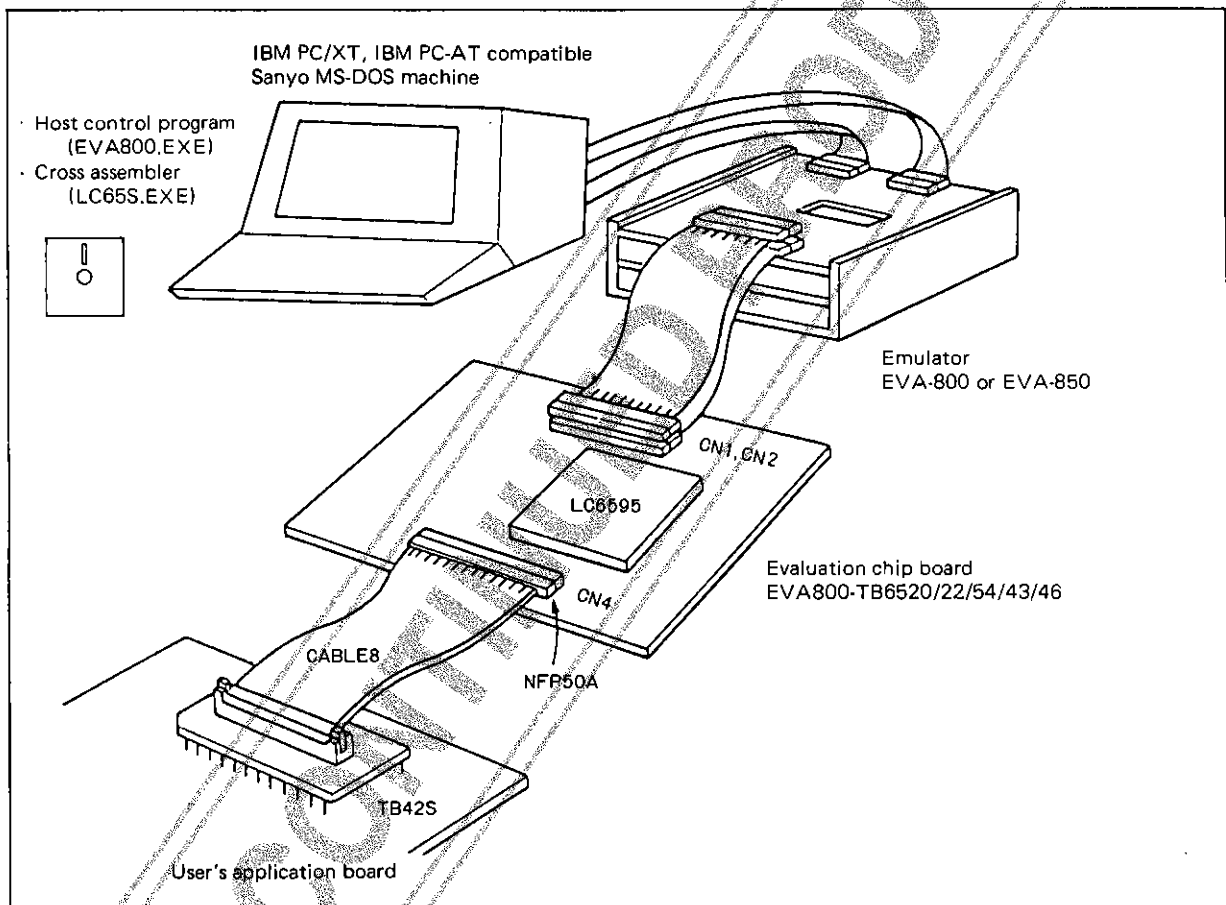
Piggyback



- 3) For program development (EVA-800 system)
 - i. IBM PC/XT, IBM PC-AT (Note 1) compatible Sanyo MS-DOS machine
 - ii. Cross assemblerMS-DOS base cross assembler: (LC65S.EXE)
 - iii. Host control program: (EVA800.EXE)
 - iv. Evaluation chip: LC6595
 - v. Emulator : EVA-800 or EVA-850 control board and evaluation chip board (Note 2)

Appearance of Development Support System

EVA-800 System



(Note 1) IBM PC/XT, IBM PC-AT: Products of IBM Corporation
 MS-DOS: Trademark of Microsoft Corporation

(Note 2) The EVA-800 is a general term for emulator. A suffix (A, B ...) is added at the end of EVA-800 as the EVA-800 is improved to be a newer version. Do not use the EVA-800 with no suffix added.

Main Specifications of the LC6520C, 6522C

Absolute Maximum Ratings/ $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

			unit
Maximum Supply Voltage	$V_{DD\text{ max}}$	V_{DD}	-0.3 to +7.0 V
Output Voltage	V_o	OSC2	Allowable up to voltage generated V
Input Voltage	V_i (1)	OSC1 (Note 1)	-0.3 to $V_{DD}+0.3$ V
	V_i (2)	TEST, RES	-0.3 to $V_{DD}+0.3$ V
	V_i (3)	PB0 to 3	-0.3 to +15 V
Input/Output Voltage	V_{IO} (1)	Port of OD type	-0.3 to +15 V
	V_{IO} (2)	Port of PU type	-0.3 to $V_{DD}+0.3$ V
Peak Output Current	I_{OP}	Input/output port	-2 to +20 mA
Average Output Current	I_{OA}	Input/output port:	-2 to +20 mA
		Per pin over the period of 100 msec.	
	ΣI_{OA} (1)	Total current of PA0 to 3, PC0 to 3, PD0 to 3 and PE0 to 3 (Note 2)	-30 to +140 mA
	ΣI_{OA} (2)	Total current of PF0 to 3, PG0 to 3, PI0 to 3 and PJ0 to 3, (Note 2)	-30 to +140 mA
Allowable Power Dissipation	$P_d\text{ max}$ (1)	DIP package, $T_a = -30$ to $+70^\circ\text{C}$	600 mW
	$P_d\text{ max}$ (2)	QIP package, $T_a = -30$ to $+70^\circ\text{C}$	400 mW
Operating Temperature	T_{opr}		-30 to +70 $^\circ\text{C}$
Storage Temperature	T_{stg}		-55 to +125 $^\circ\text{C}$

Allowable Operating Conditions/ $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{V}$, $V_{DD} = 3.0$ to 5.5V

			min	typ	max	unit
Operating Supply Voltage	V_{DD}	V_{DD}	3.0		5.5	V
Standby Supply Voltage	V_{st}	V_{DD} : RAM, resistor hold (Note 3)	1.8		5.5	V
"H"-Level Input Voltage	V_{IH} (1)	Port of OD type, PB0 to 3: Output Nch Tr OFF	$0.7V_{DD}$		+13.5	V
	V_{IH} (2)	Port of PU type: Output Nch Tr OFF	$0.7V_{DD}$		V_{DD}	V
	V_{IH} (3)	SCK, SI, INT of OD type: Output Nch Tr OFF	$0.8V_{DD}$		+13.5	V
	V_{IH} (4)	SCK, SI, INT of PU type: Output Nch Tr OFF	$0.8V_{DD}$		V_{DD}	V
	V_{IH} (5)	RES	$0.8V_{DD}$		V_{DD}	V
	V_{IH} (6)	OSC1: External clock mode	$0.8V_{DD}$		V_{DD}	V
"L"-Level Input Voltage	V_{IL} (1)	PORT: $V_{DD} = 4$ to 5.5V , Output Nch Tr OFF	V_{SS}		$0.3V_{DD}$	V
	V_{IL} (2)	PORT: Output Nch Tr OFF	V_{SS}		$0.25V_{DD}$	V
	V_{IL} (3)	INT, SCK, SI: $V_{DD} = 4$ to 5.5V Output Nch Tr OFF	V_{SS}		$0.25V_{DD}$	V
	V_{IL} (4)	INT, SCK, SI: Output Nch Tr OFF	V_{SS}		$0.2V_{DD}$	V
	V_{IL} (5)	OSC1: $V_{DD} = 4$ to 5.5V , External clock mode	V_{SS}		$0.25V_{DD}$	V
	V_{IL} (6)	OSC1: External clock mode	V_{SS}		$0.2V_{DD}$	V
	V_{IL} (7)	TEST: $V_{DD} = 4$ to 5.5V	V_{SS}		$0.3V_{DD}$	V
	V_{IL} (8)	TEST	V_{SS}		$0.25V_{DD}$	V
	V_{IL} (9)	RES: $V_{DD} = 4$ to 5.5V	V_{SS}		$0.25V_{DD}$	V
	V_{IL} (10)	RES	V_{SS}		$0.2V_{DD}$	V
Operating Frequency (Cycle Time)	f_{op} (T_{cyc})	($V_{DD} = 4.0$ to 5.5V)	(2.77) (6.0)	See Table 2.	(20) (20)	(μs) (μs)

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External Clock Conditions (When the external clock or 2-pin RC OSC option is selected)		min	typ	max	unit
Frequency	f_{ext}	OSC1: Fig. 1	See Table 2.		
Pulse Width	$\left\{ \begin{array}{l} textH, \\ textL \end{array} \right.$	OSC1: $V_{DD} = 4$ to $5.5V$, Fig. 1	90		ns
Rise/Fall Time	$\left\{ \begin{array}{l} textR, \\ textF \end{array} \right.$	OSC1: Fig. 1	180		ns
		OSC1: $V_{DD} = 4$ to $5.5V$, Fig. 1		30	ns
		OSC1: Fig. 1		100	ns
Oscillation Guaranteed Constants					
2-Pin RC Oscillation	C_{ext}	OSC1, OSC2: $V_{DD} = 4$ to $5.5V$, Fig. 2	$220 \pm 5\%$		pF
	R_{ext}	OSC1, OSC2: $V_{DD} = 4$ to $5.5V$, Fig. 2	$6.8 \pm 1\%$		k Ω
	C_{ext}	OSC1, OSC2: Fig. 2	$270 \pm 5\%$		pF
	R_{ext}	OSC1, OSC2: Fig. 2	$15 \pm 1\%$		k Ω
Ceramic Resonator Oscillation		Fig. 3	See Table 1.		
Electrical Characteristics/$T_a = -30$ to $+70^\circ C$, $V_{SS} = 0V$, $V_{DD} = 3.0$ to $5.5V$					
"H"-Level Input Current	I_{IH} (1)	Port of open drain type, PB0 to 3: Output Nch Tr OFF, Including OFF leakage current of Nch Tr, $V_{IN} = +13.5V$		+5.0	μA
"L"-Level Input Current	I_{IL} (2)	OSC1: External clock mode, $V_{IN} = V_{DD}$		+1.0	μA
	I_{IL} (1)	Port of open drain type, PB0 to 3: Output Nch Tr OFF, $V_{IN} = V_{SS}$	-1.0		μA
	I_{IL} (2)	Port with pull-up resistance: Output Nch Tr OFF, $V_{IN} = V_{SS}$	-1.3	-0.35	mA
	I_{IL} (3)	RES: $V_{IN} = V_{SS}$	-45	-10	μA
	I_{IL} (4)	OSC1: External clock mode, $V_{IN} = V_{SS}$	-1.0		μA
"H"-Level Output Voltage	V_{OH} (1)	Port with pull-up resistance: $V_{DD} = 4$ to $5.5V$, $I_{OH} = -50 \mu A$	$V_{DD} - 1.2$		V
	V_{OH} (2)	Port with pull-up resistance: $I_{OH} = -10 \mu A$	$V_{DD} - 0.5$		V
"L"-Level Output Voltage	V_{OL} (1)	Port: $V_{DD} = 4$ to $5.5V$, $I_{OL} = 10$ mA		1.5	V
	V_{OL} (2)	Port: $I_{OL} = 1$ mA, When I_{OL} of each port is 1 mA or less.		0.5	V
Hysteresis Voltage	V_{Hys}	RES, INT, SCK, SI, OSC1 of Schmitt type (Note 6)	$0.1V_{DD}$		V
Current Dissipation					
2-Pin RC Oscillation	I_{DDOP} (1)	Operation mode, Output Nch Tr OFF, Port = V_{DD} V_{DD} : $V_{DD} = 4$ to $5.5V$, Fig. 2 $f_{osc} = 750$ kHz typ	2	5	mA
	I_{DDOP} (2)	V_{DD} : Fig. 2 $f_{osc} = 350$ kHz typ	1.5	4.5	mA
Ceramic Resonator Oscillation	I_{DDOP} (3)	V_{DD} : Fig. 3 $V_{DD} = 4$ to $5.5V$, 4MHz, 1/3 predivider	5	10	mA
	I_{DDOP} (4)	V_{DD} : Fig. 3 $V_{DD} = 4$ to $5.5V$, 4MHz, 1/4 predivider	5	10	mA
	I_{DDOP} (5)	V_{DD} : Fig. 3 400kHz	1.5	4	mA
	I_{DDOP} (6)	V_{DD} : $V_{DD} = 4$ to $5.5V$, Fig. 3 800kHz	2	5	mA
External Clock	I_{DDOP} (7)	V_{DD} : 200 kHz to 667 kHz, 1/1 predivider 600 kHz to 2000 kHz, 1/3 predivider 800 kHz to 2667 kHz, 1/4 predivider	2	5	mA
	I_{DDOP} (8)	V_{DD} : $V_{DD} = 4$ to $5.5V$, 200 kHz to 1444 kHz, 1/1 predivider 600 kHz to 4330 kHz, 1/3 predivider 800 kHz to 4330 kHz, 1/4 predivider	3	10	mA
Standby Mode	I_{DDSt}	V_{DD} : $V_{DD} = 5.5V$ (Output Nch Tr OFF, V_{DD} : $V_{DD} = 3V$ Port = V_{DD})	0.05	10	μA
			0.025	5	μA

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			min	typ	max	unit
Oscillation Characteristics						
Ceramic Resonator Oscillation						
Oscillation Frequency	f _{CFOSC} (Note 4)	OSC1, OSC2: Fig. 3 f _o = 400 kHz OSC1, OSC2: V _{DD} = 4 to 5.5V, Fig. 3 f _o = 800 kHz	392 784	400 800	408 816	kHz
		OSC1, OSC2: V _{DD} = 4 to 5.5V, Fig. 3 f _o = 3 MHz, 1/3 predivider, 1/4 predivider	2940	3000	3060	kHz
		OSC1, OSC2: V _{DD} = 4 to 5.5V, Fig. 3 f _o = 4 MHz, 1/3 predivider, 1/4 predivider	3920	4000	4080	kHz
Oscillation Stabilizing Period	t _{CFS}	Fig. 4 f _o = 400 kHz V _{DD} = 4 to 5.5V, Fig. 4 f _o = 4 MHz, 3 MHz, 800 kHz			10 10	ms ms
2-Pin RC Oscillation						
Oscillation Frequency	f _{MOSC} (1)	OSC1, OSC2: V _{DD} = 4 to 5.5V, Fig. 2, C _{ext} = 220 pF±5%, R _{ext} = 6.8 kΩ±1%	515	750	1156	kHz
	f _{MOSC} (2)	OSC1, OSC2: Fig. 2, C _{ext} = 270 pF±5%, R _{ext} = 15 kΩ±1%	222	350	609	kHz
Pull-up Resistance						
I/O Port Pull-up Resistance	R _{pp}	Port of PU type: V _{DD} = 5V		14		kΩ
External Reset Characteristics						
"H"-Level Threshold	V _{tH}		0.5V _{DD}		0.8V _{DD}	V
"L"-Level Threshold	V _{tL}		0.2V _{DD}		0.5V _{DD}	V
Reset Time	TRST			See Fig. 5.		
Pin Capacitance	CP	f = 1 MHz, Other than pins to be tested, V _{IN} = V _{SS}		10		pF
Serial Clock						
Input Clock Cycle Time	t _{CKCY} (1)	\overline{SCK} : V _{DD} = 4 to 5.5V, Fig. 6 \overline{SCK}	3.0 12.0			μs μs
Output Clock Cycle Time	t _{CKCY} (2)	\overline{SCK} (T _{CYCY} = 4 x System clock period), Fig. 6		64 x T _{CYCY}		μs
Input Clock "L"-Level Pulse Width	t _{CKL} (1)	\overline{SCK} : V _{DD} = 4 to 5.5V, Fig. 6 \overline{SCK}	1.0 4.0			μs μs
	t _{CKL} (2)	\overline{SCK} , Fig. 6		32 x T _{CYCY}		μs
Output Clock "L"-Level Pulse Width	t _{CKH} (1)	\overline{SCK} : V _{DD} = 4 to 5.5V, Fig. 6 \overline{SCK}	1.0 4.0			μs μs
	t _{CKH} (2)	\overline{SCK} : Fig. 6		32 x T _{CYCY}		μs
Serial Input						
Data Setup Time	t _{ICK}	SI: Specified for ↑ of \overline{SCK} , Fig. 6	0.5			μs
Data Hold Time	t _{ICKI}	SI: Specified for ↑ of \overline{SCK} , Fig. 6	0.5			μs
Serial Output						
Output Delay Time	t _{CKO}	SO: V _{DD} = 4 to 5.5V, Specified for ↓ of \overline{SCK} , Nch OD only: External 1 kohm, external 50 pF, Fig. 6 SO			0.5 2.0	μs μs
Pulse Output						
Period	t _{PCY}	PE0: T _{CYCY} = 4 x System clock period, Nch OD only: External 1 kohm, external 50 pF, Fig. 7		64 x T _{CYCY}		μs
"H"-Level Pulse Width	t _{PH}	PE0:		32 x T _{CYCY} ±10%		μs
"L"-Level Pulse Width	t _{PL}	PE0:		32 x T _{CYCY} ±10%		μs

Note 1: When oscillated internally under the oscillating conditions in Fig. 3, up to the oscillation amplitude generated is allowable.

Note 2: Average over the period of 100 msec.

Note 3: Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction.
The PA3 (or PA0 to 3) pin must be free from chattering during the HALT instruction execution cycle.

Note 4: f_{CFOSC} represents an oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

Note 5: When mounting the QIP version on the board, do not dip it in solder.

Note 6: The OSC1 becomes the Schmitt type when the OSC option is the 2-pin RC OSC or external clock OSC.

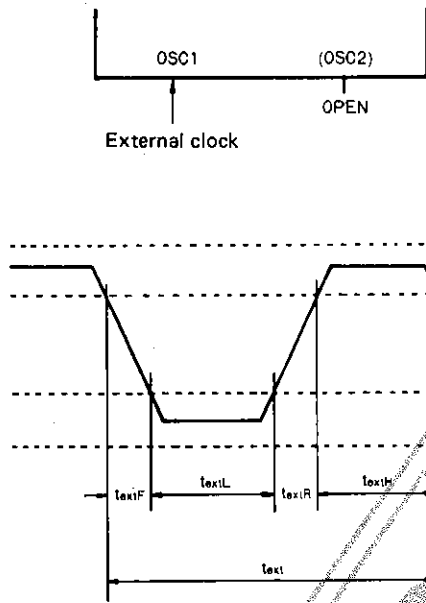


Fig. 1 External Clock Input Waveform

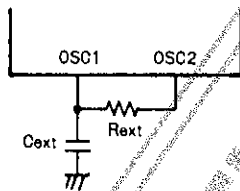


Fig. 2 2-Pin RC Oscillation Circuit

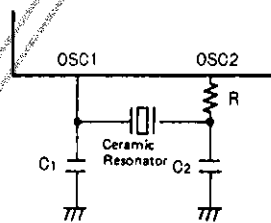


Fig. 3 Ceramic Resonator Oscillation Circuit

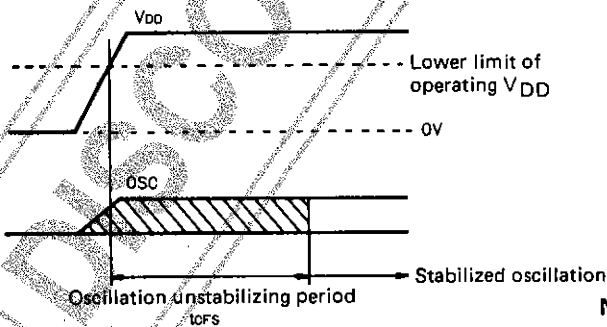


Fig. 4 Oscillation Stabilizing Period

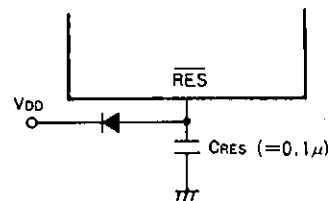


Fig. 5 Reset Circuit

Note 7: When the rise time of the power supply is 0, the reset time becomes 10 ms to 100 ms at $C_{RES} = 0.1 \mu\text{F}$. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10 ms or greater.

4MHz (Murata) CSA4.00MG	C1	33pF ± 10%	800kHz (Murata) CSB800D CSB800K	C1	220pF ± 10%
	C2	33pF ± 10%		C2	220pF ± 10%
	R	0Ω		R	0Ω
4MHz (Kyocera) KBR4.0MS	C1	33pF ± 10%	800kHz (Kyocera) KBR800H	C1	150pF ± 10%
	C2	33pF ± 10%		C2	150pF ± 10%
	R	0Ω		R	0Ω
3MHz (Murata) CSA3.00MG	C1	33pF ± 10%	400kHz (Murata) CSB400P	C1	470pF ± 10%
	C2	33pF ± 10%		C2	470pF ± 10%
	R	0Ω		R	0Ω
3MHz (Kyocera) KBR3.0MS	C1	47pF ± 10%	400kHz (Kyocera) KBR400B	C1	330pF ± 10%
	C2	47pF ± 10%		C2	330pF ± 10%
	R	0Ω		R	0Ω

Table 1 Constants Guaranteed for Ceramic Resonator Oscillation

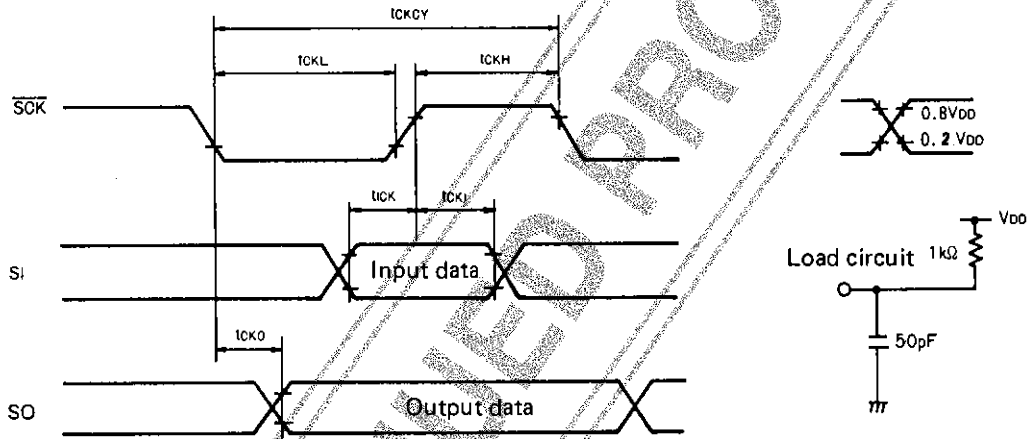


Fig. 6 Serial Input/Output Timing

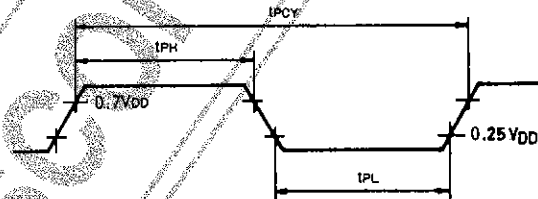


Fig. 7 Pulse Output Timing at Port PE0

The load conditions are the same as in Fig. 6.

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	V _{DD}	Remarks
Ceramic Resonator Option	400 kHz	1/1 (10 μs)	3 to 5.5V	Unusable with 1/3, 1/4 predivider
	800 kHz	1/1 (5 μs)	4 to 5.5V	
		1/3 (15 μs)	4 to 5.5V	
		1/4 (20 μs)	4 to 5.5V	
3 MHz	1/3 (4 μs)	4 to 5.5V	Unusable with 1/1 predivider	
	1/4 (5.33 μs)	4 to 5.5V		
4 MHz	1/3 (3 μs)	4 to 5.5V	Unusable with 1/1 predivider	
	1/4 (4 μs)	4 to 5.5V		
External Clock Option or External Clock Drive by RC OSC Option	200 to 667 kHz	1/1 (20 to 6 μs)	3 to 5.5V	
	600 to 2000 kHz	1/3 (20 to 6 μs)	3 to 5.5V	
	800 to 2667 kHz	1/4 (20 to 6 μs)	3 to 5.5V	
	200 to 1444 kHz	1/1 (20 to 2.77 μs)	4 to 5.5V	
	600 to 4330 kHz	1/3 (20 to 2.77 μs)	4 to 5.5V	
	800 to 4330 kHz	1/4 (20 to 3.70 μs)	4 to 5.5V	
External Clock Drive by ceramic resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option or RC OSC option.			
RC OSC Option	Used with 1/1 predivider, recommended constants (V _{DD} = 4 to 5.5V, V _{DD} = 3 to 5.5V). If used with other than recommended constants, the predivider option, frequency, V _{DD} range must be the same as for the external clock option.			

Table 2 Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown above.)

RC Oscillation Characteristic of the LC6520C, 6522C

Fig. 8 shows the RC oscillation characteristic of the LC6520C, 6522C. For the variation range of RC OSC frequency of the LC6520C, 6522C, the following are guaranteed at the external constants only shown below.

- 1) V_{DD} = 3.0V to 5.5V, T_a = -30°C to +70°C
 External constants C_{ext} = 270 pF, R_{ext} = 15 kohms
 $222 \text{ kHz} \leq f_{\text{mosc}} \leq 609 \text{ kHz}$
- 2) V_{DD} = 4.0V to 5.5V, T_a = -30°C to +70°C
 External constants C_{ext} = 220 pF, R_{ext} = 6.8 kohms
 $515 \text{ kHz} \leq f_{\text{mosc}} \leq 1156 \text{ kHz}$

If any other constants than specified above are used, the range of R_{ext} = 4 kohms to 23 kohms, C_{ext} = 150 pF to 400 pF must be observed. (See Fig. 8.)

Note 8: The oscillation frequency at V_{DD} = 5.0V, T_a = 25°C must be in the range of 350 kHz to 750 kHz.

Note 9: The oscillation frequency at V_{DD} = 4.0V to 5.5V, T_a = -30°C to +70°C and V_{DD} = 3.0V to 5.5V, T_a = -30°C to +70°C must be within the operation clock frequency range. (See Table 2.)

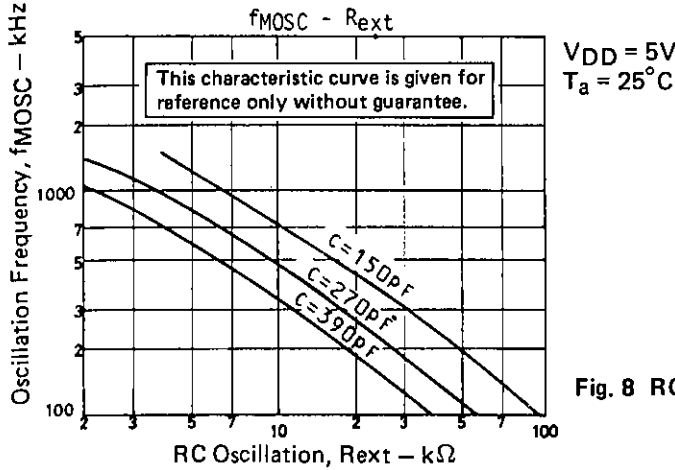


Fig. 8 RC Oscillation Frequency Data (Typ.)

Main Specifications of the LC6520H, 6522H

Absolute Maximum Ratings/Ta = 25°C, VSS = 0V

				unit
Maximum Supply Voltage	VDD max	VDD	-0.3 to +7.0	V
Output Voltage	Vo	OSC2	Allowable up to voltage generated	V
Input Voltage	Vi (1)	OSC1 (Note 1)	-0.3 to VDD+0.3	V
	Vi (2)	TEST, RES	-0.3 to VDD+0.3	V
	Vi (3)	PB0 to 3	-0.3 to +15	V
Input/Output Voltage	VIO (1)	Port of OD type	-0.3 to +15	V
	VIO (2)	Port of PU type	-0.3 to VDD+0.3	V
Peak Output Current	IOP	Input/output port	-2 to +20	mA
Average Output Current	IOA	Input/output port: Per pin over the period of 100 msec.	-2 to +20	mA
	ΣIOA (1)	Total current of PA0 to 3, PC0 to 3, PD0 to 3, and PE0 to 3 (Note 2)	-30 to +140	mA
	ΣIOA (2)	Total current of PF0 to 3, PG0 to 3, and PH0 to 3, PJ0 to 3 (Note 2)	-30 to +140	mA
Allowable Power Dissipation	Pd max (1)	DIP package, Ta = -30 to +70°C	600	mW
	Pd max (2)	QIP package, Ta = -30 to +70°C	400	mW
Operating Frequency	T _{opg}		-30 to +70	°C
Storage Temperature	T _{stg}		-55 to +125	°C

Allowable Operating Conditions/Ta = -30 to +70°C, VSS = 0V, VDD = 4.5 to 5.5V

			min	typ	max	unit
Operating Supply Voltage	VDD	VDD	4.5		5.5	V
Standby Supply Voltage	Vst	VDD: RAM, resister hold (Note 3)	1.8		5.5	V
"H"-Level Input Voltage	VIH (1)	Port of OD type, PB0 to 3: Output Nch Tr OFF	0.7VDD		+13.5	V
	VIH (2)	Port of PU type: Output Nch Tr OFF	0.7VDD		VDD	V
	VIH (3)	SCK, SI, INT: Output Nch Tr OFF	0.8VDD		+13.5	V
	VIH (4)	SCK, SI, INT: Output Nch Tr OFF	0.8VDD		VDD	V
	VIH (5)	RES	0.8VDD		VDD	V
	VIH (6)	OSC1: External clock mode	0.8VDD		VDD	V
"L"-Level Input Voltage	VIL (1)	Port: Output Nch Tr OFF	VSS		0.3VDD	V
	VIL (2)	INT, SCK, SI: Output Nch Tr OFF	VSS		0.25VDD	V
	VIL (3)	OSC1: External clock mode	VSS		0.25VDD	V
	VIL (4)	TEST	VSS		0.3VDD	V
	VIL (5)	RES	VSS		0.25VDD	V
Operating Frequency (Cycle Time)	f _{op} (T _{cycl})			See Table 2.		
			(0.92)		(20)	(μs)

External Clock Conditions (When the external clock option is selected)

Frequency	f _{ext}	OSC1: Fig. 1		See Table 2.	
Pulse Width	t _{extH}	OSC1: Fig. 1	90		ns
	t _{extL}				
Rise/Fall Time	t _{extR}	OSC1: Fig. 1			30 ns
	t _{extF}				

Oscillation Guaranteed Constants
Ceramic Resonator Oscillation

Fig. 2

See Table 1.

Electrical Characteristics/ $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{V}$, $V_{DD} = 4.5$ to 5.5V		min	typ	max	unit		
"H"-Level Input Current	I_{IH} (1)	Port of open drain type, PB0 to 3: Output Nch Tr OFF, Including Nch Tr OFF leakage current, $V_{IN} = 13.5\text{V}$		+5.0	μA		
"L"-Level Input Current	I_{IH} (2)	OSC1: External clock mode, $V_{IN} = V_{DD}$		+1.0	μA		
	I_{IL} (1)	Port of open drain type, PB0 to 3: Output Nch Tr OFF, $V_{IN} = V_{SS}$		-1.0	μA		
	I_{IL} (2)	Port with pull-up resistance: Output Nch Tr OFF, $V_{IN} = V_{SS}$		-1.3	-0.35	mA	
	I_{IL} (3)	RES: $V_{IN} = V_{SS}$		-45	-10	μA	
"H"-Level Output Voltage	V_{OH} (1)	Port with pull-up resistance: $I_{OH} = -50 \mu\text{A}$		$V_{DD} - 1.2$	V		
	V_{OH} (2)	Port with pull-up resistance: $I_{OH} = -10 \mu\text{A}$		$V_{DD} - 0.5$	V		
"L"-Level Output Voltage	V_{OL} (1)	Port: $I_{OL} = 10 \text{mA}$		1.5	V		
	V_{OL} (2)	Port: $I_{OL} = 1 \text{mA}$, When I_{OL} of each port is 1 mA or less.		0.5	V		
Hysteresis Voltage	V_{Hys}	RES, INT, SCK, SI, OSC1 of Schmitt type (Note 6)		$0.1V_{DD}$	V		
Current Dissipation							
Ceramic Resonator Oscillation	I_{DDOP} (1)	V_{DD} : Fig. 2, 4MHz, Operating mode, Output Nch Tr OFF, Port = V_{DD}		5	10	mA	
External Clock	I_{DDOP} (2)	V_{DD} : 200 kHz to 4330 kHz, Operating mode, Output Nch Tr OFF, Port = V_{DD}		5	10	mA	
Standby Mode	I_{DDST}	V_{DD} : $V_{DD} = 5.5\text{V}$ (Output Nch Tr OFF, Port = V_{DD})		0.05	10	μA	
		V_{DD} : $V_{DD} = 3\text{V}$ (Port = V_{DD})		0.025	5	μA	
Oscillation Characteristics							
Ceramic Resonator Oscillation							
Oscillation Frequency	f_{CFOSC} (Note 4)	OSC1, OSC2: Fig. 2, $f_o = 4 \text{MHz}$		3920	4000	4080	kHz
Oscillation Stabilizing Period	t_{CFS}	Fig. 3 $f_o = 4 \text{MHz}$				10	ms
Pull-up Resistance							
I/O Port Pull-up Resistance	R_{pp}	Port of PU type: $V_{DD} = 5\text{V}$			14		k Ω
External Reset Characteristics							
"H"-Level Threshold	V_{tH}			$0.5V_{DD}$		$0.8V_{DD}$	V
"L"-Level Threshold	V_{tL}			$0.25V_{DD}$		$0.5V_{DD}$	V
Reset Time	T_{RST}			See Fig. 4.			
Pin Capacitance	CP	$f = 1 \text{MHz}$, Other than pins to be tested, $V_{IN} = V_{SS}$			10		pF
Serial Clock							
Input Clock Cycle Time	t_{CKCY} (1)	$\overline{\text{SCK}}$: Fig. 5		3.0			μs
Output Clock Cycle Time	t_{CKOY} (2)	SCK : ($T_{CYC} = 4 \times$ System clock period), Fig. 5			$64 \times T_{CYC}$		μs
Input Clock "L"-Level Pulse Width	t_{CKL} (1)	$\overline{\text{SCK}}$: Fig. 5		1.0			μs
Output Clock "L"-Level Pulse Width	t_{CKL} (2)	$\overline{\text{SCK}}$: Fig. 5			$32 \times T_{CYC}$		μs

Continued on next page.

Continued from preceding page.

			min	typ	max	unit
Input Clock "H"-Level Pulse Width	t _{CKH} (1)	\overline{SCK} : Fig. 5	1.0			μs
Output Clock "H"-Level Pulse Width	t _{CKH} (2)	\overline{SCK} : Fig. 5	32 x T _{CYC}			μs
Serial Input Data Setup Time	t _{ICK}	SI: Specified for \uparrow of \overline{SCK} , Fig. 5	0.5			μs
Serial Input Data Hold Time	t _{ICKI}	SI: Specified for \uparrow of \overline{SCK} , Fig. 5	0.5			μs
Serial Output Output Delay Time	t _{CKO}	SO: Specified for \downarrow of \overline{SCK} , Nch OD only: External 1 kohm, external 50 pF, Fig. 5			0.5	μs
Pulse Output Period	t _{PCY}	PE0: T _{CYC} = 4 x System clock period, Nch OD only: External 1 kohm, external 50 pF, Fig. 5	64 x T _{CYC}			μs
"H"-Level Pulse Width	t _{PH}	PE0:	32 x T _{CYC} ± 10%			μs
"L"-Level Pulse Width	t _{PL}	PE0:	32 x T _{CYC} ± 10%			μs

- Note 1:** When oscillated internally under the oscillating conditions in Fig. 2, up to the oscillation amplitude generated is allowable.
- Note 2:** Average over the period of 100 msec.
- Note 3:** Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 (or PA0 to 3) pin must be free from chattering during the HALT instruction execution cycle.
- Note 4:** f_{CFOSC} represents an oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.
- Note 5:** When mounting the QIP version on the board, do not dip it in solder.
- Note 6:** The OSC1 becomes the Schmitt type when the OSC option is the external clock OSC.

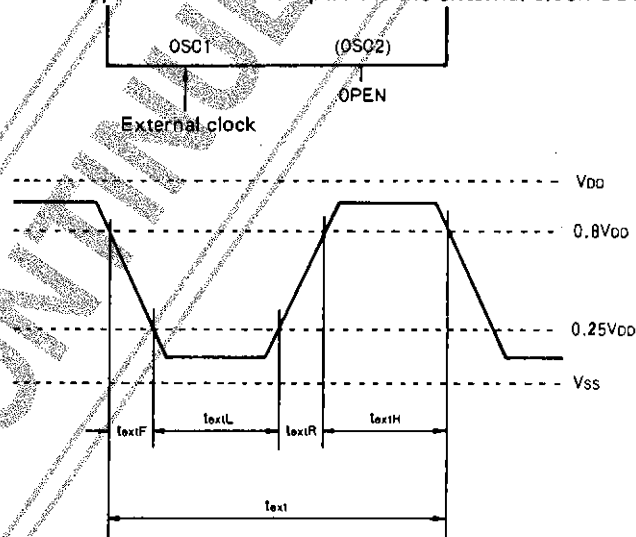


Fig. 1 External Clock Input Waveform

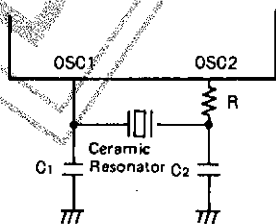


Fig. 2 Ceramic Resonator Oscillation Circuit

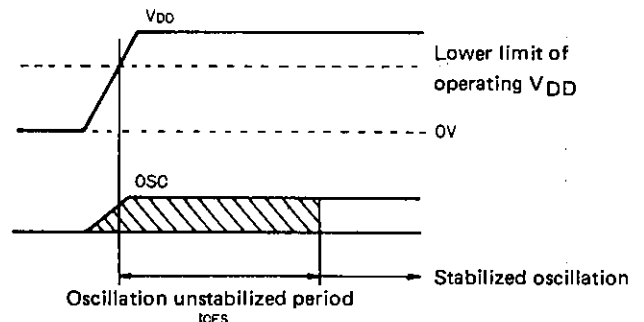


Fig. 3 Oscillation Stabilizing Period

4MHz (Murata) CSA4.00MG	C1	33pF ± 10%
	C2	33pF ± 10%
	R	0Ω
4MHz (Kyocera) KBR4.0MS	C1	33pF ± 10%
	C2	33pF ± 10%
	R	0Ω

Table 1 Constants Guaranteed for Ceramic Resonator Oscillation

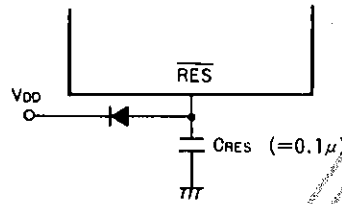


Fig. 4 Reset Circuit

Note 7: When the rise time of the power supply is 0, the reset time becomes 10 ms to 100 ms at $C_{RES} = 0.1 \mu F$. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10 ms or greater.

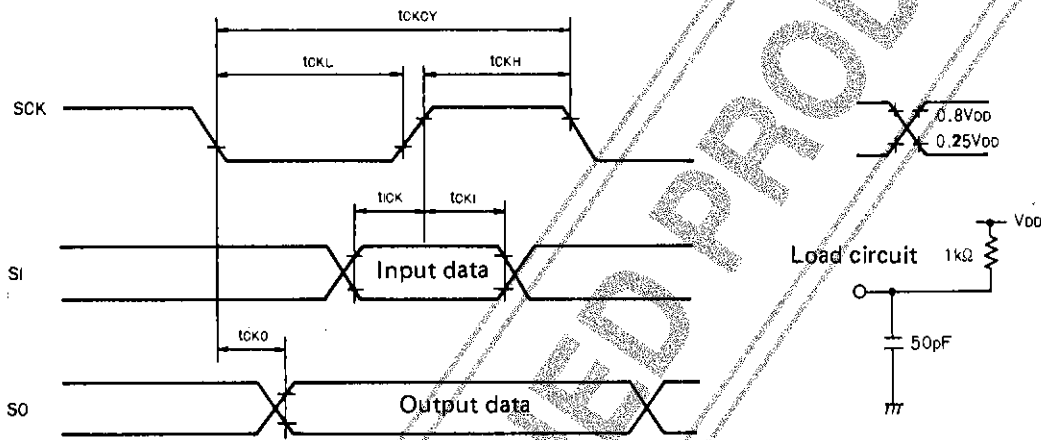


Fig. 5 Serial Input/Output Timing

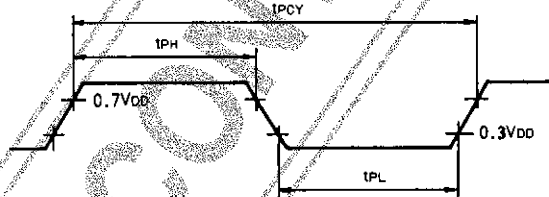


Fig. 6 Pulse Output Timing at Port PE0

The load conditions are the same as in Fig. 5.

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	VDD	Remarks
Ceramic Resonator OSC Option	4 MHz	1/1 (1 μs)	4.5 to 5.5V	
External Clock Option	200 to 4330 kHz	1/1 (20 to 0.92 μs)	4.5 to 5.5V	
External Clock Drive by Ceramic Resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option.			

Table 2 Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown above.)

Notes for Standby Function Application

The LC6520, LC6522 provide the standby function called HALT mode to minimize the current dissipation when the program is in the wait state.

The standby function is controlled by the HALT instruction, PA pin, $\overline{\text{RES}}$ pin, and serial transfer completion signal. A peripheral circuit and program must be so designed as to provide precise control of the standby function. In most applications where the standby function is performed, voltage regulation, instantaneous break of power, and external noise are not negligible. When designing an application circuit and program, whether or not to take some measures must be considered according to the extent to which these factors are allowed. This section mainly describes power failure backup for which the standby function is mostly used. A sample application circuit where the standby function is performed precisely is shown below and notes for circuit design and program design are also given below.

When using the standby function, the application circuit shown below must be used and the notes must be also fully observed.

If any other method than shown in this section is applied, it is necessary to fully check the environmental conditions such as power failure and the actual operation of an application equipment.

1. HALT mode release conditions

1-1. Supplementary description of release by serial transfer completion signal

On completion of serial transfer, the HALT mode is released and the execution of the program starts with an instruction immediately following the HALT instruction. This function can be used to execute the program only when serial transfer occurs, placing the program in the wait state when no serial transfer occurs. This function is effective in reducing the current dissipation or clock noise.

— Notes —

- Release by the serial transfer completion signal is available only when the RC mode is used for system clock generation; and unavailable when the ceramic mode is used.
- On completion of serial transfer, the HALT mode is released unconditionally. In an application, such as capacitor backup application, where the current dissipation must be kept as low as possible during backup and serial transfer by external clock is also used, the HALT mode is released when serial data is transferred externally during backup.

1-2. Summary of HALT release conditions

The HALT mode setting, release conditions are shown in Table 1.

Table 1 HALT mode setting, release conditions

HALT mode setting conditions	HALT mode release conditions
HALT instruction Provided that PA ₃ , (PA ₃ to PA ₀ or PA ₃ is program-selectable) is at high level.	1 Reset (Low level is applied to $\overline{\text{RES}}$.) 2 Low level is applied to PA ₃ , (PA ₃ to PA ₀ or PA ₃ is program-selectable.) 3 Serial transfer completion.

Note) HALT mode release conditions (2), (3) are available only when the RC mode is used for system clock generation; and unavailable when the ceramic mode is used.

2. Proper cares in using standby function

When using the standby function, an application circuit and program must be designed with the following in mind.

- (1) The supply voltage at the standby state must not be less than specified.
- (2) Input timing and conditions of each control signal ($\overline{\text{RES}}$, port A, serial transfer) must be observed at the standby initiate/release state.
- (3) Release operation must not be overlapped at the time of execution of the HALT instruction.

A sample application where the standby function is used for power failure backup is shown below as a concrete method to observe these notes. A sample application circuit, its operation, and notes for program design are given below.

Sample application where the standby function is used for power failure backup

Power failure backup is an application where power failure of the main power source is detected and the HALT instruction is executed to cause the standby state to be entered. The current dissipation is minimized and a backup capacitor is used to retain the contents of the internal registers for a certain period of time. After power is restored, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC). Shown below are sample applications where the program selects or not between power-ON reset and reset after power is restored, notes, measures for instantaneous break of AC power, and notes for serial transfer.

2-1. Sample application 1 where the standby function is used for power failure backup

Shown below is a sample application where the program does not select between power-ON reset and reset after power is restored.

2-1-1. Sample application circuit – (1)

Fig. 2-1 shows a sample application where the standby function is used for power failure backup.

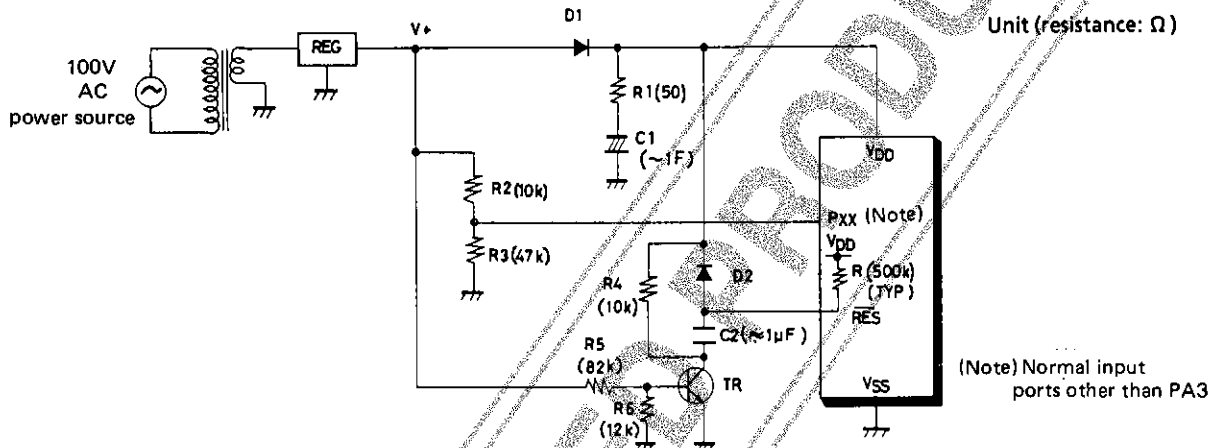


Fig. 2-1. Sample application – (1) where the standby function is used for power failure backup

2-1-2. Operating waveform in sample application circuit – (1)

The operating waveform in the sample application circuit in Fig. 2-1 is shown in Fig. 2-2. The mode is roughly divided as follows: a, Power-ON reset, b, Instantaneous break of main power, c, Return from power failure backup.

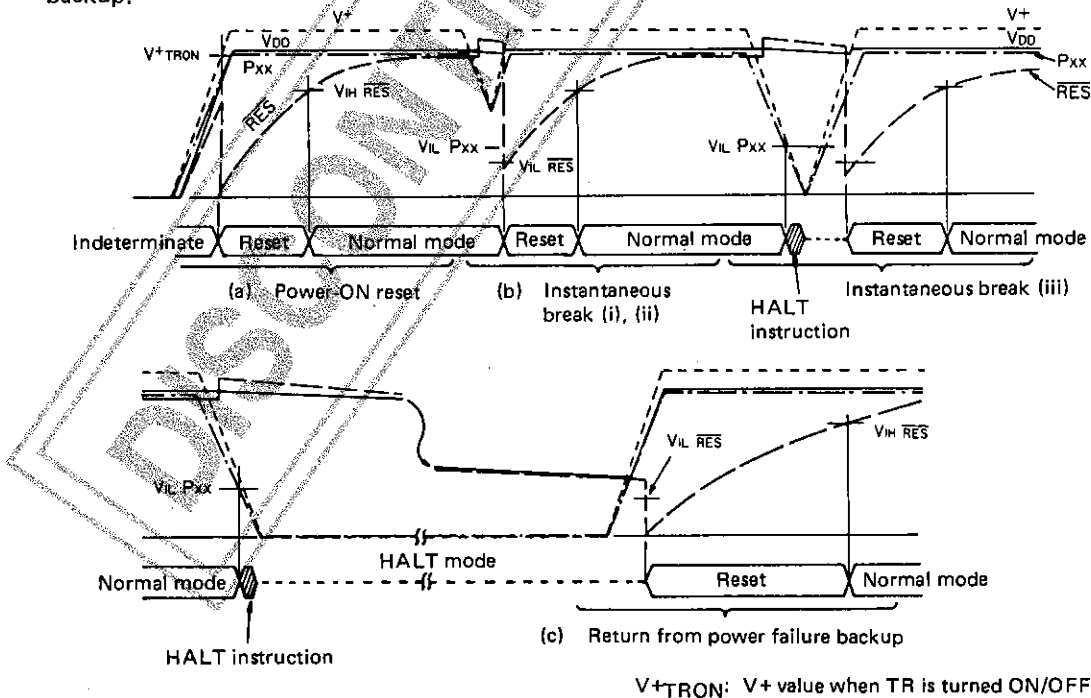


Fig. 2-2. Operating waveforms – (1) in sample application circuit

2-1-3. Operation of sample application circuit — (1)

(a) At the time of power-ON reset

After power rises, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC).

— Note —

This sample application circuit provides an indeterminate region where no reset occurs before the operating VDD range is entered.

(b) At the time of instantaneous break

(i) When the PXX input voltage does not meet V_{IL} (The PXX input level does not get lower than input threshold level V_{IL}) and the RES input voltage only meets V_{IL}:
A reset occurs in the normal mode, providing the same operation as power-ON reset.

(ii) When both of the PXX input voltage and RES input voltage do not meet V_{IL}:
The program continues running in the normal mode.

(iii) When both of the PXX input voltage and RES input voltage meet V_{IL}:
When two pollings do not regard the PXX input voltage as "L" level, the HALT mode is not entered and a reset occurs.

When two pollings regard the PXX input voltage as "L" level, the HALT mode is entered and after power is restored a reset occurs, releasing the standby mode.

(c) At the time of return from power failure backup

After power is restored, a reset occurs, releasing the standby mode.

2-1-4. Notes for design of sample application circuit — (1)

● V₊ rise time and C₂

Make the time constant (C₂, R) of the reset circuit 10 times as long as the V₊ rise time. (R: ON-chip resistor, 500 kohm typ.)

Make the V₊ rise time shorter (up to 20 ms).

● R₁ and C₁

Make the R₁ value as small as possible. Make the C₁ value as large as possible according to the backup time calculated, (Fix the R₁ value so that the C₁ charging current does not exceed the power source capacity.)

● R₂ and R₃

Make the "H"-level input voltage applied to the PXX pin equal to V_{DD}.

● R₄

Fix the time constant of C₂ and C₄ so that C₂ can discharge during the period of time from when V₊ gets lower than V_{+TROM} (TR OFF) at the time of instantaneous break until the PXX input voltage gets lower than V_{IL} (because release by reset is not available after the HALT mode is entered by instantaneous break).

● R₅ and R₆

Make V₊ (V_{BE} ≒ 0.6V is obtained by R₅ and R₆) when the reset circuit works (Tr ON) more than (operating V_{DD} min + V_F of diode D1). Observing this note, make V₊ as low as possible to provide a reset early enough after power-ON.

● Backup time

The normal operation continues with a relatively high current dissipation from when power failure is detected by the PXX until the HALT instruction is executed. Fix the C₁ value so that the standby supply voltage is held during backup time of set + above-mentioned time.

2-1-5. Notes for software design

● Design the program so that port A₀ to A₂ cannot be used for standby release and port A₃ is brought to "H" level at the standby mode.

● Input a standby request to a normal input port other than the PA₃ and check by polling this input port twice.

(Example)

```

:
BP1      AAA      ; 1st polling
RCTL     3        ; Interrupt inhibit
BP1      AAA      ; 2nd polling
HALT     ; Standby
AAA:     :
    
```

2-2. Sample application 2 where the standby function is used for power failure backup

Shown below is a sample application where the program selects between power-ON reset and reset after power is restored.

2-2-1. Sample application circuit – (2) (No instantaneous break in power source)

Fig. 2-3 shows a sample application where the standby function is used for power failure backup.

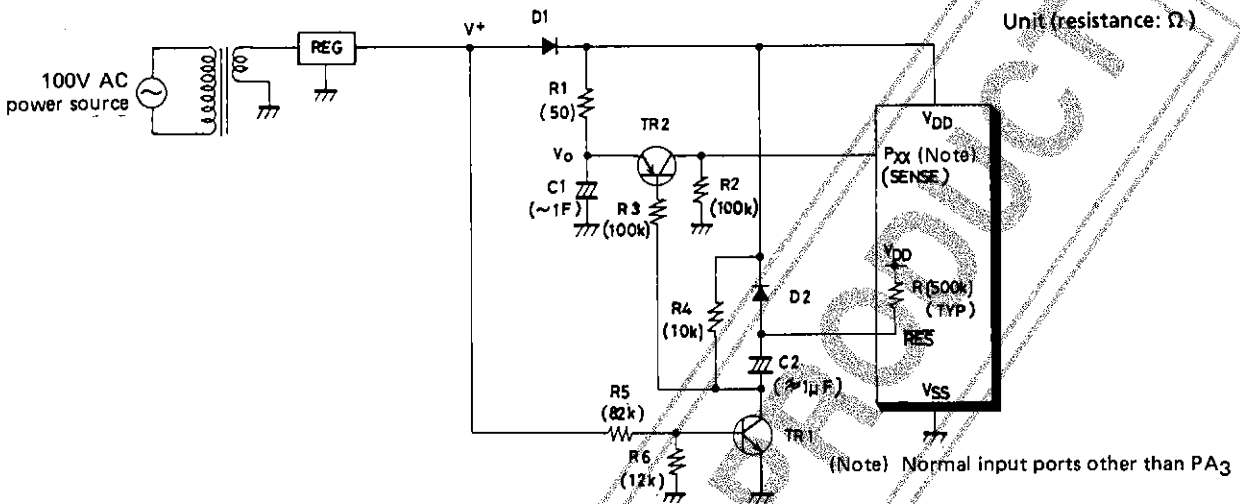


Fig. 2-3 Sample application – (2) where the standby function is used for power failure backup

2-2-2. Operating waveform in sample application circuit – (2)

The operating waveform in the sample application circuit in Fig. 2-3 is shown in Fig. 2-4. The mode is roughly divided as follows: a, Power-ON reset, b. Return from power failure backup.

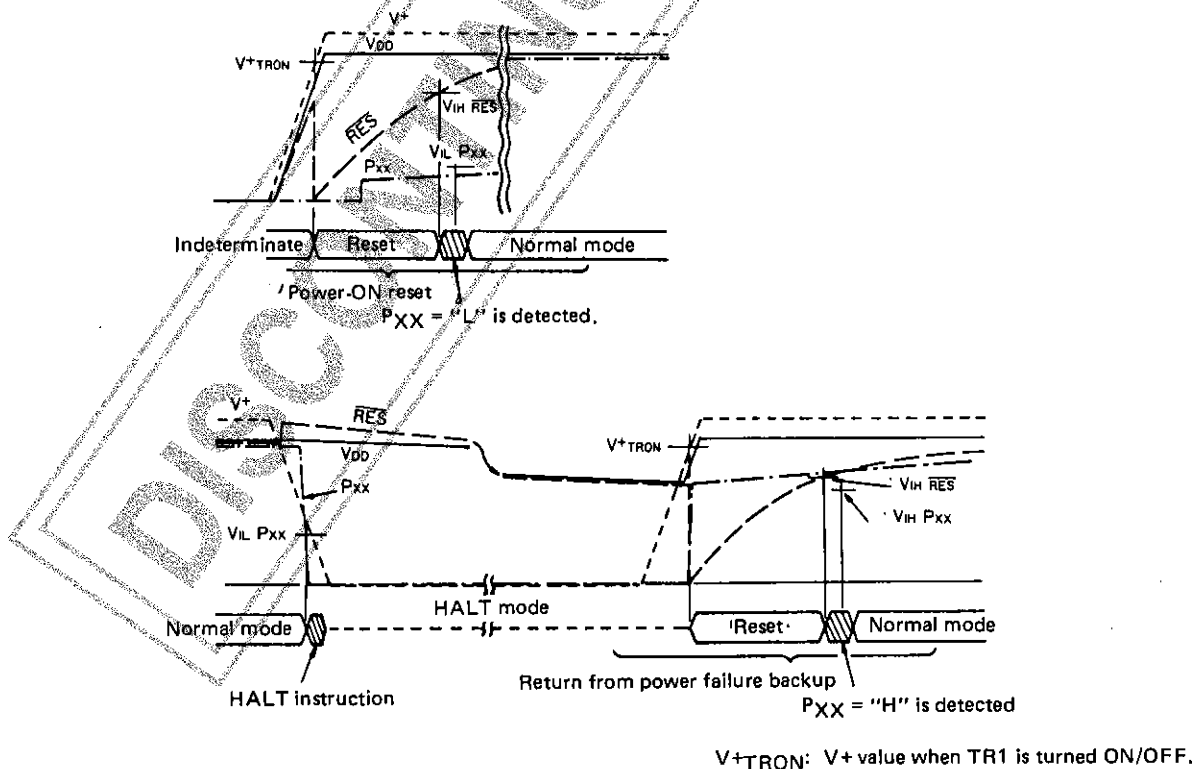


Fig. 2-4. Operating waveform – (2) in sample application circuit

2-2-3. Operation of sample application circuit – (2)

- (a) At the time of power-ON reset
The operation and notes are the same as for sample application circuit – (1), except that after reset release P_{XX} = "L" is program-detected to decide program start after initial reset.
- (b) Standby initiation
When one polling regards the P_{XX} input voltage as "L" level, the HALT mode is entered.
- (c) At the time of return from power failure backup
After power is restored, a reset occurs, releasing the standby mode. After standby release P_{XX} = "H" is program-detected, deciding program start after power is restored.

– Note –

If power is restored after V_{DD} during power failure backup gets lower than V_{IH} on the P_{XX}, P_{XX} = "L" may be program-detected, deciding program start after initial reset.

2-2-4. Notes for design of sample application circuit – (2)

- R₂ and R₃
Fix the R₂ value so that R₂ >> R₁ is yielded and fix the R₃ value so that I_B of TR₂ is limited.
- R₄
There is no severe restriction on the R₄ value, but fix it so that C₂ can discharge quickly.
Other notes are the same as for sample application circuit – (1).

2-2-5. Notes for software design

- Design the program so that port A₀ to A₂ cannot be used for standby release and port A₃ is brought to "H" level.
- Input a standby request to a normal input port other than the PA₃ and check by polling this input port once.

(Example)

```

:
: BP1      AAA      : Polling
: HALT     :         : Standby
AAA:
:
    
```

2-3. Sample application 3 where the standby function is used for power failure backup

2-3-1. Sample application circuit – (3) (There is an instantaneous break in power source.)

Fig. 2-5. shows a sample application where the standby function is used for power failure backup.

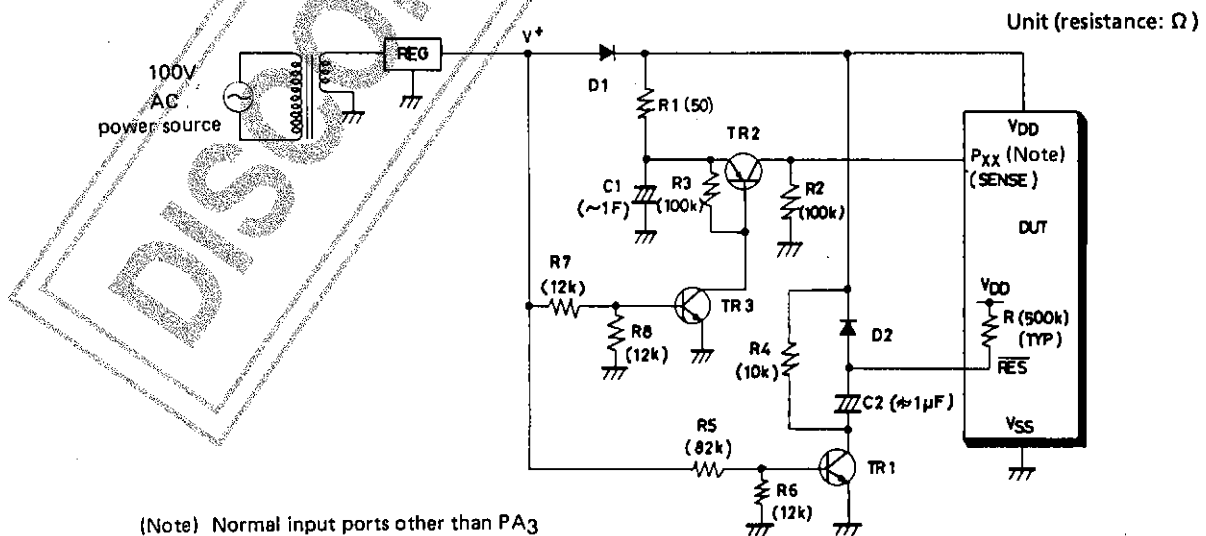


Fig. 2-5 Sample application – (3) where the standby function is used for power failure backup

2-3-2. Operating waveform in sample application circuit – (3)

The operating waveform in the sample application circuit in fig. 2-5 is shown in Fig. 2-6. The mode is roughly divided as follows: a, Power-ON reset, b, Instantaneous break of main power, C, Return from power failure backup.

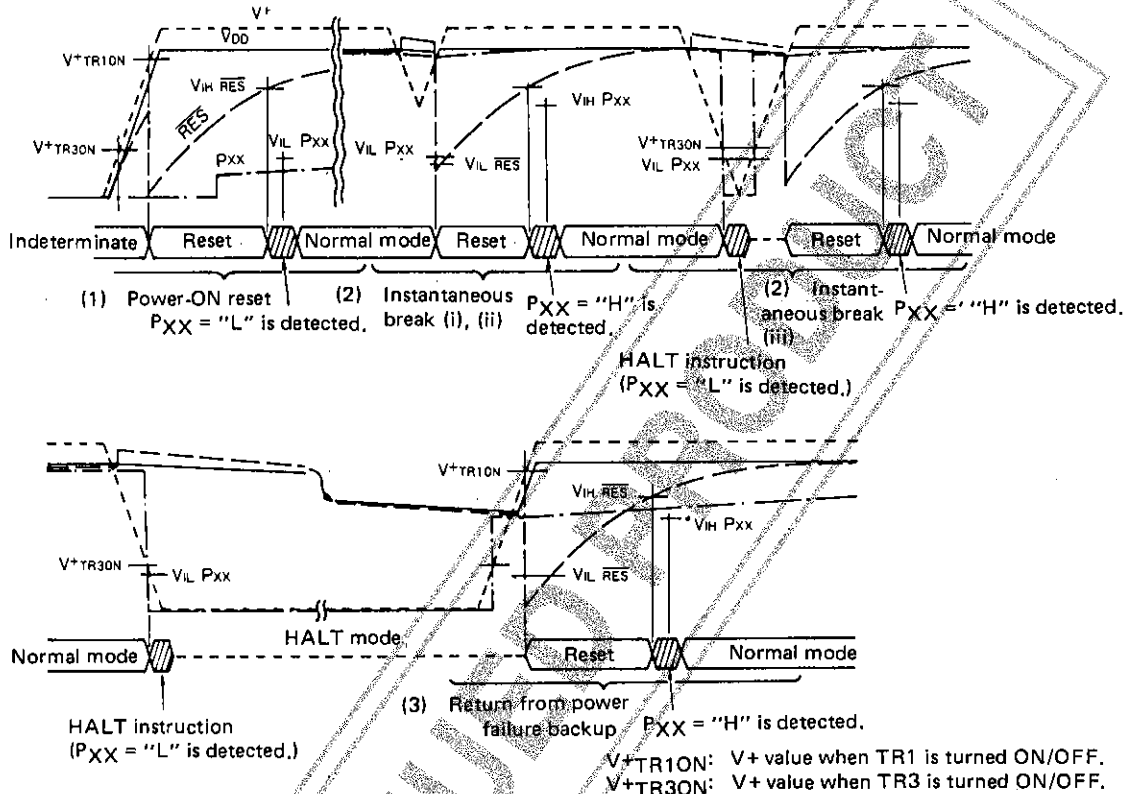


Fig. 2-6 Operating waveform in sample application circuit – (3)

2-3-3. Operation of sample application circuit – (3)

(a) At the time of power-ON reset

The operation and notes are the same as for sample application circuit – (2)

(b) At the time of instantaneous break

(i) When the PXX input voltage does not meet VIL (the PXX input level does not get lower than input threshold level VIL) and the RES input voltage only meets VIL:
A reset occurs in the normal mode. After reset release PXX = "H" is program-detected, deciding program start after instantaneous break.

(ii) When both of the PXX input voltage and RES input voltage do not meet VIL:
The program continues running in the normal mode.

(iii) When both of the PXX input voltage and RES input voltage meet VIL:
When two pollings do not regard the PXX input voltage as "L" level, the HALT mode is not entered and a reset occurs.
When two pollings regard the PXX input voltage as "L" level, the HALT mode is entered and after power is restored, a reset occurs, releasing the standby mode. After standby release PXX = "H" is program-detected, deciding program start after instantaneous break.

(c) At the time of return from power failure backup

The operation and notes are the same as for sample application circuit – (2)

2-3-4. Notes for design of sample application circuit – (3)

- R₃
Bias resistance of TR2
 - R₇ and R₈
Fix the R₇ and R₈ values so that TR3 is turned ON/OFF at approximately 1.5V of V₊.
- Other notes are the same as for sample application circuit – (1)

2-3-5. Notes for software design

Same as for sample application circuit – (1)

2-4. Notes (1) for providing serial transfer

Notes for providing power failure backup and serial transfer

This application assigns top priority to power failure backup. When power failure backup is provided, serial transfer may not be provided normally.

- (1) When the internal clock is used for the serial clock:
Execute the serial transfer start instruction immediately before executing the HALT instruction. If this is done during serial transfer, the power failure backup mode is entered without normal transfer.
- (2) When the external clock is used for the serial clock:
When power failure is detected, it is most prioritized that the HALT mode is entered, providing power failure backup. It is necessary to design an application system where no release signal by serial transfer completion is inputted to the HALT instruction executing cycle and no release signal is inputted during backup.

2-5. Notes (2) for providing serial transfer

Notes for providing HALT and serial transfer for program standby without power failure backup

This application assigns top priority to serial transfer. The following notes for system design must be observed.

- (1) When the internal clock is used for the serial clock:
Transfer starts when it is ready on both sides. When transfer is not ready on the other side, the HALT instruction is executed to reduce the current dissipation. When transfer is ready, the HALT release signal (RES, PA) causes return from the standby mode, starting serial transfer.
- (2) When the external clock is used for the serial clock:
Synchronization must be provided between microcomputers to prevent the HALT instruction and HALT release signal (RSIOEND) from overlapping. When transfer is ready, the serial transfer start instruction is executed and the program is placed in the wait state. The other side adjusts time so that no overlap occurs between the HALT instruction and transfer completion and starts serial transfer. On completion of transfer, the HALT mode is released and the program is executed with an instruction immediately following the HALT instruction.

LC6520, LC6522 INSTRUCTION SET

Symbol Description

AC	: Accumulator	M(DP)	: Memory addressed by DP	(), []	: Contents
ACt	: Accumulator bit t	P(DP _L)	: Input/output port addressed by DP _L	-	: Transfer and direction
CF	: Carry flag	PC	: Program counter	+	: Addition
CTL	: Control register	STACK	: Stack register	-	: Subtraction
DP	: Data pointer	TM	: Timer	∧	: AND
E	: E register	TMF	: Timer (internal) interrupt request flag	∨	: OR
EXTF	: External interrupt request flag	At, Ma, La	: Working register	⊖	: Exclusive OR
Fn	: Flag bit n	ZF	: Zero flag =		
M	: Memory				

Instruction group	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks													
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀																			
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	The AC contents are cleared.	ZF	* 1												
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	The CF contents are cleared.	CF													
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	The CF is set.	CF													
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← \overline{AC}	The AC contents are complemented.	ZF													
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	The AC contents are incremented +1.	ZF CF													
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) - 1	The AC contents are decremented -1.	ZF CF													
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC ₀ ← (CF), AC _{n+1} ← (AC _n), CF ← (AC ₃)	The AC contents are shifted left through the CF.	ZF CF													
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	The AC contents are transferred to the E.														
XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ↔ (E)	The AC contents and the E contents are exchanged.															
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← (M(DP)) + 1	The M(DP) contents are incremented +1.	ZF CF													
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← (M(DP)) - 1	The M(DP) contents are decremented -1.	ZF CF													
	SMB bit	Set M data bit	0 0 0 0	1 0 B ₁ B ₀	1	1	M(DP, B ₁ B ₀) ← 1	A single bit of the M(DP) specified with B ₁ B ₀ is set.														
	RMB bit	Reset M data bit	0 0 1 0	1 0 B ₁ B ₀	1	1	M(DP, B ₁ B ₀) ← 0	A single bit of the M(DP) specified with B ₁ B ₀ is reset.	ZF													
Arithmetic operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP))	Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF													
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP)) + (CF)	Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF													
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	6 is added to the AC contents.	ZF													
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	10 is added to the AC contents.	ZF													
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC.	ZF													
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ (M(DP))	The AC contents and the M(DP) contents are ANDed and the result is stored in the AC.	ZF													
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	The AC contents and the M(DP) contents are ORed and the result is stored in the AC.	ZF													
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	(M(DP)) + (AC) + 1	The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset. <table border="1" style="margin-left: 20px;"> <tr><th>Comparison result</th><th>CF</th><th>ZF</th></tr> <tr><td>(M(DP)) > (AC)</td><td>0</td><td>0</td></tr> <tr><td>(M(DP)) = (AC)</td><td>1</td><td>1</td></tr> <tr><td>(M(DP)) < (AC)</td><td>1</td><td>0</td></tr> </table>	Comparison result	CF	ZF	(M(DP)) > (AC)	0	0	(M(DP)) = (AC)	1	1	(M(DP)) < (AC)	1	0	ZF CF	
	Comparison result	CF	ZF																			
	(M(DP)) > (AC)	0	0																			
(M(DP)) = (AC)	1	1																				
(M(DP)) < (AC)	1	0																				
CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 1 3 1 2 1 1 1 0	2	2	I ₃ I ₂ I ₁ I ₀ + (AC) + 1	The AC contents and the immediate data I ₃ I ₂ I ₁ I ₀ are compared and the ZF and CF are set/reset. <table border="1" style="margin-left: 20px;"> <tr><th>Comparison result</th><th>CF</th><th>ZF</th></tr> <tr><td>I₃I₂I₁I₀ > (AC)</td><td>0</td><td>0</td></tr> <tr><td>I₃I₂I₁I₀ = (AC)</td><td>1</td><td>1</td></tr> <tr><td>I₃I₂I₁I₀ < (AC)</td><td>1</td><td>0</td></tr> </table>	Comparison result	CF	ZF	I ₃ I ₂ I ₁ I ₀ > (AC)	0	0	I ₃ I ₂ I ₁ I ₀ = (AC)	1	1	I ₃ I ₂ I ₁ I ₀ < (AC)	1	0	ZF CF		
Comparison result	CF	ZF																				
I ₃ I ₂ I ₁ I ₀ > (AC)	0	0																				
I ₃ I ₂ I ₁ I ₀ = (AC)	1	1																				
I ₃ I ₂ I ₁ I ₀ < (AC)	1	0																				
CLI data	Compare DP _L with immediate data	0 0 1 0 0 0 0 1	1 1 0 0 1 3 1 2 1 1 1 0	2	2	(DP _L) ∨ I ₃ I ₂ I ₁ I ₀	The DP _L contents and the immediate data I ₃ I ₂ I ₁ I ₀ are compared.	ZF														
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	1 3 1 2 1 1 1 0	1	1	AC ← I ₃ I ₂ I ₁ I ₀	The immediate data I ₃ I ₂ I ₁ I ₀ is loaded in the AC.	ZF	* 1												
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)	The AC contents are stored in the M(DP).														
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← (M(DP))	The M(DP) contents are loaded in the AC.	ZF													
	XM data	Exchange AC with M, then modify DP _H with immediate data	1 0 1 0	0 M ₂ M ₁ M ₀	1	2	(AC) ↔ (M(DP)) DP _H ← (DP _H) ∨ 0 M ₂ M ₁ M ₀	The AC contents and the M(DP) contents are exchanged and then the DP _H contents are modified with the contents of (DP _H) ∨ 0 M ₂ M ₁ M ₀ .	ZF	The ZF is set/reset according to the result of (DP _H) ∨ 0 M ₂ M ₁ M ₀ .												
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ↔ (M(DP))	The AC contents and the M(DP) contents are exchanged.	ZF	The ZF is set/reset according to the DP _H contents at the time of instruction execution.												
	XI	Exchange AC with M, then increment DP _L	1 1 1 1	1 1 1 0	1	2	(AC) ↔ (M(DP)) DP _L ← (DP _L) + 1	The AC contents and the M(DP) contents are exchanged and then the DP _L contents are incremented +1.	ZF	The ZF is set/reset according to the result of (DP _L + 1).												
	XD	Exchange AC with M, then decrement DP _L	1 1 1 1	1 1 1 1	1	2	(AC) ↔ (M(DP)) DP _L ← (DP _L) - 1	The AC contents and the M(DP) contents are exchanged and then the DP _L contents are decremented -1.	ZF	The ZF is set/reset according to the result of (DP _L - 1).												
RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E ← ROM (PCh, E, AC)	The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.															

LC6520C, 6520H, 6522C, 6522H

Instruction group	Mnemonic	Instruction code				Bytes	Cycles	Function	Description	Status flag affected	Remarks
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀								
Data pointer manipulation instructions	LDZ data	1 0 0 0	13 12 11 10	1	1	DP _H ← 0 DP _L ← 13 12 11 10	The DP _H and DP _L are loaded with 0 and the immediate data 13 12 11 10 respectively.				
	LHI data	0 1 0 0	13 12 11 10	1	1	DP _H ← 13 12 11 10	The DP _H is loaded with the immediate data 13 12 11 10.				
	IND	1 1 1 0	1 1 1 0	1	1	DP _L ← (DP _L) + 1	The DP _L contents are incremented +1.	ZF			
	DED	1 1 1 0	1 1 1 1	1	1	DP _L ← (DP _L) - 1	The DP _L contents are decremented -1.	ZF			
	TAL	1 1 1 1	0 1 1 1	1	1	DP _L ← (AC)	The AC contents are transferred to the DP _L .				
	TLA	1 1 1 0	1 0 0 1	1	1	AC ← (DP _L)	The DP _L contents are transferred to the AC.	ZF			
Working register manipulation instructions	XAH	0 0 1 0	0 0 1 1	1	1	(AC) ↔ (DP _H)	The AC contents and the DP _H contents are exchanged.				
	XAt		11 10								
	XAO	1 1 1 0	0 0 0 0	1	1	(AC) ↔ (A0)	The AC contents and the contents of working register A ₀ are exchanged. A ₀ is assigned one of A ₀ , A ₁ , A ₂ , A ₃ according to t ₁₀ .				
	XA1	1 1 1 0	0 1 0 0	1	1	(AC) ↔ (A1)					
	XA2	1 1 1 0	1 0 0 0	1	1	(AC) ↔ (A2)					
	XA3	1 1 1 0	1 1 0 0	1	1	(AC) ↔ (A3)					
Working register manipulation instructions	XHa		a								
	XHO	1 1 1 1	1 0 0 0	1	1	(DP _H) ↔ (H0)	The DP _H contents and the contents of working register H ₀ are exchanged. H ₀ is assigned either of H0 or H1 according to a.				
	XH1	1 1 1 1	1 1 0 0	1	1	(DP _H) ↔ (H1)					
Working register manipulation instructions	XLs		s								
	XLO	1 1 1 1	0 0 0 0	1	1	(DP _L) ↔ (L0)	The DP _L contents and the contents of working register L ₀ are exchanged. L ₀ is assigned either of L0 or L1 according to s.				
	XL1	1 1 1 1	0 1 0 0	1	1	(DP _L) ↔ (L1)					
Flag manipulation instructions	SFB flag	0 1 0 1	B ₃ B ₂ B ₁ B ₀	1	1	F _n ← 1	The flag specified with B ₃ B ₂ B ₁ B ₀ is set.				
	RFB flag	0 0 0 1	B ₃ B ₂ B ₁ B ₀	1	1	F _n ← 0	The flag specified with B ₃ B ₂ B ₁ B ₀ is reset.	ZF	The flags are divided into 4 groups of F ₀ to F ₃ , F ₄ to F ₇ , F ₈ to F ₁₁ , F ₁₂ to F ₁₅ . The ZF is set/reset according to the 4 bits including a single bit specified with the immediate data B ₃ B ₂ B ₁ B ₀ .		
Jump/subroutine instructions	JMP addr	0 1 1 0	1 P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄	2	2	PC ₁₁ ← PC ₁₁ (or PC ₁₁) P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₄ P ₃ P ₂ P ₁ P ₀	A jump to the address specified with the PC ₁₁ (or PC ₁₁) and immediate data P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ occurs.		If the BANK and JMP instructions are executed consecutively, PC ₁₁ → PC ₁₁ .		
	JPEA	1 1 1 1	1 0 1 0	1	1	PC ₇ ← (E, AC)	A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.				
	CZP addr	1 0 1 1	P ₃ P ₂ P ₁ P ₀	1	1	STACK ← (PC) + 1 PC ₁₁ ← 6, PC ₁ ← 0 PC ₅ ← 2 → P ₃ P ₂ P ₁ P ₀	A subroutine in page 0 of bank 0 is called.				
	CAL addr	1 0 1 0	1 P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄	2	2	STACK ← (PC) + 2 PC ₁ ← 0 → OP ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀	A subroutine in bank 0 is called.				
	RT	0 1 1 0	0 0 1 0	1	1	PC ← (STACK)	A return from a subroutine occurs.				
	RTI	0 0 1 0	0 0 1 0	1	1	PC ← (STACK) CF ZF ← CSF, ZSF	A return from an interrupt service routine occurs.	ZF CF			
	BANK	1 1 1 1	1 1 0 1	1	1	PC ₁₁ ← (PC ₁₁)	The bank is changed.		Effective only when used immediately before the JMP instruction.		
Branch instructions	BA _t addr	0 1 1 1	0 0 1 1 1 0	2	2	PC ₇ ← 0 → P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if AC ₁ = 1	If a single bit of the AC specified with the immediate data t ₁₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.		
	BNAt addr	0 0 1 1	0 0 1 1 1 0	2	2	PC ₇ ← 0 → P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if AC ₁ = 0	If a single bit of the AC specified with the immediate data t ₁₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.		
	BMt addr	0 1 1 1	0 1 1 1 1 0	2	2	PC ₇ ← 0 → P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (M(DP, t ₁₀)) = 1	If a single bit of the M(DP) specified with the immediate data t ₁₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.		
	BNMt addr	0 0 1 1	0 1 1 1 1 0	2	2	PC ₇ ← 0 → P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (M(DP, t ₁₀)) = 0	If a single bit of the M(DP) specified with the immediate data t ₁₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.		
	BP _t addr	0 1 1 1	1 0 1 1 1 0	2	2	PC ₇ ← 0 → P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (P(DP, t ₁₀)) = 1	If a single bit of port P(DP) specified with the immediate data t ₁₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BP0 to BP3 according to the value of t.		
	BNP _t addr	0 0 1 1	1 0 1 1 1 0	2	2	PC ₇ ← 0 → P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (P(DP, t ₁₀)) = 0	If a single bit of port P(DP) specified with the immediate data t ₁₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.		
	BTM addr	0 1 1 1	1 1 0 0 0	2	2	PC ₇ ← 0 → P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if TMF = 1 then TMF ← 0	If the TMF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The TMF is reset.	TMF			

LC6520C, 6520H, 6522C, 6522H

Instruction group	Mnemonic	Instruction code		Bytes	Cycles	Function	Description ¹	Status flag affected	Remarks	
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀							
Branch instructions	BNT addr	Branch on no timer	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 0 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The TMF is reset.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if EXTF = 1 then EXTF ← 0	If the EXTF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The EXTF is reset.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if EXTF = 0 then EXTF ← 0	If the EXTF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs. The EXTF is reset.	EXTF	
	BC addr	Branch on CF	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 1 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if CF = 1	If the CF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 1 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if CF = 0	If the CF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 P ₇ P ₆ P ₅ P ₄	1 1 1 0 P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if ZF = 0	If the ZF is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		
	BF _n addr	Branch on flag bit	1 1 0 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if F _n = 1	If the flag bit of the 16 flags specified with the immediate data n ₃ n ₂ n ₁ n ₀ is 1, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BF0 to BF15 according to the value of n.
	BNF _n addr	Branch on no flag bit	1 0 0 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC ₇₋₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if F _n = 0	If the flag bit of the 16 flags specified with the immediate data n ₃ n ₂ n ₁ n ₀ is 0, a branch to the address specified with the immediate data P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ within the same page occurs.		Mnemonic is BN0 to BN15 according to the value of n.
Input/Output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← P(IDP _L)	Port P(IDP _L) contents are loaded in the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(IDP _L) ← AC	The AC contents are outputted to port P(IDP _L).		
	SPB bit	Set port bit	0 0 0 0	0 1 B ₁ B ₀	1	2	P(IDP _L) B ₁ B ₀ ← 1	A single bit in port P(IDP _L) specified with the immediate data B ₁ B ₀ is set.		When this instruction is executed, the E contents are destroyed.
	RPB bit	Reset port bit	0 0 1 0	0 1 B ₁ B ₀	1	2	P(IDP _L) B ₁ B ₀ ← 0	A single bit in port P(IDP _L) specified with the immediate data B ₁ B ₀ is reset.	ZF	When this instruction is executed, the E contents are destroyed.
Other instructions	SCTL bit	Set control register bit(S)	0 0 1 0 1 0 0 0	1 1 0 0 B ₃ B ₂ B ₁ B ₀	2	2	CTL ← (CTL) ∨ B ₃ B ₂ B ₁ B ₀	The bits of the control register specified with the immediate data B ₃ B ₂ B ₁ B ₀ are set.		
	RCTL bit	Reset control register bit(S)	0 0 1 0 1 0 0 0	1 1 0 0 B ₃ B ₂ B ₁ B ₀	2	2	CTL ← (CTL) ∧ B ₃ B ₂ B ₁ B ₀	The bits of the control register specified with the immediate data B ₃ B ₂ B ₁ B ₀ are reset.	ZF	
	WTTM	Write timer	1 1 1 1	0 0 1 1	1	1	TM ← (E), (AC) TMF ← 0	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	All operations stop.		Only when all pins of port PA are set at L stop.
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

*1 If the CLA instruction is used consecutively in such a manner as CLA, CLA, ----, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.

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