

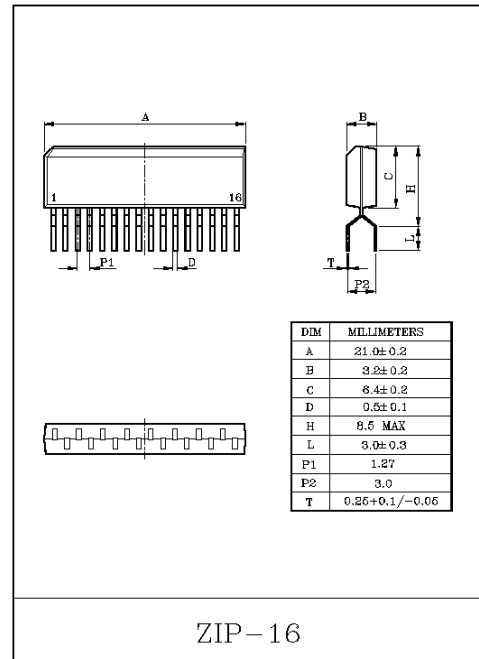
FM MPX SYSTEM FOR CAR ETR

KIA6030Z having the function against noise during the electric field is weak and the pilot canceling. Function is an IC for PLL FM stereo multiplex in which VCO is made adjustment-free.

- Separation Control (SPC)
- High Cut Control (HCC)
- High Blend Control (HBC)
- Pilot Cancel
- VCO Stop
- Forced Monaural

FEATURES

- Adjustment-free type VCO is adopted.
- Since separation control (SPC) and high cut control (HCC) are independent of each other, high blend control (HBC) can also be realized.
- Through paired application of noise canceler IC KIA6010SN multi-path noise can be reduced.
- With this paired application unfavorable influence caused by the pilot signal can be reduced. (Beat distortion etc.).
- Low Distortion Ratio. THD=0.04% STEREO at $V_{IN}=400mV_{rms}(Typ.)$.
- Operation power supply range : $V_{opr}=7\sim 16V$ ($T_a=25^{\circ}C$).



MAXIMUM RATINGS ($T_a=25^{\circ}C$)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D	750	mW
Operating Temperature	T_{opr}	-30~85	$^{\circ}C$
Storage Temperature	T_{stg}	-55~150	$^{\circ}C$
Stereo Lamp Driving Current	I_{LAMP}	30	mA

Note : Derated above $25^{\circ}C$ in the Proportion of $6mW/^{\circ}C$ for KIA6030Z

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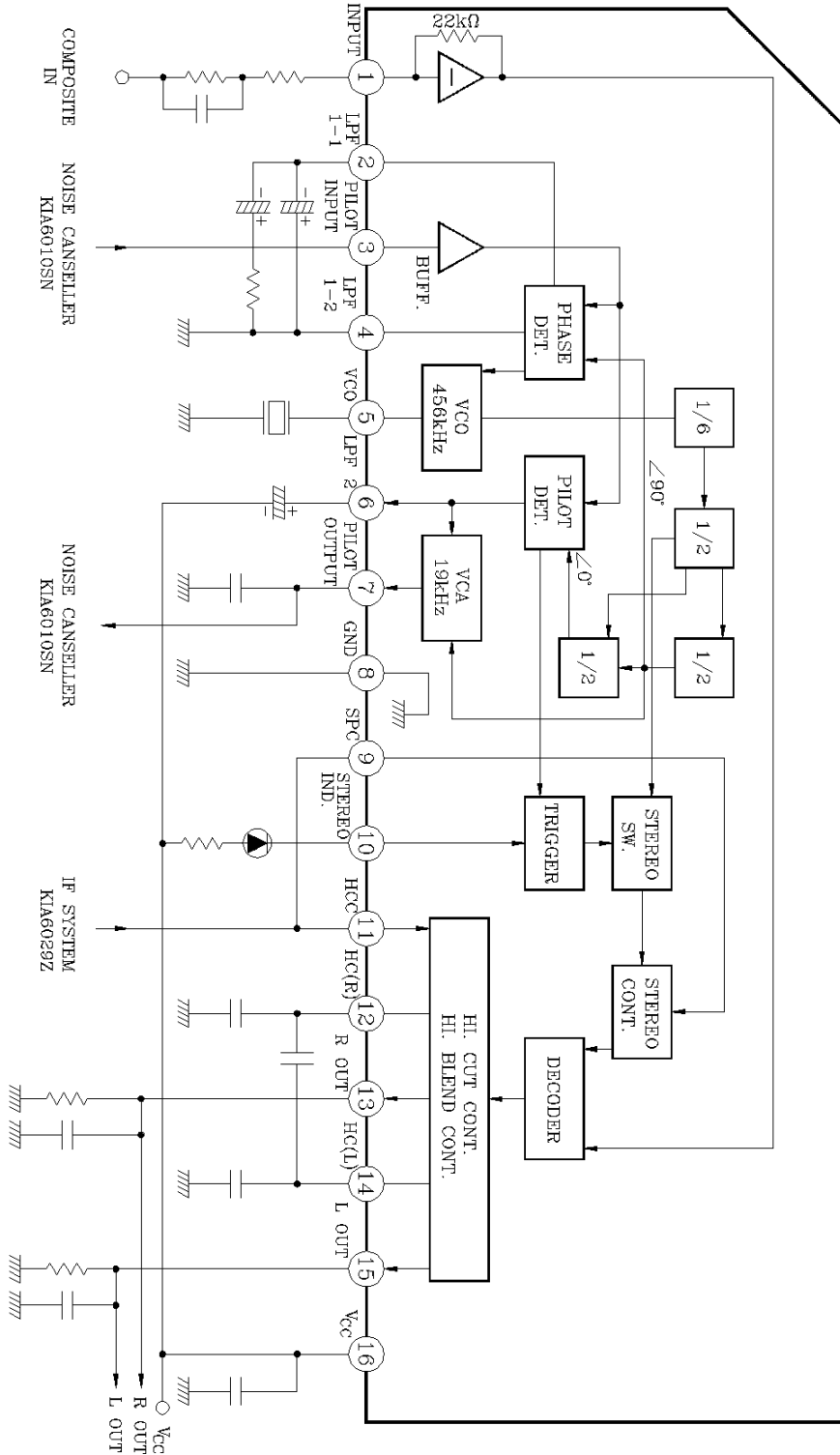
ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, $V_{CC1}=8.5V$, $V_{IN}(\text{mono})=400mV_{rms}$, $f_m=1kHz$,
 $V_{SPC}=2.4V$, $V_{HCC}=1.5V$, $SW1=a$, $SW2=off$, $SW3=a$, $SW5=a$, $T_a=25^\circ C$)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT	
Quiescent Current	I_{CCQ}	$V_{IN}=0$		-	17	25	mA	
Allowable Composite Input	$V_{IN}(\text{stereo})_{max}$	$\frac{L+R}{P} = 9$, THD=1%		700	1000	-	mV_{rms}	
Separation	Sep	L only Mode. (SW4=a→b) R only Mode. (SW4=b→a)	$f_m=1kHz$ $SW_1=b$	40	60	-	dB	
Stereo Distortion Factor	THD	$L+R=360mV_{rms}$ $P=40mV_{rms}$	$f_m=1kHz$	-	0.04	0.3	%	
Monaural Distortion Factor	THD(mono)			-	0.04	0.3		
Voltage Gain	GV			-3	-0.5	0	dB	
Channel Balance	C.B	$SW_3=a \rightarrow b$		-1.5	0	1.5		
Signal to Noise Ratio at Stereo	S/N (stereo)	$L+R=360mV_{rms}$, $P=40mV_{rms}$		74	82	-		
SPC Attenuation Amount	S.ATT1	$L-R=360mV_{rms}$ $P=40mV_{rms}$	$V_{SPC}=1.3V$	2	5	8		
	S.ATT2		$V_{SPC}=0.3V$	37	43	-		
HCC Attenuation Amount	H.ATT1	$f_m=10kHz$	$V_{HCC}=0.7V$	2	4	6		
	H.ATT2		$V_{HCC}=0.3V$	8	11	14		
Pilot Cancel Amount	P.ATT			-	20	-		
Lamp Sensitivity	$V_L(\text{on})$	Turn on P only		5.3	9	15		mV_{rms}
Stereo Current	I_S	$SW_5=b$, $I_S = \frac{V_S}{1k}$ Sep=25dB (L only mod.)		1.2	-	-		mA
Lamp Sensitivity of Hysteresis	V_H			-	3	6	dB	
SCA Rejection Ratio	SCA Rej			-	75	-	dB	
Carrier Leak	CL	$L+R=360mV_{rms}$ $P=40mV_{rms}$, $SW_3=b$	$f=19kHz$	-	43	-	dB	
			$f=38kHz$	-	75	-		

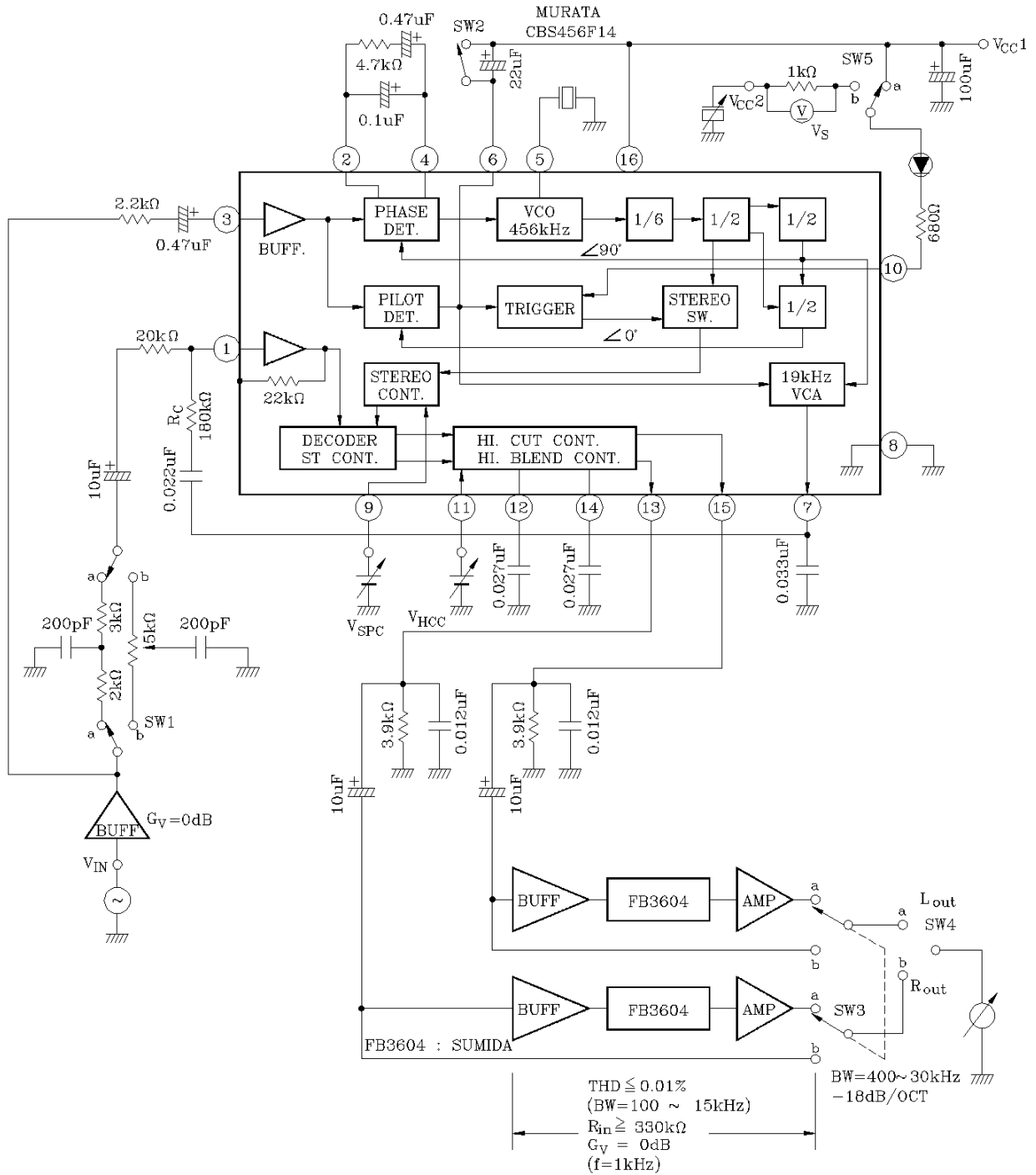
KIA6030Z

BLOCK DIAGRAM



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TEST CIRCUIT



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BUILT-IN FUNCTION

1. METHOD FOR FORCIBLE MONAURAL AT STEREO RECEPTION

In KIA6030Z, in addition to the function of switching the stereo and the monaural receptions according to the existence of the pilot signal, the stereo reception can forcibly be switched to the monaural reception with the three kinds of methods shown in table 1.

Table 1.

NO.	METHODE FOR FORCIBLE MONAURAL	LAMP	PILOT CANCEL	VCO	REFERENCE
1	⑥ Pin V _{CC}	x	x	x	AM
2	⑩ Pin OPEN	x	0	0	ST-MONO SW
3	⑨ Pin GND	0	0	0	

No.1 is effective for using the high cut control of KIA6030Z at AM reception and the connection is made as shown in Fig. 1
 Since ① Pin is an input terminal of the operational amplifier, the impedance is low and AM characteristics is little influenced even if AM input is connected.
 NO.2 is applicable for changing over the stereo and the monaural receptions at FM reception through the panel switch.

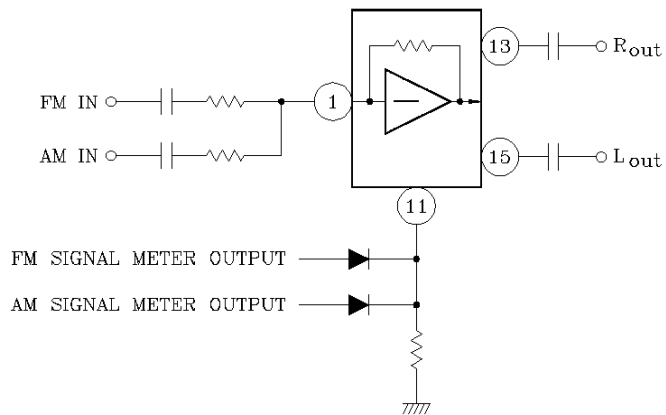


Fig. 1

2. SPC (Separation Control)

For SPC, the circuit which gradually controls the 38kHz amplitude to be used in separation circuit is adopted.

The relation between the control voltage and the separation is different from the conventional one.

As shown in Fig. 2, in the range of 0~20dB of the separation which is effective for the noise reduction, the curve is slow and in the range of 20~50dB, the curve is made sharp and when the separation becomes about 20dB, SPC is made to rapidly grow effective. Therefore, the noise is effectively reduced without sacrificing the separation.

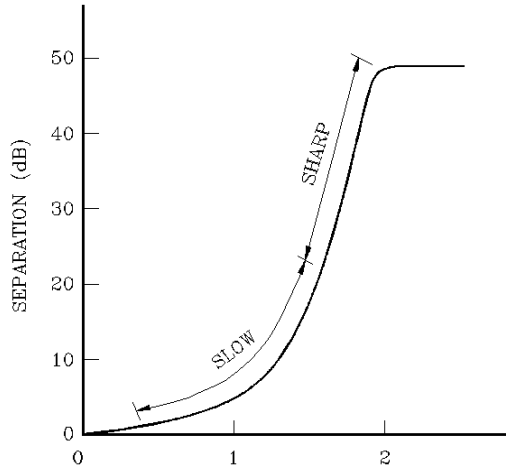


Fig. 2

3. HCC (High Cut Control)

In KIA6030Z composite signal is separated into L and R outputs and HCC is carried out independently on each outputs.

Therefore, this system has following advantages as compared with the conventional system.

(1) Since SPC and HCC can independently be controlled, flexible setting is possible regarding the separation depended on the destination and the frequency characteristics.

(2) Even when HCC is carried out with SPC released, the effect of noise reduction can be obtained. In the conventional system, HCC is applied only to (L+R), and the output of (L-R) modulation circuit is output unchanged, therefore, when HCC is applied, although the treble is attenuated, the reduction effect of the noise produced by (L-R) demodulation can not be expected. Since the phases in the mean and treble signals in (L+R) delay according to HCC, the separation of the mean and treble is inevitable deteriorated. For the cut-off frequency of HCC, refer to the item of HBC described later.

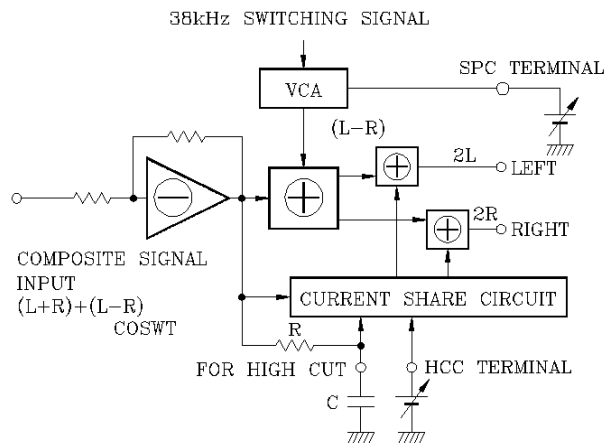


Fig. 3 BLOCK DIAGRAM OF CONVENTIONAL SYSTEM

KIA6030Z

4. HBC (High Blend Control)

By means of connecting the capacitor CHB between HC (High Cut) terminals of ⑫ and ⑭ pins as shown in Fig. 4 to control HCC terminal with DC voltage V_{HCC} such as the signal meter output, HBC is made possible. The signal high-blended with CHB and the fundamental L and R signals are individually input to the current share circuit, and which signal is to be output is determined by V_{HCC} . The cut-off frequency of HCC is obtained through the formula below.

$$f_c = \frac{1}{2\pi CR} \text{ (Hz)} \quad C: CHC \quad R: 2.2k\Omega \text{ (Typ.)}$$

The cut-off frequency of HBC is determined by the following formula.

$$f_c = \frac{1}{4\pi CR} \text{ (Hz)} \quad C: CHB \quad R: 2.2k\Omega \text{ (Typ.)}$$

For blending all bands, short CHB as shown in Fig.4, and for additional high cut, CHC can be reduced to one piece.

In this case, the internal resistance becomes $1.1k\Omega$ (Typ.) and f_c is determined by the following formula. For making f_c equal to that in case of HCC described by the following formula. For making f_c equal to that in case of HCC described above, CHC is necessary to be doubled.

$$f_c = \frac{1}{2\pi CR} \text{ (Hz)} \quad C: CHC \quad R: 1.1k\Omega \text{ (Typ.)}$$

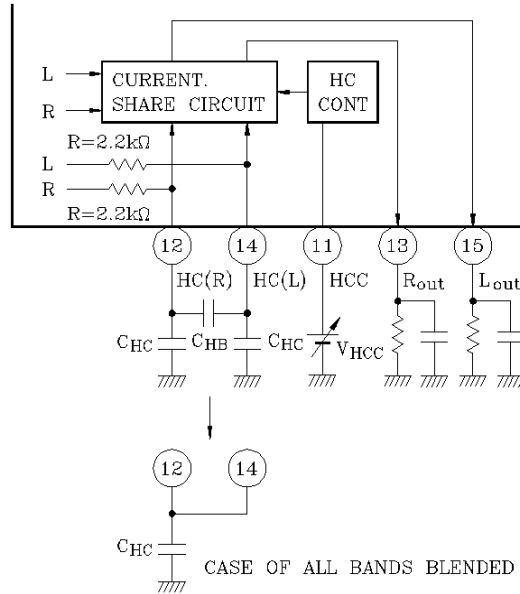


Fig. 4 PRINCIPLE DIAGRAM OF HBC

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5. Pilot Cancel

For pilot cancel, the triangular wave (pilot output V_P), which is made through integrating the current output of the square wave at ⑦ pin, is connected to input ① pin with the resistance R_C .

This pilot output V_P is obtained in proportion to the input pilot level.

Since this pilot output V_P is the input pilot level following type, when the cancel is once set with R_C , the enough pilot cancel amount is obtained even if the modulation degree is varied at the broadcasting station.

For using with FM noise canceller IC KIA6010SN make connection as shown in Fig. 5.

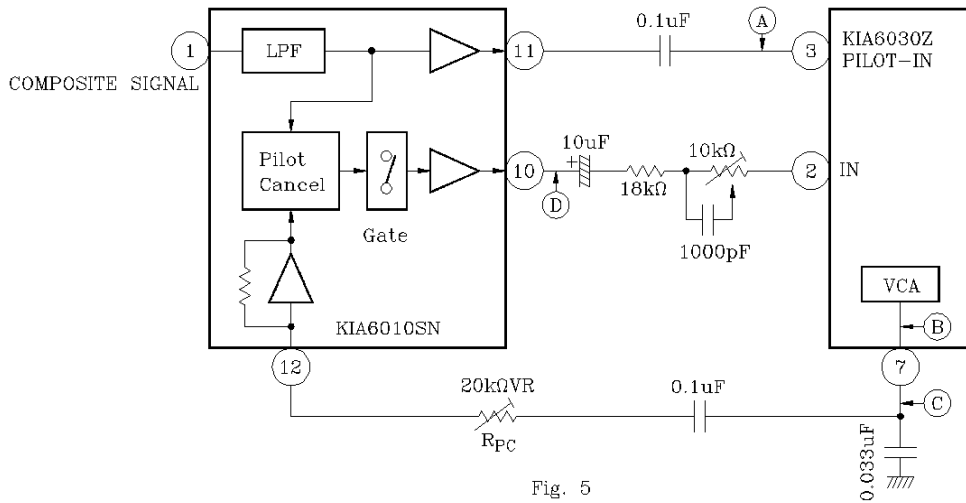


Fig. 5

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WAVEFORM OF EACH PART (Pilot modulation only)

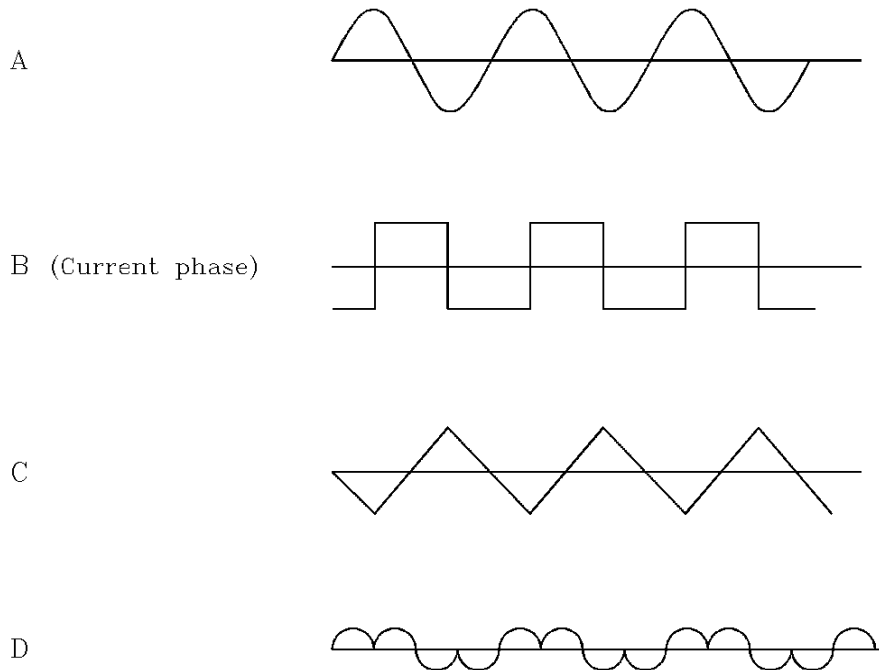


Fig. 6

OPERATION DESCRIPTION

When the pilot signal is input to ③ pin, the triangular wave (pilot output V_p), of which phase is delayed by about 180° , is output to ⑦ pin.

When this triangular wave is input to ⑫ pin of KIA6010SN, the pilot signal is canceled by the internal differential amplifier and only the residual component is output from ⑩ pin.

ADJUSTING METHOD

Perform adjustment so that KIA6010SN ⑩ pin output is made minimum with R_{PC} at the modulation only of the pilot signal. For the correct adjustment, carry out adjustment so as to make the residual components equal and minimum with L_{OUT} and R_{OUT} of KIA6030Z.

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6. Separation Adjustment

KIA6030Z is designed for using with IC for noise canceller in pair.

To obtain the optimum separation, adjust with phase compensating circuit provided to the input

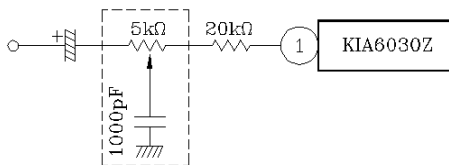


Fig. 7 PHASE COMPENSATING CIRCUIT

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