Gigabit SERDES Transceiver

IDT77V7101™

Features

- IEEE 802.3z Gigabit Ethernet compatible
- ANSI X3T11 Fibre Channel compatible
- 1.25 Gbps full duplex transmission and reception in a single IC
- Optical interface through fiber module
- 10-bit parallel TX and RX interfaces based on EIA/TIA X3T11
- Signal Detect, internal or external
- Code Group Realignment with Disable
- Internal Loopback mode
- 62.5MHz recovered clock
- Low power 3.3V CMOS
- Few external components required
- 64-pin 10mm and 14mm packages
- Pin-outs are compatible with industry standard devices
- Industrial Temperature (-40°C to +85°C) is available.

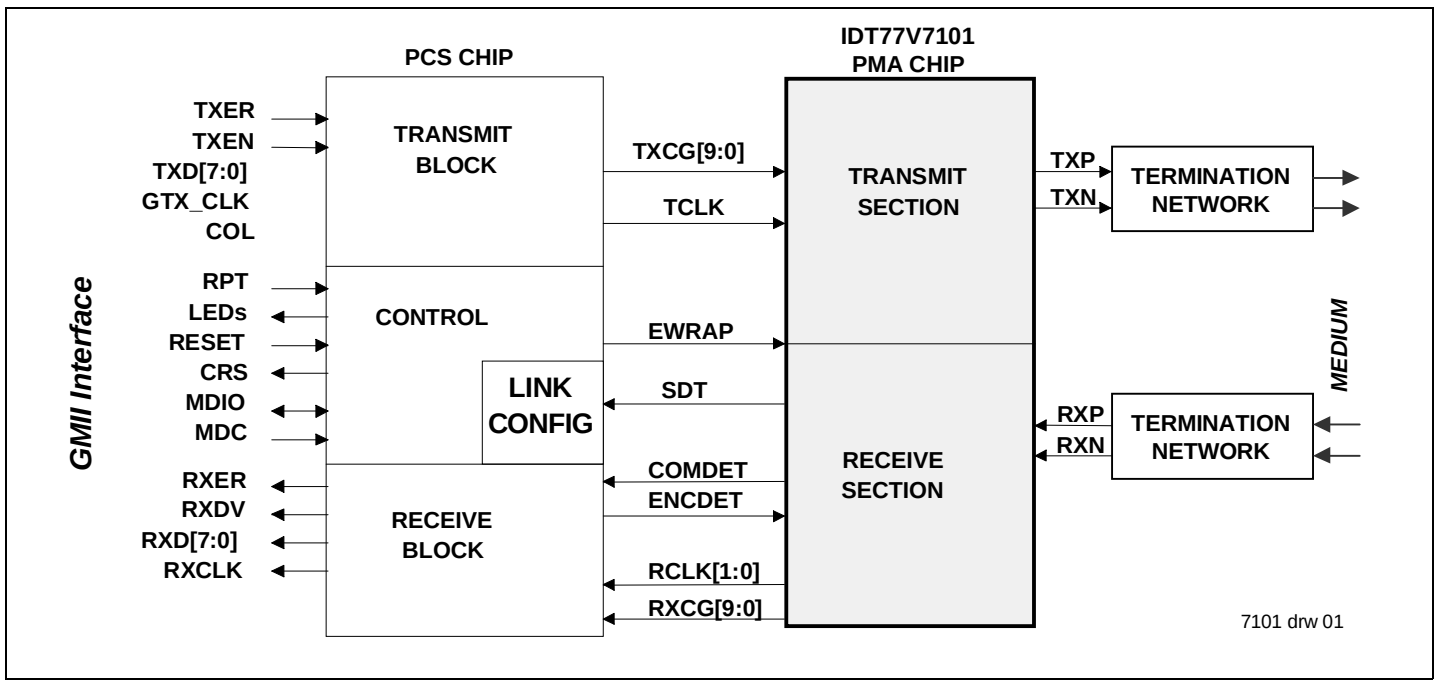
Applications

- IEEE 802.3z Gigabit media interfaces:
  - *1000BASE-LX Optical*
  - *1000BASE-SX Optical*
- *Provides the PMA function of the PHY*
- *High speed custom serial interface*
- *Backplane serial link*
- *Bus extension*

Description

The IDT77V7101 is a monolithic 1.25 Gigabits per second (Gbps) Ethernet Serializer/Deserializer (SERDES) Transceiver. It is designed to provide the Physical Medium Attachment (PMA) portion of the IEEE 802.3z PHY layer.

Typical Application Block Diagram



Functional Description

Overview

Figure 1 shows a block diagram of a typical application. The parallel interface connects to a Physical Coding Sublayer (PCS) chip. The serial inputs and outputs connect directly to a fiber optic module for optical transmission.

Figure 2 shows an internal block diagram of the IDT77V7101. The TXCG[9:0] inputs receive parallel 10-bit transmit code groups, already encoded in 8B/10B format by the PCS chip. The code groups are latched on the rising edges of the incoming 125MHz reference clock (TCLK). Then they are serialized, and the bit stream is retimed by an internal PLL that multiplies TCLK up to 1250MHz. This data stream is transmitted through PECL drivers into the cable or fiber optic module.

The 77V7101 receives serial data from the fiber optic module. It deserializes the data into 10-bit receive code groups, and recovers a receive clock (RCLK) from the data stream. RCLK is used to clock-out the receive code groups to the PCS chip.

RCLK is output at 62.5MHz in two complementary phases as RCLK[0] and RCLK[1]. RCLK[0] and RCLK[1] are used to clock out alternating code groups.

A Signal Detect I/O pin has been provided. For fiber optic media, it can be configured as an input, allowing the fiber module to perform signal detection.

Transmit Clock (TCLK)

The user-supplied 125MHz transmit reference clock (TCLK) is used for several functions. As the transmit code group clock, its rising edges directly strobe the 10-bit input data latch to sample the transmit code group bus, TXCG[9:0]. Therefore, its edges must be properly aligned to the incoming parallel transmit data.

TCLK also serves as the frequency reference for the Transmit PLL Clock Multiplier, which uses it to synthesize the internal clock signals necessary for 1.25 Gbps signaling.

Transmit Data Path

It is assumed that the original 8-bit user data to be transmitted has already been 8B/10B-encoded into 10-bit transmit code groups by external PCS logic before being sent to the IDT77V7101 for transmission. The incoming code groups are received on the Transmit Code Group bus, TXCG[9:0], and are sampled on the rising edges of TCLK by the input data latch. Figure 6 shows the timing relationship between the clock and the parallel data, and the "AC Electrical Characteristics" section shows the timing requirements for these signals.

The parallel transmit data is sent to the parallel-to-serial converter. This uses the internal clock signals synthesized by the transmit PLL to convert the 10-bit transmit data from parallel to serial format, and to retime each bit at 1250MHz. The least significant bit TXCG[0] is transmitted first.

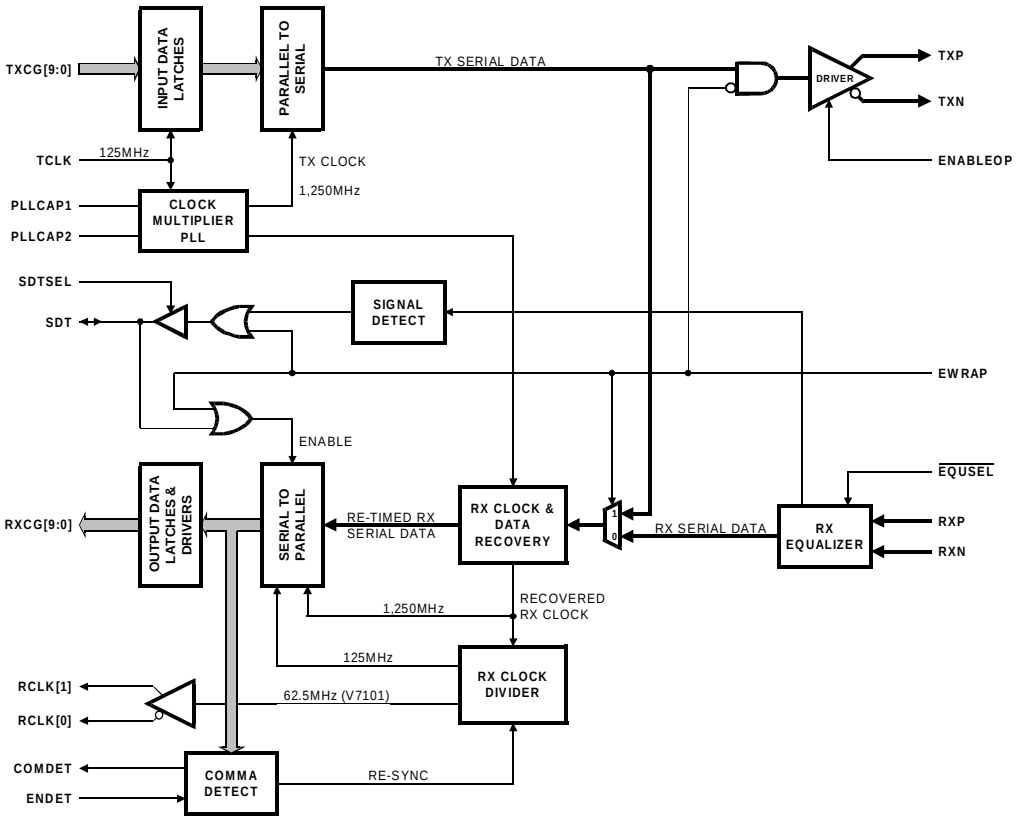


Figure 1 IDT77V7101 Internal Block Diagram

The Transmit Line Driver transmits the serial data in differential form onto the transmit half of the chosen medium. The Line Driver can connect directly to copper media such as 150W twinax cable (through DC-blocking capacitors), or through a fiber optic transceiver module to fiber optic cable.

The Line Driver is a source-follower that provides a voltage-mode differential PECL-level-compatible output. It has a differential source impedance of approximately 30W. ENABLEOP must be held to a logic high level for normal operation. When ENABLEOP is held low, the Line Driver output is set to a high impedance state.

Refer to the "Medium Attachment" section below for more information on connecting the line driver to various media.

Receive Equalization

The 77V7101 has an equalization circuit at the receiver input to compensate the signal distortion caused by unequalized cable. For operation over short cables or long internally equalized cables, the equalizer can be either enabled or disabled.

Users may wish to disable it in cases where crosstalk or reflections rather than electrical line length are the major causes of signal impairment, such as when the serial link runs through a crowded backplane or poorly matched connector rather than a long unequalized cable. Doing so can improve the tolerance of these impairments. The equalizer can also be disabled for the same reason when interfacing to fiber optic transceivers or to short or internally-equalized cables.

Clock Recovery

After the serial input signal has passed through the front end's equalizing amplifier, a receive clock must be recovered with which to sample the incoming data stream. Clock recovery is automatic, with no user intervention such as PLL training necessary. The internal Receive PLL locks the phase of its VCO to that of the incoming data to produce a bit-clock. This bit-clock is then divided down to become the internal 125MHz code-group clock (ICLK). Finally, the recovered receive clock is output as complementary signals (180ø out of phase with each other) at RCLK[0] and RCLK[1] at 62.5MHz in the 77V7101. In the 77V7101, the 62.5MHz RCLK[0] and RCLK[1] signals are used to clock out alternating 125MHz code groups.

Data Recovery

Following equalization and buffering, the receive serial data stream is retimed by the recovered bit-clock, then converted from serial to parallel form using both bit- and code-group-clocks. Parallel receive data is clocked into the output data latch by the internal 125MHz code-group-clock, and output at the Receive Code Group bus, RXCG[9:0]. RCLK[1:0] are used to clock out the data from RXCG[9:0] as described in "Clock Recovery" above.

Code Group Alignment

A code group alignment function detects the presence of comma+ characters (0011111xxx) in the receive data stream. If ENDET=1, each occurrence of a comma+ causes realignment of the bit positions of the received comma+ code group to match the standard 8B/10B format. Realignment may be achieved by dropping bits from the data stream when necessary. Comma+ characters are always clocked out by the rising edge of RCLK[1]. In the case of the 77V7101 this may entail stretching RCLK[1:0] half a cycle (nominally 8ns). Subsequent code groups retain this bit and clock alignment unless shifted by errors. If ENDET=0, realignment and clock stretching are disabled.

The COMDET output is an indicator for the detection of comma+ characters. When ENDET is high and a comma+ character is detected, COMDET will go high for half an RCLK period, following the rising edge of RCLK[0]. Otherwise, it will remain low.

Proper operation of COMDET, RCLK[1:0], and the code group alignment function requires that comma+ characters not be received back-to-back, as per standard 8B/10B encoding.

Signal Detect

The Signal Detect pin SDT is a bi-directional pin controlled by SDTSEL. When STDSEL is high, SDT is an output that remains high when the receive signal amplitude exceeds the Signal Detect threshold VSD, and receive data will be output normally at RXCG[9:0]. (Note that this does not indicate that a compliant 1000BASE-X signal is being received.) A receive signal amplitude below the threshold causes the SDT output to remain low, and the RXCG[9:0] outputs to all be forced to logic 1. This helps prevent the generation of random data at the receiver outputs in the absence of valid incoming data.

When SDTSEL is low, SDT becomes a PECL input to allow external devices such as fiber optic modules to perform the Signal Detect function. Signal detection should cause the external device to drive SDT to PECL logic 1, while insufficient signal amplitude should drive SDT to PECL logic 0. As before, a logic 0 at SDT will cause RXCG[9:0] outputs to all be forced to logic 1.

Internal Loopback

Loopback mode permits testing most of the internal circuitry without using an external medium, and is enabled by holding EWRAP high. Transmit code groups sent to the TXCG[9:0] inputs are processed normally by the transmit circuitry, then looped back through the receive circuitry to the RXCG[9:0] outputs as if they were incoming serial data. At the loopback point, transmit serial data is diverted from before the Line Driver, and replaces the equalizer output as the input to the clock and data recovery circuits. Nearly all the internal circuits except for the Line Driver and Receive Equalizer are exercised, with all internal Serializer, Deserializer, and clock functions occurring at their normal rates.

Loopback mode holds the Line Driver output at PECL logic 1. For normal operation, EWRAP must be held low.

Medium Attachment (Serial Interface)

Figure 3 shows a typical method of connecting either fiber optic links. In this case 150Ω bias resistors are connected from TXP and TXN to ground. AC-coupling of transmitter output to cable is used, as required by IEEE 802.3z. The optional series resistors RSER may be added to help absorb reflections due to mismatched loads. Typical values range from 0-50Ω. The amount of output attenuation desired should also be considered when setting these values. Load terminations, transmission lines (including traces) and connectors should be selected or designed to have matching impedances.

Thermal Considerations

The 77V7101 consumes less than 625 mW at peak power. The device is guaranteed in an ambient temperature range of 0° to +70° C for commercial temperature devices; -40° to +85° for industrial temperature devices.

Revision History

July 1, 1999: Initial publication.

September 14, 1999: Deleted drawing on page 3.

October 6, 1999: Revised Figure 2. Changed figure numbers. Added "Recommended Operating Conditions."

October 21, 1999: Revised "Receive Equalization" session. Changed t_{JTT} from "200 ps pk-pk" to "40 ps RMS." Changed cable length from 30m to 25m.

April 21, 2000: Removed references to 77V7114, 1000BASE-CX, and TwinAx cable. Deleted the figure "Typical 1000BASE-CX Medium Attachment."

September 15, 2000: Changed 100**Ω** to 115**Ω** on page 5.

November 13, 2000: Added Thermal Considerations section. Added Industrial Temperature information to Features and Ordering Information sections.

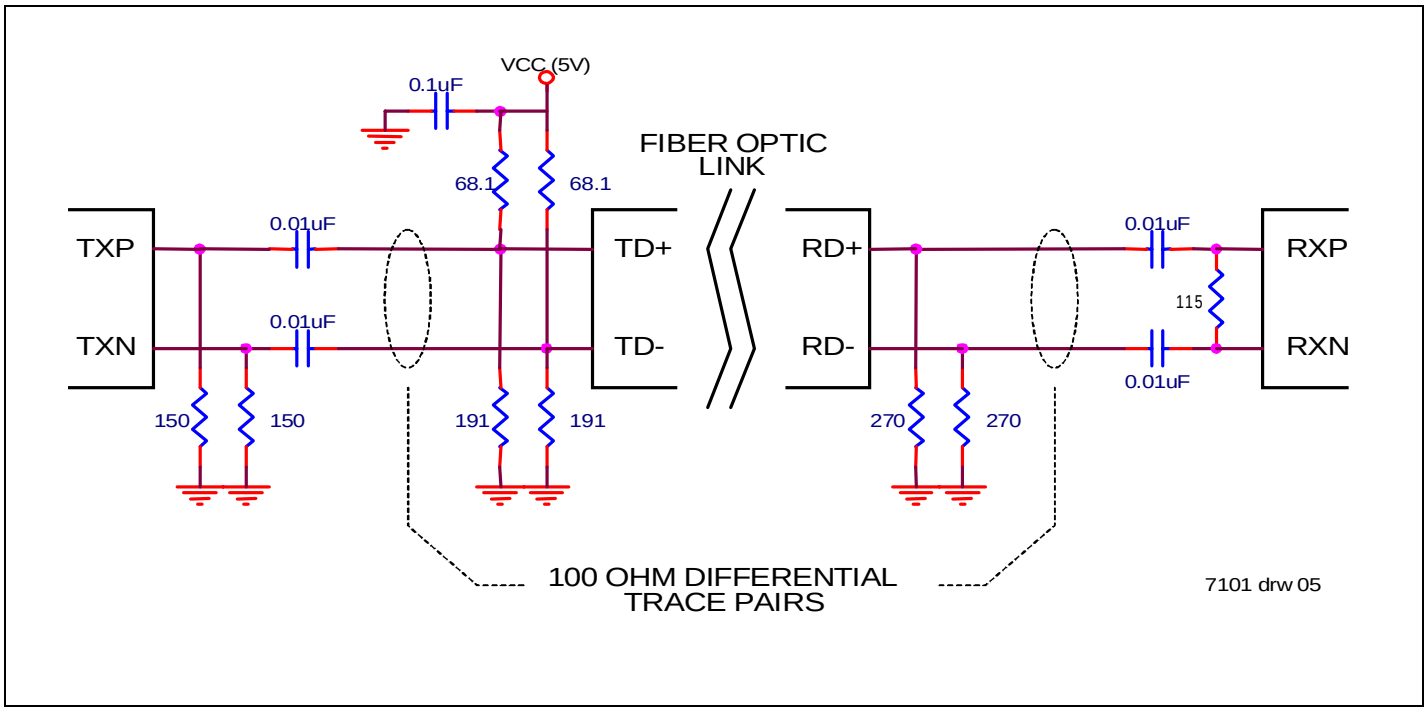


Figure 2 Typical 1000BASE-LX/SX Medium Attachment (Fiber Optic Half Link Shown)

Notes:

- The optional series RSER resistors may be added to help absorb reflections due to mismatched loads. Typical values range from 0-50Ω, depending on the characteristic impedance of the transmission lines and the amount of acceptable attenuation.
- Termination circuits at the fiber optic module are typical values for a module running on a 5V supply, with 115Ω differential impedance at each load end. Modules with other supply voltages may require adjustment of these circuit values to achieve the recommended input voltages. Follow fiber optic module manufacturer's recommendations for setting input voltages, receiver bias resistors, and termination impedance.

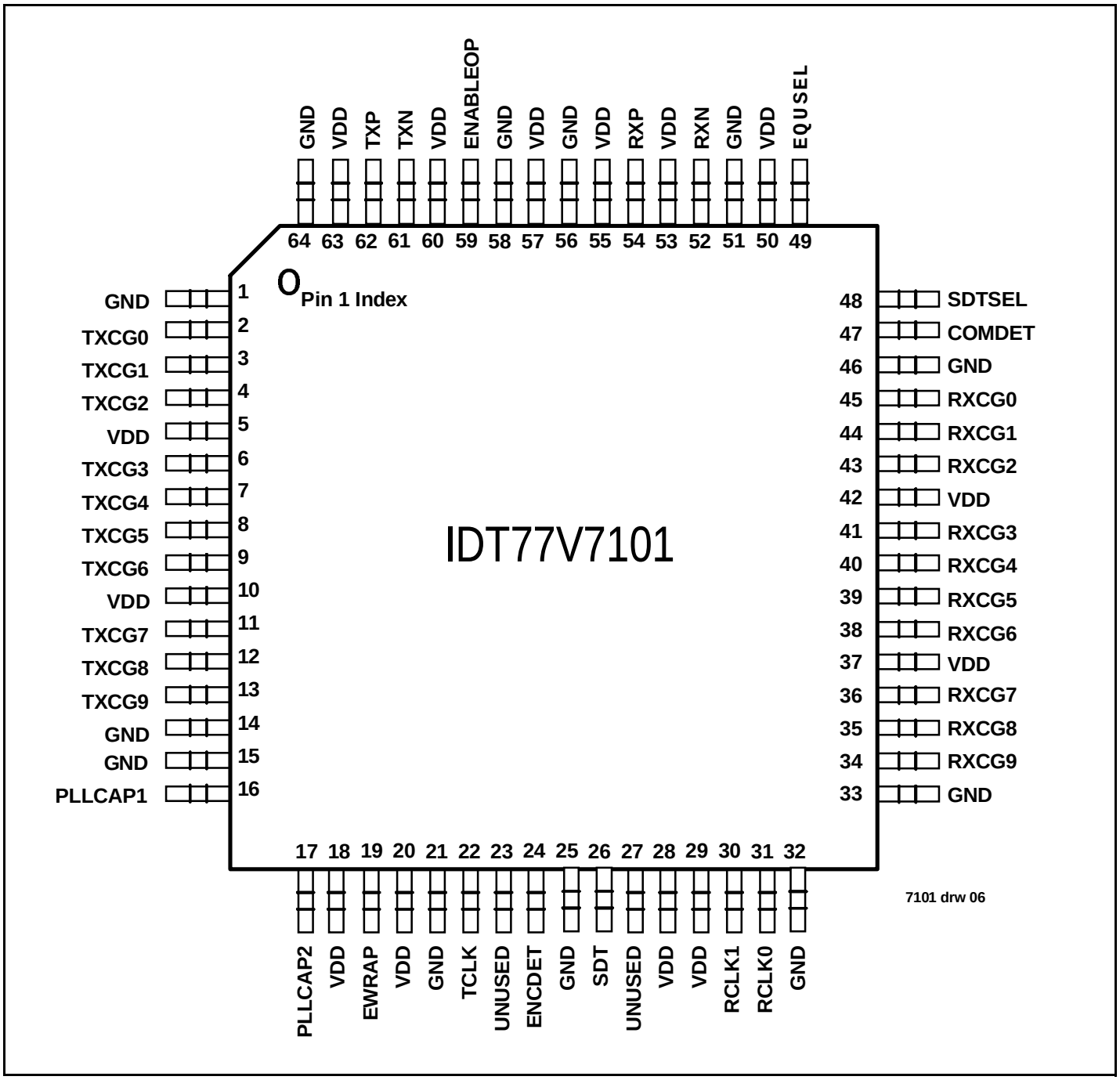


Figure 3 Pin Assignments

Pin Descriptions

Transmit-Side Signals

Pin #	Name	Type	Description
22	TCLK	TTL Input	The transmit code group clock, 1/10 the serial baud rate, whose rising edges are used to sample the incoming transmit code groups (TXCG[9:0]). TCLK is also the reference clock used by the transmit PLL to synthesize the high-speed serial data clock.
13,12,11,9,8,7, 6,4,3,2	TXCG[9:0]	TTL Inputs	The PMA chip's transmit code group input port, accepting 10-bit parallel transmit data already encoded in 8B/10B format. This bus is clocked into the chip on the rising edge of TCLK. TXCG[0] is the least significant bit and the first to be transmitted.
62,61	TXP,TXN	HS Output	The high-speed + and - serial data differential outputs to the cable or fiber optic transmitter. For output = "1", TXP > TXN.

Table 1 Transmit-Side Signals

Receive-Side Signals

Pin #	Name	Type	Description
54, 52	RXP, RXN	HS Input	The high-speed serial data differential inputs from the twisted-pair cable or fiber optic receiver. For input = "1", RXP > RXN.
34,35,36,38, 39,40,41,43, 44,45	RXCG[9:0]	TTL Output	The PMA chip's receive code group output port, presenting 10-bit receive data on alternate rising edges of RCLK[0] and RCLK[1] for the V7101. If ENCDET = 1, comma + code groups are realigned and forced to be clocked by RCLK[1]. RXCG[9:0] are forced high when SDT = 0. RXCG[0] is the least significant bit and the first to be received.
30, 31	RCLK1 RCKL0	TTL Output	The complementary receive clock outputs, recovered from the received serial data. The V7101 RCLK[1:0] outputs are 1/20 the serial baud rate, and clock-out alternate receive code groups from RXCG[9:0] on their rising edges. If ENCDET = 1. RCLK[1] clocks all comma + characters.

Table 2 Receive-Side Signals

Control Signals

Pin #	Name	Type	Description
47	COMDET	TTL Output	When ENCDET=1 and a comma+ character is detected in the receive bit stream, COMDET will go high for half an RCLK period in the V7101, or one clock period in the V7111, following the rising edge of RCLK[0].
59	ENABLEOP	TTL Input	A high level on this pin is required to activate the Line Driver, which otherwise remains in a high impedance state. An internal 50k pull-up resistor prevents "floating". Hold ENABLEOP high for normal operation.
24	ENCDET	TTL Input	A logic 1 input enables code group realignment on comma+ reception. A logic 0 input keeps current word alignment and disables COMDET. An internal 50k pull-up resistor prevents "floating".
49	EQUSEL	TTL Input	Mode Select input for Equalizer. If EQUSEL=0, equalization is on. If EQUSEL=1, equalization is off. Equalization may be turned on for all cable lengths. An internal 50k pull-down resistor prevents "floating". Hold EQUSEL low for normal operation.

Table 3 Control Signals (Part 1 of 2)

Pin #	Name	Type	Description
19	EWRAP	TTL Input	"Enable Wrap," this signal must be at a logic low level for normal operation. A high logic level forces the transmit data to be looped back from TXCG[9:0] to RXCG[9:0], exercising most of the internal circuitry. An internal 50k pull-down resistor prevents "floating". Hold EWRAP low for normal operation.
16 17	PLLCAP1 PLLCAP2	Analog	A .001µF capacitor is connected between these pins to set the loop filter characteristics of the transmit PLL.
26	SDT	Bi-directional PECL Input TTL Output	Signal Detect, with direction controlled by SDTBYPASS. If SDTBYPASS is high, SDT is a TTL output, where a logic 1 indicates that the receiver input level is above the internal "signal detect" threshold. If SDTBYPASS is low, SDT becomes a PECL input, enabling signal detection by external devices such as fiber optic transceivers. In any case, a logic 0 at SDT forces all RXCG[9:0] signals high, while a logic 1 allows normal operation.
48	SDTBYPASS	TTL Input	Signal Detect direction control. If SDTBYPASS=0, SDT is a PECL level input. If SDTBYPASS=1, SDT is a TTL output. (See SDT description above.) An internal 50k pull-up resistor prevents "floating". Hold SDTBYPASS high for normal operation.
23	UNUSED	TTL Input	This pin must be connected to VCC.
27	UNUSED	Output	This pin should be left unconnected.

Table 3 Control Signals (Part 2 of 2)

Power Supply Pins

Pin #	Name	Type	Description
5,10,18,20, 28,29,37,42,50,53,55,57,60,63	VDD	Power	Positive supply pins.
1,14,15,21, 25,32,33,46,51,56,58,64	GND	Power	Ground supply pins.

Table 4 Power Supply Pins

Electrical Specifications

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
DC Supply Voltage (VDD)	-0.5	+5	V
Terminal Voltage with respect to GND	-0.5	+5	V
Terminal Voltage with respect to VDD		+0.5	V
Storage Temperature Range	-40°	+150°	Celsius

Table 5 Absolute Maximum Ratings[1]

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	DC supply voltage	3.15	3.3	3.45	V
TA	Ambient Temperature	-40		+85	°C

Table 6 Recommended Operating Conditions

DC Electrical Characteristics (Includes all I/O pins except TXP, TXN, RXP, RXN)

Symbol	Parameter	Test Conditions[1]	Min.	Typ.	Max.	Unit
VIL, TTL[2]	TTL Input High Voltage		2.0		VDD + 0.5	V
VIL, TTL[2]	TTL Input Low Voltage		-0.3		0.80	V
VIL, PECL[3]	PECL Input High Voltage	SDTSEL is low	VDD - 1.165		VDD + 0.5	V
VIL, PECL[3]	PECL Input Low Voltage	SDTSEL is low	-0.3		VDD - 1.475	V
IIH	Input High Current	VDD = 3.45V, VIN = 2.4V			40	µA
IIL	Input Low Current	VDD = 3.5V, VIN = 0.4V	-600			µA
VOH	Output High Voltage	VDD = 3.15V, IOUT = -400µA	2.2		VDD	V
VOL	Output Low Voltage	VDD = 3.15V, IOUT = 1mA	0		0.5	V
CIH	Input Capacitance				4	pF
IDD	Transceiver VDD Supply Current	TA = 25°		180		mA
VDD	DC supply voltage		3.15	3.3	3.45	V
PD	Power dissipation			570	890	mW

Table 7 DC Electrical Characteristics (Includes all I/O pins except TXP, TXN, RXP, RXN)

1. Test conditions are Recommended Operating Conditions unless otherwise noted.
2. Not for SDT.
3. For SDT only, when SDTSEL is logic low.

AC Electrical Characteristics

Symbol	Parameter	Test Conditions[1]	Min.	Typ.	Max.	Unit
fBD[2]	Serial Baud Rate		1000	1250	1360	MBaud
fREF	TCLK Reference Frequency			fBD/10		MHz
fTOL	TCLK Frequency Tolerance		-100		+100	ppm
tDC, TC	TCLK Duty Cycle		40		60	%
tJTT	TCLK Jitter				40	ps RMS
tR, TC	TCLK Rise Time	0.8V to 2.0V	0.7		2.4	ns
tF, TC	TCLK Fall Time	2.0V to 0.8V	0.7		2.4	ns
fRCLK	RCLK Frequency (77V7101)			fBD/20		MHz
tR, RC	RCLK Rise Time	0.8V to 2.0V, CL = 10pF	0.7		2.4	ns

Table 8 AC Electrical Characteristics (Part 1 of 2)

Symbol	Parameter	Test Conditions[1]	Min.	Typ.	Max.	Unit
tF, RC	RCLK Fall Time	0.8V to 2.0V, CL = 10pF	0.7		2.4	ns
tDC, RC	RCLK Duty Cycle	1.4V to 1.4V, CL = 10pF	40		60	%
tA-B	RCLK0 to RCLK1 rising edge skew (77V7101)	1.4V to 1.4V, CL = 10pF	7.5		8.5	ns
tR, RX[3]	RXCG Rise Time	0.8V to 2.0V, CL = 10pF	0.7	1		ns
tF, RX[3]	RXCG Fall Time	0.8V to 2.0V, CL = 10pF	0.7	1		ns
tSU, RX	RXCG Setup Time to rising RCLK	{0.8,2.0}V to 1.4V, CL = 10pF	2.5			ns
tHO, RX	RXCG Hold Time from rising RCLK	1.4V to {0.8,2.0}V, CL = 10pF	1.5			ns
tR, TX[3]	TXCG Rise Time	0.8V to 2.0V	0.7			ns
tF, TX[3]	TXCG Fall Time	0.8V to 2.0V	0.7			ns
tSU, TX	TXCG Setup Time to rising TCLK	{0.8,2.0}V to 1.4V	2.0			ns
tHO, TX	TXCG Hold Time to rising TCLK	1.4V to {0.8,2.0}V	1.0			ns
tLAT, TX[4]	Transmit Latency				16	ns
tLAT, RX[5]	Receiver Latency				34	ns
VSD	Signal Detect Threshold		200	100		mV pk-pk
VIHS	HS Input Differential Voltage		200		2000	mV pk-pk
VOHS	HS Output Differential Voltage		1100		2000	mV pk-pk
VOHS, OFF	HS Output Differential Off Voltage				170	mV pk-pk
tR, HS	HS Output Differential Rise Time		85		327	ps
tF, HS	HS Output Differential Fall Time		85		327	ps
JTOTAL[6]	Total Transmit Jitter				192	ps pk-pk

Table 8 AC Electrical Characteristics (Part 2 of 2)

1. Test conditions are Recommended Operating Conditions unless otherwise noted.

2. 1250 Mbaud ±100ppm is the rate specified by IEEE 802.3z.

3. IEEE does not specify code group maximum rise and fall times, but TXCG and RXCG inputs and outputs must meet the required setup and hold times.

4. Transmitter latency is the time from the positive edge of TCLK that clocks in a particular transmit code group to the differenti al first edge of the first bit of that code group to be transmitted at TXP/N. Reference levels are 1.4V for TCLK, and zero-crossing for AC-coupled TXP-TXN.

5. Receiver latency is the time from the differential first edge of the first bit of a particular code group received at RXP/N to the positive edge of the RCLK output (RCLK 0 or RCLK1) that clocks out that code group. Reference levels are 1.4V for RCLK and zero-crossing for AC-coupled RXP-RXN.

6. Total jitter at this component level is specified by IEEE 802.3z at TP1, as they define test points. See subclauses 38.5, 38.6.8 -9, and 39.3.3 for system level specifications and measurement methods.

Timing Diagrams

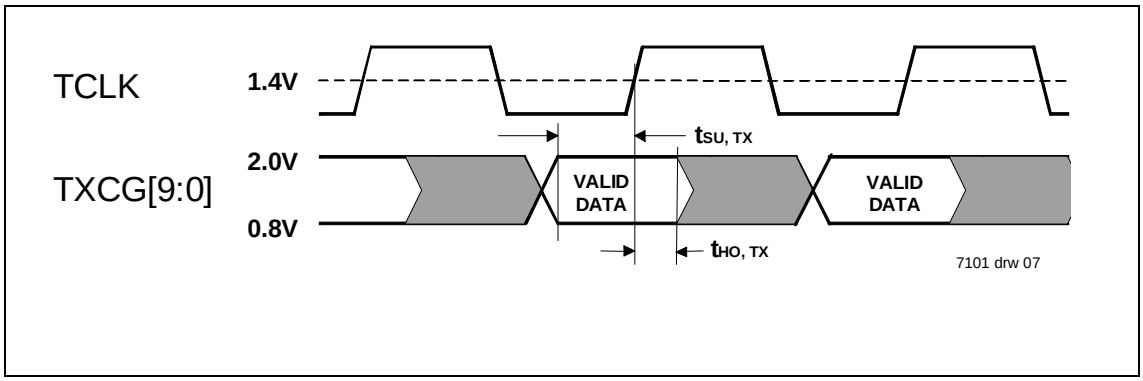


Figure 4 Transmit Parallel Interface Timing Diagram

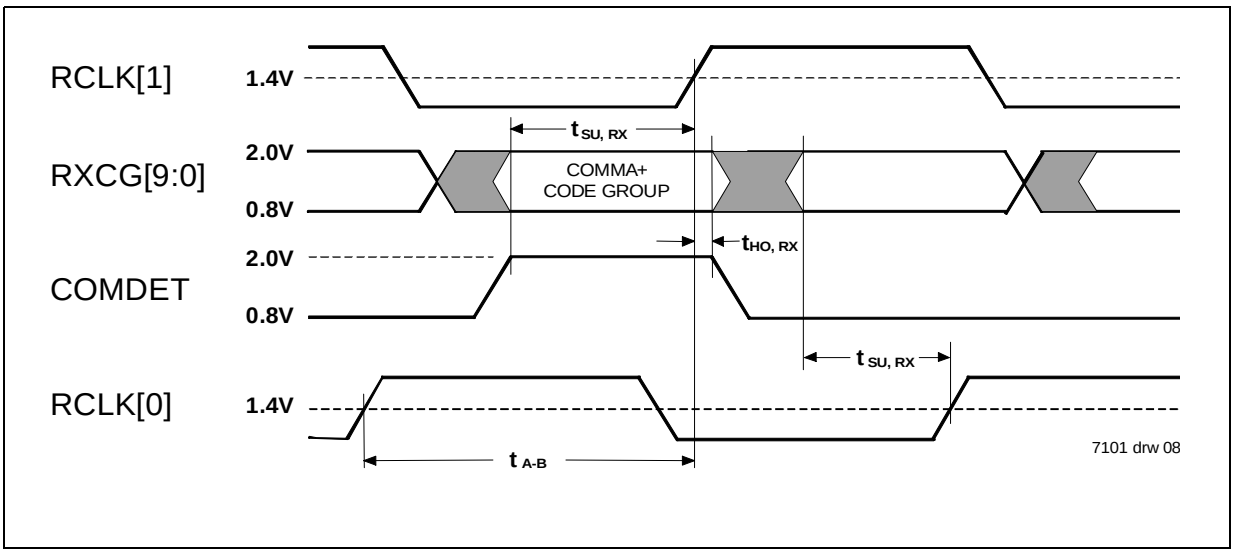


Figure 5 Receive Parallel Interface Timing Diagram

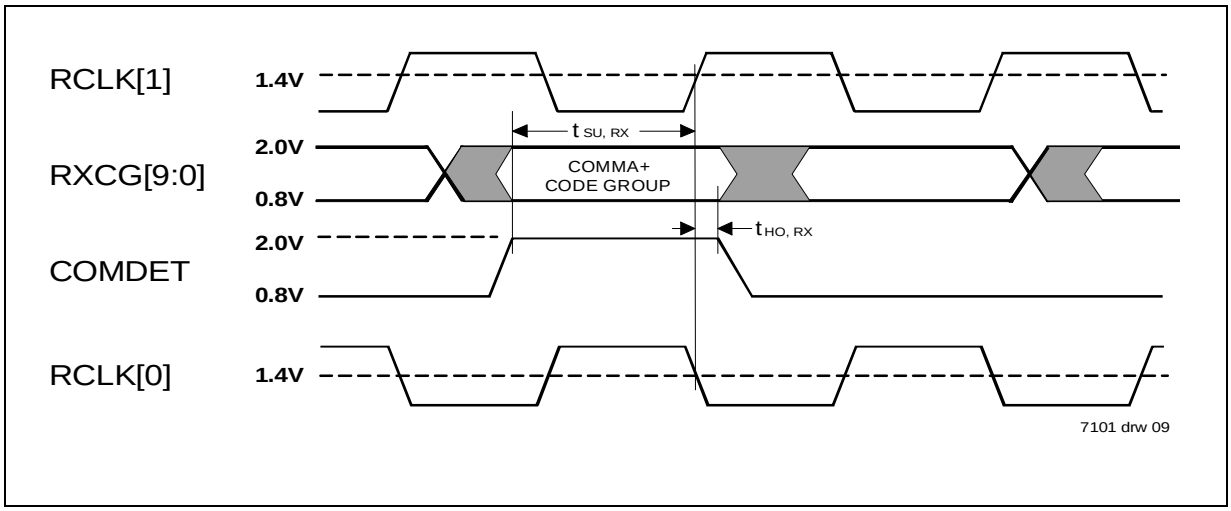
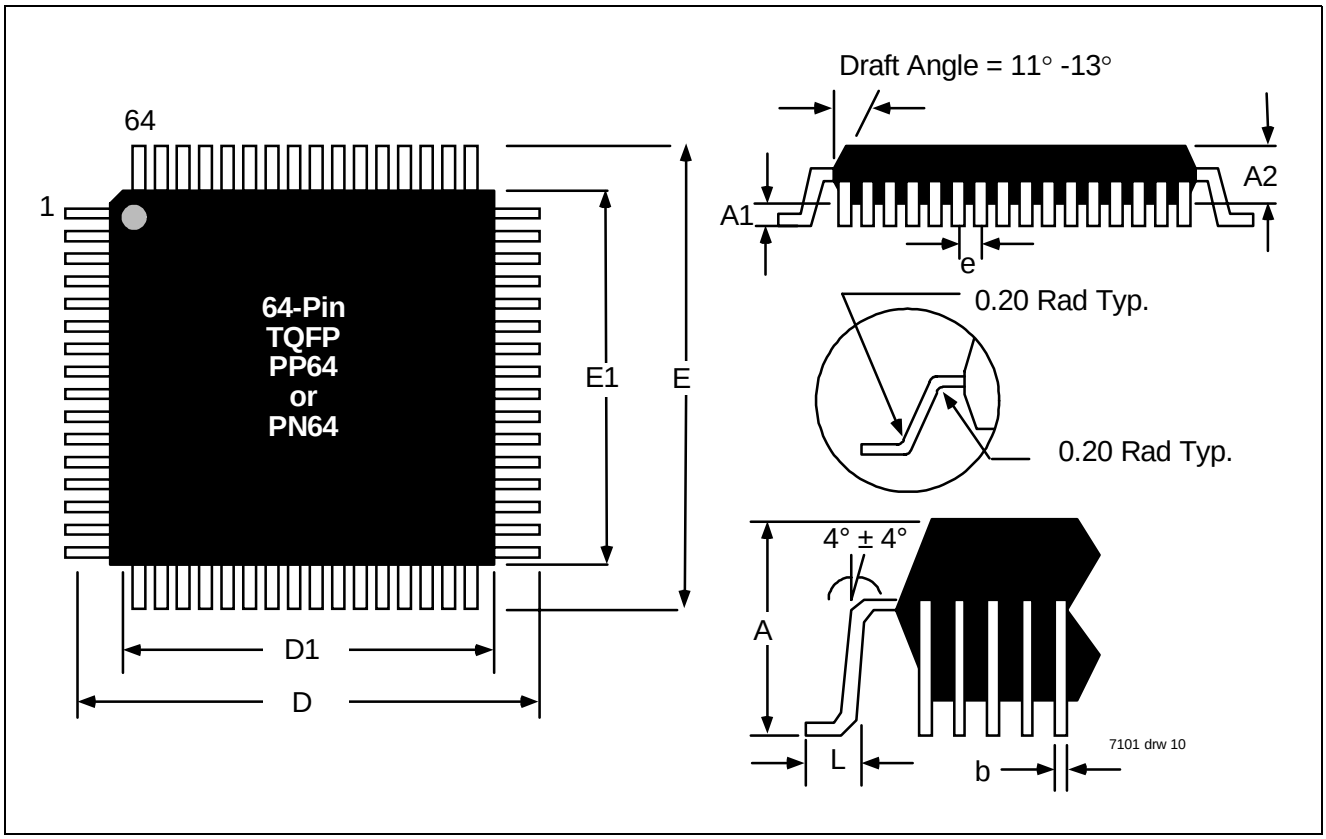


Figure 6 Receive Parallel Interface Timing Diagram

Package Dimensions[1]



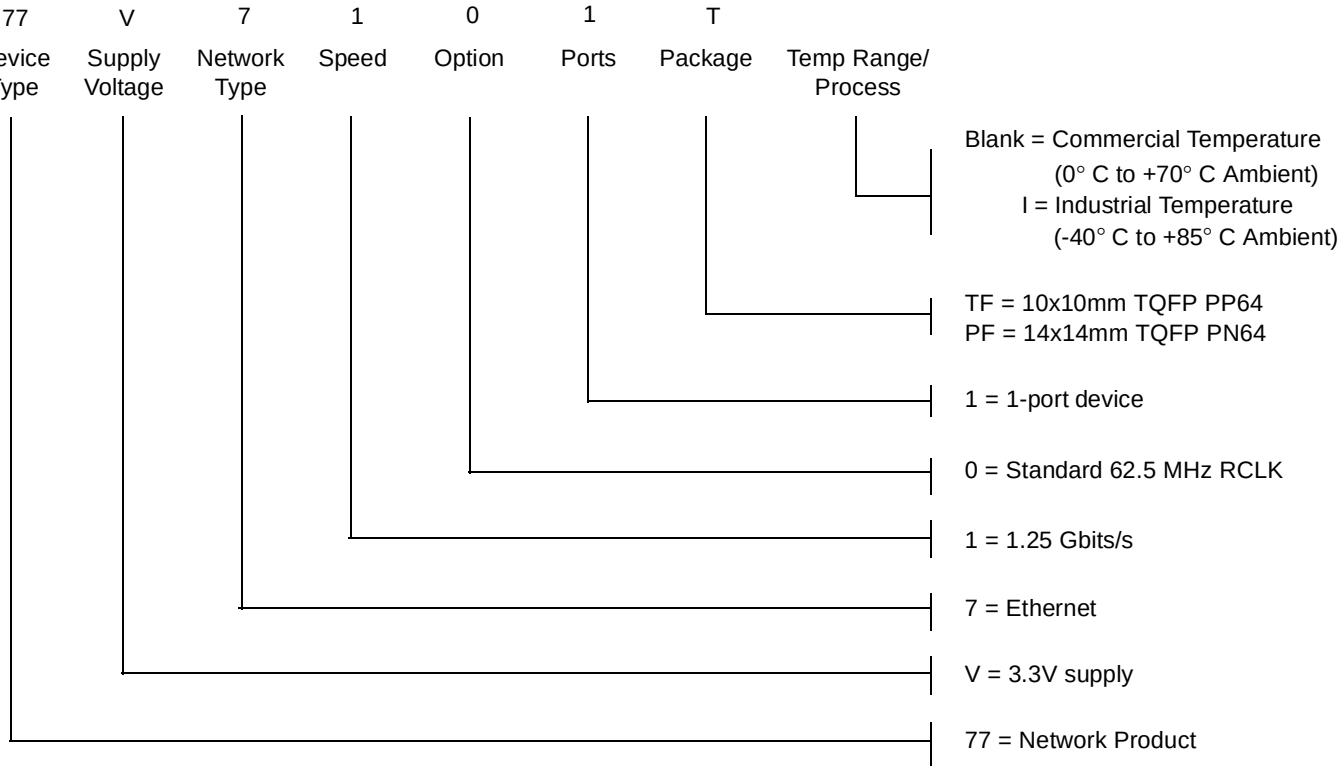
	PP64			PN64		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	1.60
A1	0.05	0.10	0.15	0.05	0.10	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45
D	—	12.00	—	—	16.00	—
D1	—	10.00	—	—	14.00	—
E	—	12.00	—	—	16.00	—
E1	—	10.00	—	—	14.00	—
L	0.45	—	0.75	0.45	—	0.75
e	—	0.50	—	—	0.80	—
b	0.17	0.22	0.27	0.30	0.37	0.45

Note: Dimensions are in millimeters.

1. A more comprehensive package outline drawing is available from the IDT website.

Ordering Information

IDT77V7101T



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