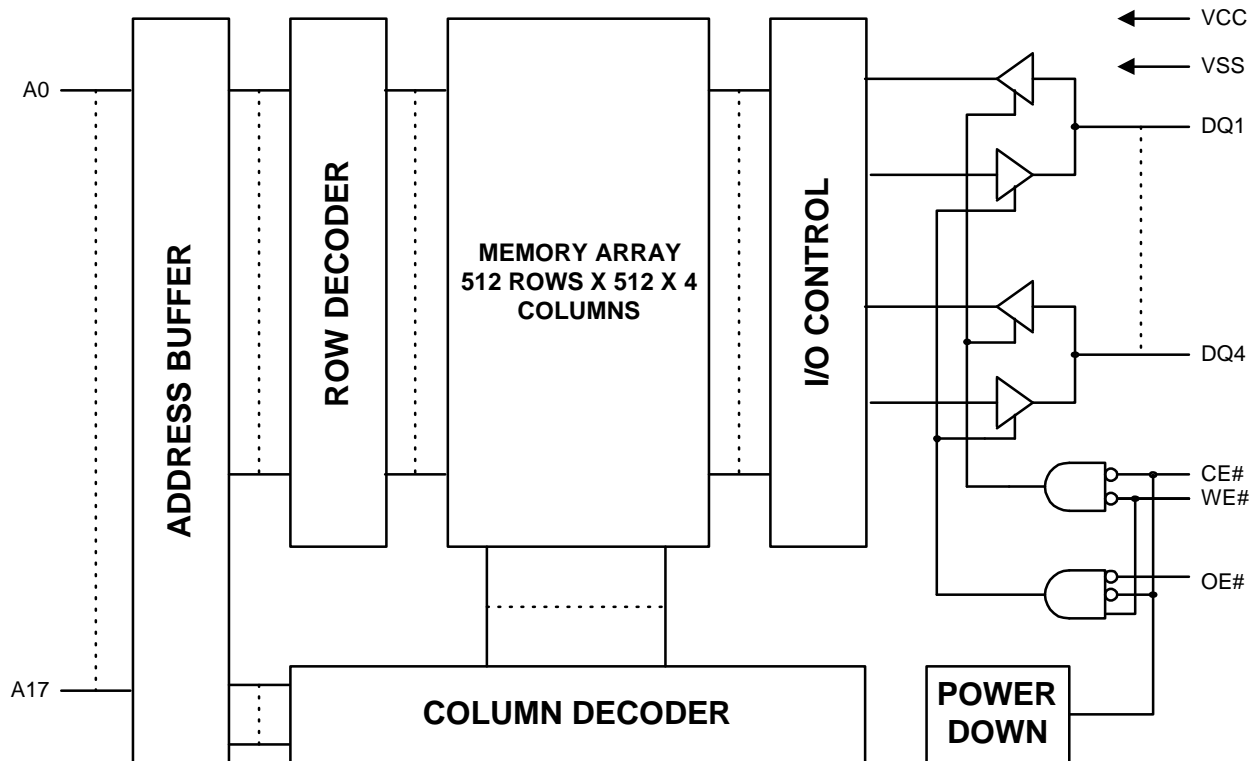


FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	CE#	WE#	OE#	DQ	POWER
READ	L	H	L	Q	ACTIVE
WRITE	L	L	X	D	ACTIVE
OUTPUT DISABLE	L	H	H	HIGH-Z	ACTIVE
STANDBY	H	X	X	HIGH-Z	STANDBY

PIN DESCRIPTIONS

SOJ Pin Numbers	SYMBOL	TYPE	DESCRIPTION
21-27, 1-11	A0-A17	Input	Addresses Inputs: These inputs determine which cell is addressed.
15	WE#	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. WE# is LOW for a WRITE cycle and HIGH for a READ cycle.
12	CE#	Input	Chip Enable: This active LOW input is used to enable the device. When CE# is LOW, the chip is selected. When CE# is HIGH, the chip is disabled and automatically goes into standby power mode.
13	OE#	Input	Output Enable: This active LOW input enables the output drivers.
16, 17, 18, 19	DQ1-DQ4	Input/Output	SRAM Data I/O: Data inputs and data outputs
28	VCC	Supply	Power Supply: 5V \pm 10%
14	VSS	Supply	Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.....-0.5V to +7.0V
 V_{IN} -0.5V to VCC+0.5V
 Storage Temperature (plastic)-55°C to +125°
 Junction Temperature+125°
 Power Dissipation1.2W
 Short Circuit Output Current50mA

*Stresses greater than those listed under “Absolute Maximum

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (All Temperature Ranges; VCC = 5V ±10% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) voltage		V_{IH}	2.2	VCC+1	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq VCC$	IL_I	-5	5	uA	
Output Leakage Current	Output(s) disabled, $0V \leq V_{OUT} \leq VCC$	IL_O	-5	5	uA	
Output High Voltage	$I_{OH} = -4.0mA$	V_{OH}	2.4		V	1
Output Low Voltage	$I_{OL} = 8.0mA$	V_{OL}		0.4	V	1
Supply Voltage		VCC	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	POWER	-10	-12	-15	-20	UNITS	NOTES
Power Supply Current: Operating	Device selected; CE# $\leq V_{IL}$; VCC =MAX; f=f _{MAX} ; outputs open	I _{CC}	80	standard	240	220	180	140	mA	3, 14
				low	210	180	150	110		
TTL Standby	CE# $\geq V_{IH}$; VCC = MAX; f=f _{MAX}	I _{SB1}	20	standard	60	55	50	40	mA	14
				low	45	40	35	30		
CMOS Standby	CE# $\geq VCC - 0.2$; VCC = MAX; all other inputs $\leq VSS + 0.2$ or $\geq VCC - 0.2$; all inputs static; f= 0	I _{SB2}	0.75	standard	5	5	5	7	mA	14
				low	5	5	5	7		

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^\circ C$; f = 1 MHz VCC = 5V	C_I	6	pF	4
Input/Output Capacitance (DQ)		$C_{I/O}$	8	pF	4

AC ELECTRICAL CHARACTERISTICS

(Note 5) (All Temperature Ranges; VCC = 5V \pm 10%)

DESCRIPTION	SYM	- 10		- 12		- 15		- 20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	^t RC	10		12		15		20		ns	
Address access time	^t AA		10		12		15		20	ns	
Chip Enable access time	^t ACE		10		12		15		20	ns	
Output hold from address change	^t OH	3		4		4		4		ns	
Chip Enable to output in Low-Z	^t LZCE	3		4		4		4		ns	4, 7
Chip disable to output in High-Z	^t HZCE		5		6		7		8	ns	4, 6, 7
Output Enable access time	^t AOE		5		6		7		8	ns	
Output Enable to output in Low-Z	^t LZOE	0		0		0		0		ns	
Output Enable to output in High-Z	^t HZOE		5		6		7		8	ns	4, 6
Chip Enable to power-up time	^t PU	0		0		0		0		ns	4
Chip disable to power-down time	^t PD		10		12		15		20	ns	4
WRITE Cycle											
WRITE cycle time	^t WC	10		12		15		20		ns	
Chip Enable to end of write	^t CW	8		8		9		10		ns	
Address valid to end of write, with OE# HIGH	^t AW	8		8		9		10		ns	
Address setup time	^t AS	0		0		0		0		ns	
Address hold from end of write	^t AH	0		0		0		0		ns	
WRITE pulse width	^t WP2	10		10		11		12		ns	
WRITE pulse width, with OE# HIGH	^t WP1	8		8		9		10		ns	
Data setup time	^t DS	6		6		7		8		ns	
Data hold time	^t DH	0		0		0		0		ns	
Write disable to output in Low-Z	^t LZWE	3		4		5		5		ns	4, 7
Write Enable to output in High-Z	^t HZWE		5		6		7		8	ns	4, 6, 7

AC TEST CONDITIONS

Input pulse levels	0V to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

OUTPUT LOADS

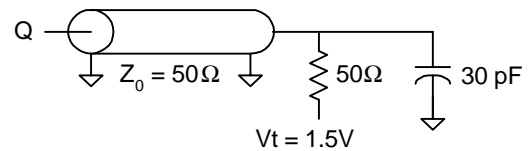


Fig. 1 OUTPUT LOAD EQUIVALENT

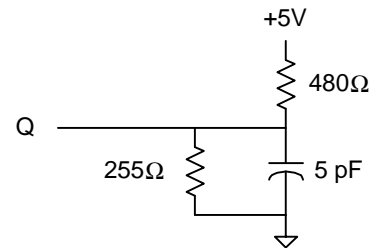


Fig. 2 OUTPUT LOAD EQUIVALENT

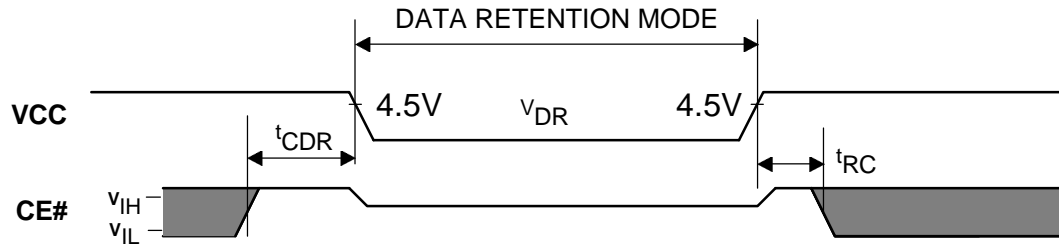
NOTES

- All voltages referenced to VSS (GND).
- Overshoot: $V_{IH} \leq +7.0V$ for $t \leq t_{RC} / 2$.
Undershoot: $V_{IL} \leq -2.0V$ for $t \leq t_{RC} / 2$
- I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- Output loading is specified with $C_L = 5pF$ as in Fig. 2. Transition is measured $\pm 500mV$ from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} .
- WE# is HIGH for READ cycle.
- Device is continuously selected. Chip enable and output enables are held in their active state.
- Address valid prior to, or coincident with, latest occurring chip enable.
- t_{RC} = Read Cycle Time.
- Chip Enable and Write Enable can initiate and terminate a WRITE cycle.
- Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.
- Typical values are measured at 5V, 25°C and 20ns cycle time.

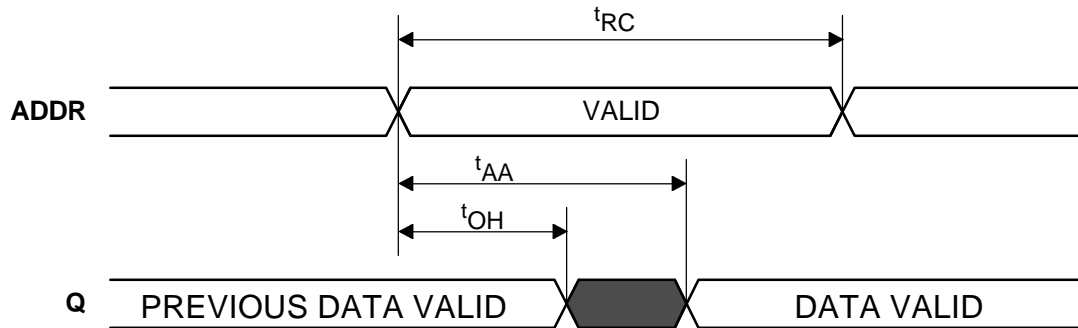
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{cc} for Retention Data		V _{DR}	2			V	
Data Retention Current	CE# $\geq V_{CC} - 0.2$; all other inputs $\leq V_{SS} + 0.2$ or $\geq V_{CC} - 0.2$; all inputs static; f = 0	V _{cc} = 2V		100	500	uA	13
		V _{cc} = 3V		200	750	uA	13
Chip Deselect to Data Retention Time		t _{CDR}	0			ns	4
Operation Recovery Time		t _r	t _{RC}			ns	4, 11

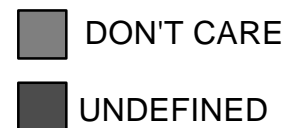
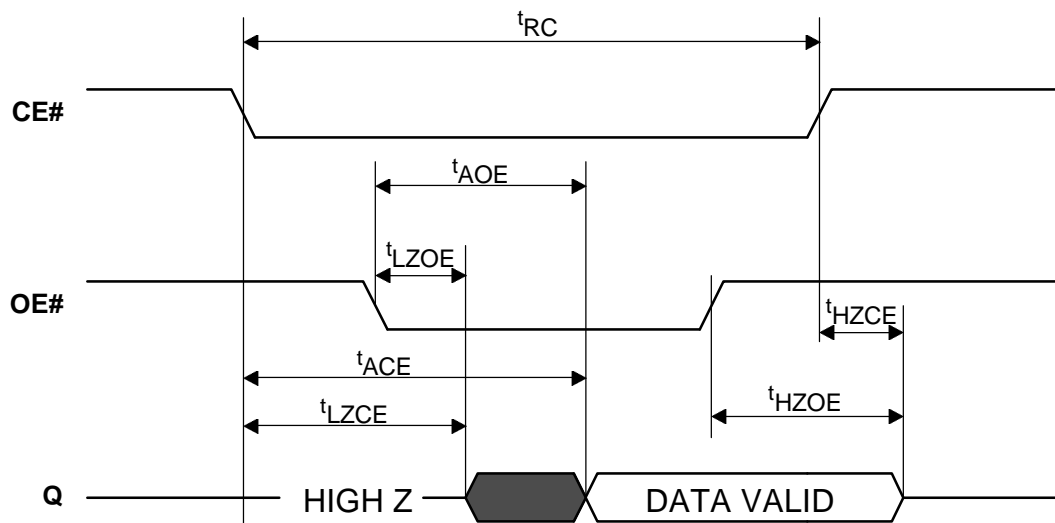
LOW VCC DATA RETENTION WAVEFORM



READ CYCLE NO. 1^(8, 9)

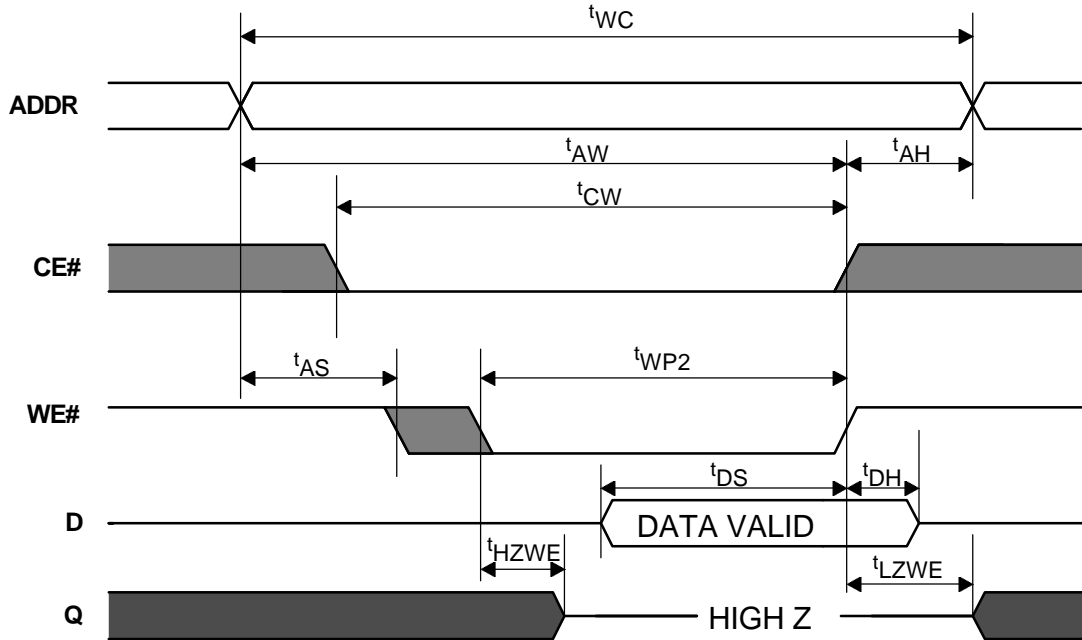


READ CYCLE NO. 2^(7, 8, 10, 12)



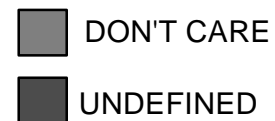
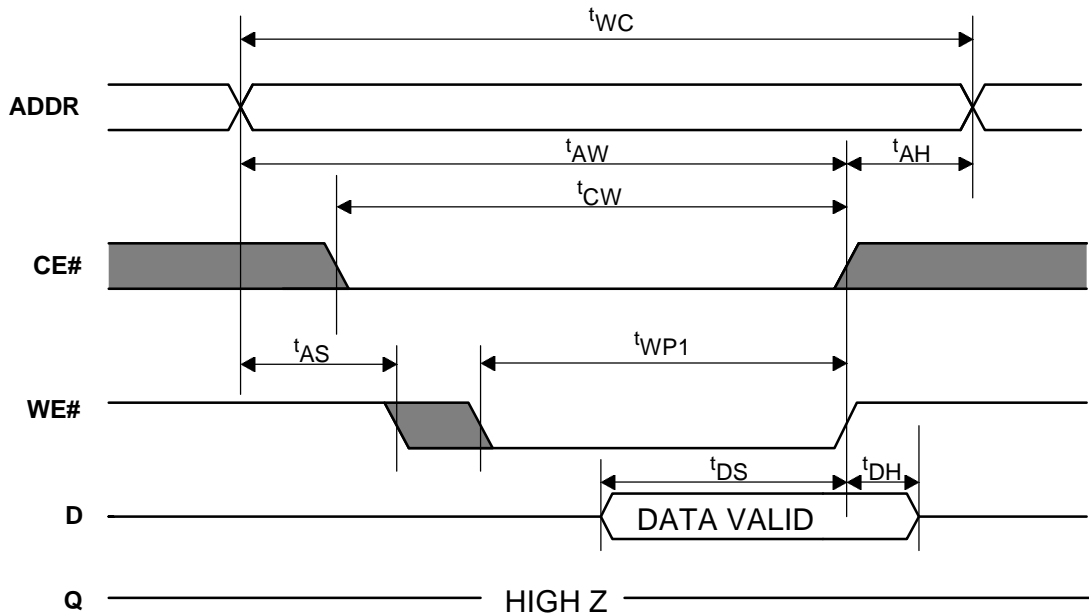
WRITE CYCLE NO. 1^(7, 12, 13)

(Write Enable Controlled with Output Enable OE# active LOW)

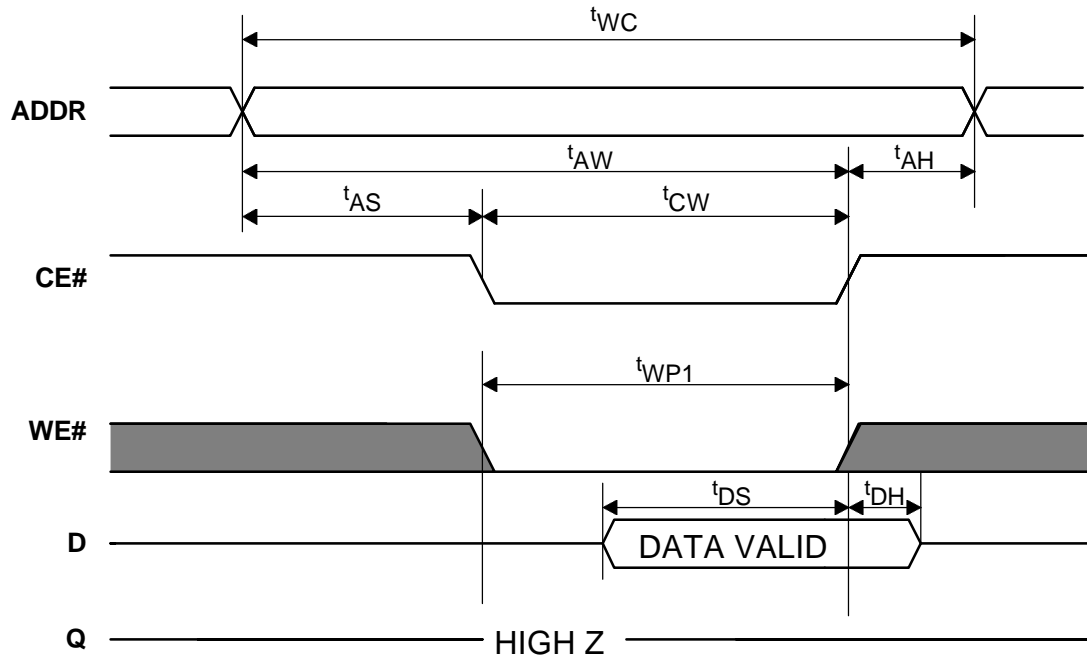


WRITE CYCLE NO. 2^(12, 13)

(Write Enable Controlled with Output Enable OE# inactive HIGH)

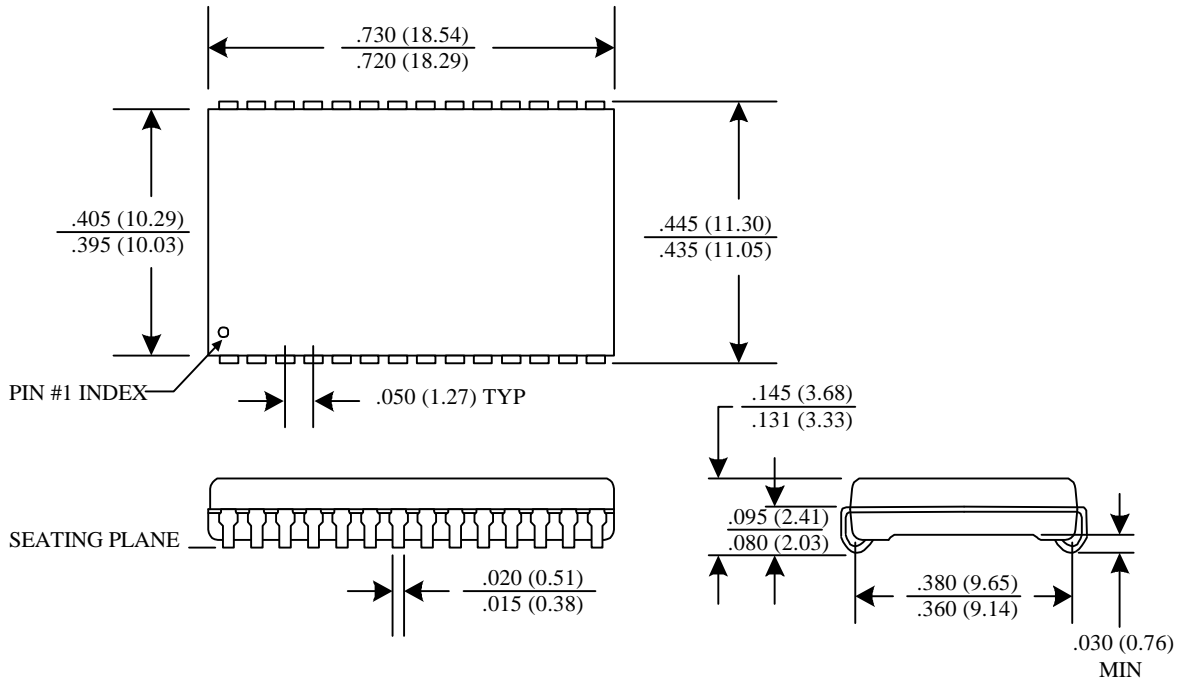


WRITE CYCLE NO. 3^(12, 13) (Chip Enable Controlled)



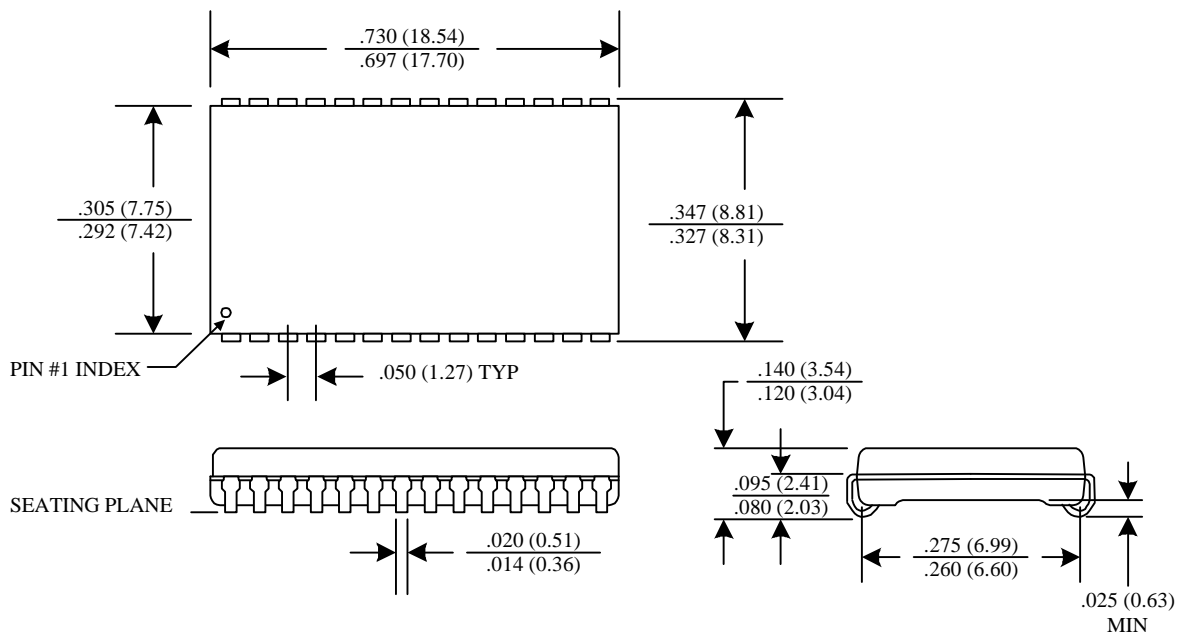
Package Dimensions

28-pin 400 Mil Plastic SOJ (J)



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical, min where noted.

28-pin 300 Mil Plastic SOJ (SJ)



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical, min where noted.

Ordering Information

GVT 72028A4 XX - XX X X

Galvantech Prefix

Part Number

Temperature (Blank = Commercial
I = Industrial)

Power (Blank= Standard,
L= Low Power)

Speed (10 = 10ns, 12= 12ns
15 = 15ns, 20 = 20ns)

Package (J = 400 mil SOJ,
SJ= 300 mil SOJ)