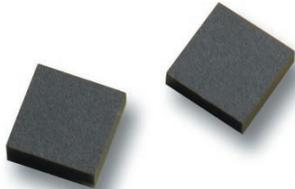


Agilent ACPM-7833 CDMA1900 (PCS) Power Amplifier

Preliminary Data Sheet



Features

- **Operating frequency:**
1850–1910 MHz
- **28.5 dBm linear output power @ 3.4 V**
- **High efficiency: 40% PAE**
- **Very low quiescent current with single control voltage or**
- **Dynamic bias control**
- **Internal 50 ohm matching networks for both RF IN/OUT**
- **3.2– 4.2 V linear operation**
- **cdma2000 1xRTT capable**
- **Only 3 SMT parts needed**
- **4.0 x 4.0 x 1.1 mm SMT package**

Description

The ACPM-7833 is a fully matched CDMA Power amplifier module. Designed around Agilent Technologies' new Enhancement Mode pHEMT process, the ACPM-7833 offers premium performance in a very small form factor. Fully matched to 50 Ohms on the input and output.

The amplifier has excellent ACPR and efficiency performance at max Pout and low quiescent

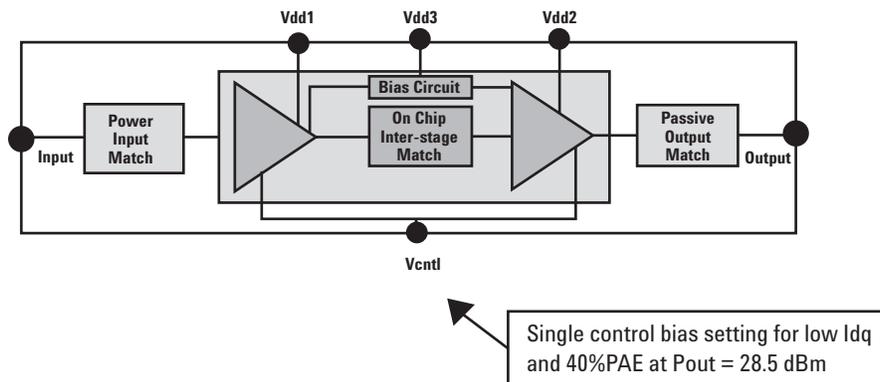
current with a single bias control voltage. For even lower quiescent current, a dynamic bias control circuit can be used; Vcntl = 1.2V to 2.2V.

Designed in a surface mount RF package, the ACPM-7833 is cost and size competitive.

The ACPM-7833 is another key component of the Agilent **CDMAAdvantage** RF chipset.

Applications

- **CDMA handsets**
- **Datacards**
- **PDA's**



Preliminary Product Disclaimer

This preliminary data sheet is provided to assist you in evaluating this product that is under development. Until Agilent Technologies releases this product for general sale, Agilent reserves the right to alter prices, specifications, features, capabilities, function, manufacturing release dates, and even general availability of the product at any time.



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Maximum Ratings^[1]

Parameter	Min.	Max.
Vdd Supply Voltage		5.0 V
Power Dissipation ^[2, 3]		2.5 W
Bias Current		1.5 A
Control Voltage (Vcntl)		3.0 V
Amplifier Input RF Power		10 dBm
Junction Temperature		+150°C
Storage Temperature (case temperature)	-30°C	+100°C

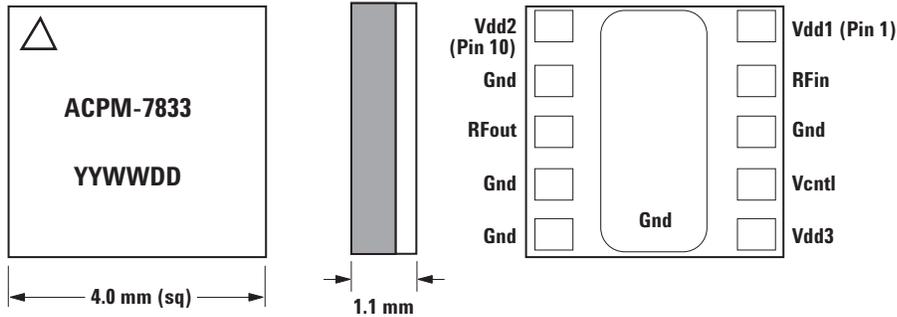
Thermal Resistance^[2] $\theta_{jc} = \text{TBD}^{\circ}\text{C}/\text{W}$

Recommended operating range of Vdd = 3.2 to 4.2 V, Ta = -30 to +85°C

Notes:

1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Tcase = 25°C
3. Derate at TBD mW/°C for Tcase >85°C

Package Marking and Dimensions



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Electrical Characterization Information

All tests are done in 50Ω system at $V_{dd} = 3.4V$, 25°C, unless noted otherwise.

Parameter	Units	Min	Typ	Max	Comments
Cellular CDMA					
Frequency Range	MHz	1850		1910	
Gain (Fixed Cntl Voltage) ($P_{out} = 28.5$ dBm)	dB		26		Vcntl= 2.2V
Power Added Efficiency					
$P_{out} = 28.5$ dBm	%		40		Vcntl= 2.2V
$P_{out} = 16$ dBm	%		8.5		Vcntl= 1.6V
Total Supply Current	mA		520		$P_{out} = 28.5$ dBm, Vcntl= 2.2V
ACPR @ ± 1.25 MHz offset	dBc/30 kHz		-48		$P_{out} \leq 28.5$ dBm
ACPR @ ± 1.98 MHz offset	dBc/30 kHz		-55		$P_{out} \leq 28.5$ dBm
Quiescent Current	mA		60		$P_{out} \leq 28.5$ dBm, Vcntl= 2.2V
Input VSWR ($P_{out} = 28.5$ dBm)			2.0:1		
Noise Figure	dB		4.5		
Noise Power @ 45 MHz offset in 1930–1990 MHz	dBm/Hz		-141		
Stability (Spurious): Load VSWR 5:1	dBc		-50		All phases
Harmonic Suppression: 2Fo	dBc		-38		

ACPR Measurement Method

$$ACPR = \frac{\text{Channel Power in the 1.2288 MHz band}}{\text{Power in a 30 kHz band @ 1.25 MHz away from the center of the channel}}$$

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Demoboard Application Information

The demoboard has a 10-pin header to apply/measure the various DC signals associated with the Power Amplifier. Each pin has a label next to it. A description for each pin is shown in the table below.

Demoboard Pin (DC header)	Function/Applied Signal
Top of Demoboard	
Gnd	Ground
Vdd1	Bias voltage, typically 3.4V
Vdd3	Bias voltage, typically 3.4V
Gnd	Ground
Vdd2	Bias voltage, typically 3.4V
Bottom of Demoboard	
Vdd1 (S)	Voltage sense line for Vdd1 (can be left unconnected)
Vcntl	Control line (0V=off, 1.6V=med pwr, 2.2V=full pwr)
Vdd3 (S)	Voltage sense line for Vdd3 (can be left unconnected)
Gnd	Ground
Vdd2 (S)	Voltage sense line for Vdd2 (can be left unconnected)

Operating Instructions

1. Connect RFin and RFout
2. Apply Gnd to demoboard
3. Apply Vcntl = 0V
4. Apply Vdd1, Vdd2, Vdd3
5. Increase Vcntl to desired value (1.6V for medium power operation or 2.2V for full power operation)

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February 10, 2003



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