INTRODUCTION

S6A0079 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology. It can display 2, or 4 lines with 5 x 8 dots format.

FUNCTIONS

— Character type dot matrix LCD driver & controller

— Internal driver: 34 common and 120 segment signal output

— Easy interface with 4-bit or 8-bit MPU

— 5 x 8 dots matrix possible

— Voltage converter for LCD drive voltage: 13V max (2 times/3 times)

— Automatic power on reset

FEATURES

— Internal memory
  – Character Generator ROM (CGROM): 9,600 bits (240 characters x 5 x 8 dot)
  – Character Generator RAM (CGRAM): 64 x 8 bits (8 characters x 5 x 8 dot)
  – Icon RAM (CGRAM): 16 x 8 bits (80 icons max.)
  – Display Data RAM (DDRAM): 96 x 8 bits (96 characters max.)

— Low power operation
  – Power supply voltage range: 2.7 to 5.5V (V_{DD})
  – LCD Drive voltage range: 3.0 to 13.0V (V_{DD} - V5)

— CMOS process

— Duty cycle: 1/33

— Internal oscillator with an external resistor

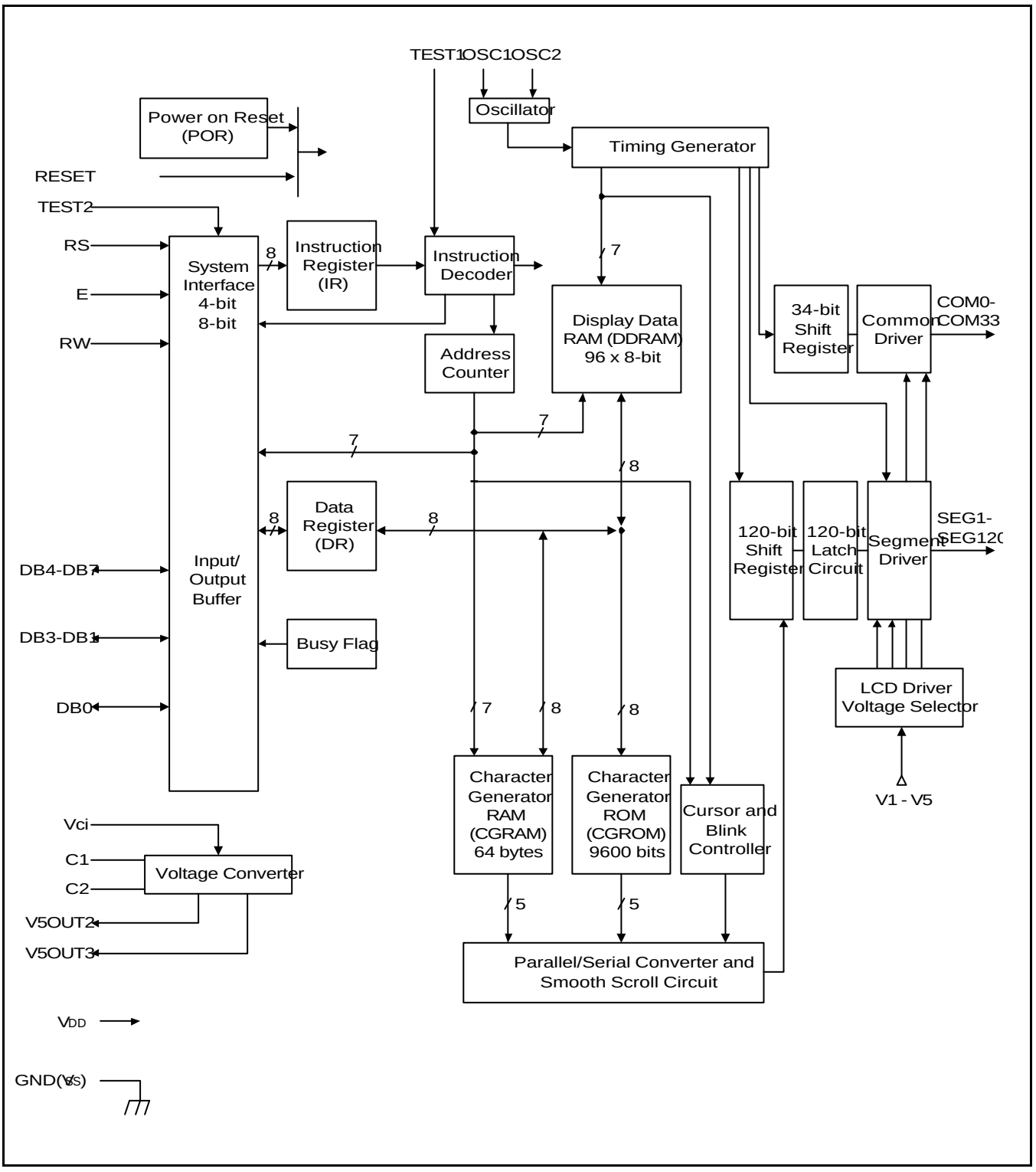
— Bare chip available

PROGRAMMABLE DUTY CYCLES

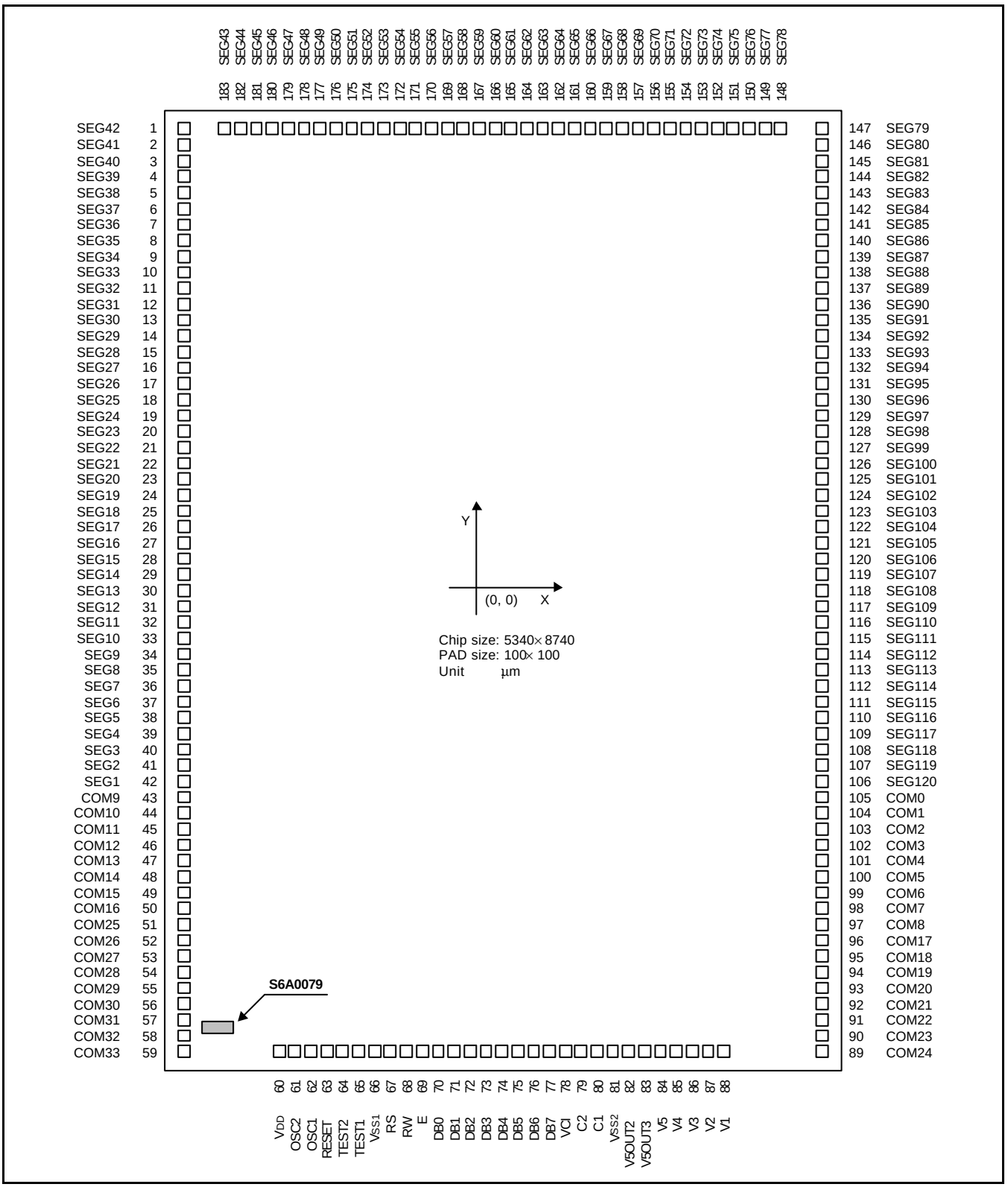
5-Dot Font Width

Display Line Numbers	Duty Ratio	Single-chip Operation	
		Displayable Characters	Possible Icons
2	1/33	2-line of 48 characters	80
4	1/33	4-line of 24 characters	80

BLOCK DIAGRAM



PAD CONFIGURATION



PAD CENTER COORDINATES

Table 1. Pad Location

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	SEG42	-2504	3540	33	SEG10	-2504	-459	65	TEST1	-1125	-4119
2	SEG41	-2504	3415	34	SEG9	-2504	-584	66	VSSI	-1000	-4119
3	SEG40	-2504	3290	35	SEG8	-2504	-709	67	RS	-875	-4119
4	SEG39	-2504	3165	36	SEG7	-2504	-834	68	RW	-750	-4119
5	SEG38	-2504	3040	37	SEG6	-2504	-959	69	E	-625	-4119
6	SEG37	-2504	2915	38	SEG5	-2504	-1084	70	DB0	-500	-4119
7	SEG36	-2504	2790	39	SEG4	-2504	-1209	71	DB1	-375	-4119
8	SEG35	-2504	2665	40	SEG3	-2504	-1334	72	DB2	-250	-4119
9	SEG34	-2504	2540	41	SEG2	-2504	-1459	73	DB3	-125	-4119
10	SEG33	-2504	2415	42	SEG1	-2504	-1584	74	DB4	0	-4119
11	SEG32	-2504	2290	43	COM9	-2504	-1822	75	DB5	125	-4119
12	SEG31	-2504	2165	44	COM10	-2504	-1947	76	DB6	250	-4119
13	SEG30	-2504	2040	45	COM11	-2504	-2072	77	DB7	375	-4119
14	SEG29	-2504	1915	46	COM12	-2504	-2197	78	Vci	500	-4119
15	SEG28	-2504	1790	47	COM13	-2504	-2322	79	C2	625	-4119
16	SEG27	-2504	1665	48	COM14	-2504	-2447	80	C1	750	-4119
17	SEG26	-2504	1540	49	COM15	-2504	-2572	81	VSS2	875	-4119
18	SEG25	-2504	1425	50	COM16	-2504	-2697	82	V5OUT2	1000	-4119
19	SEG24	-2504	1290	51	COM25	-2504	-2822	83	V5OUT3	1125	-4119
20	SEG23	-2504	1165	52	COM26	-2504	-2947	84	V5	1250	-4119
21	SEG22	-2504	1040	53	COM27	-2504	-3072	85	V4	1375	-4119
22	SEG21	-2504	915	54	COM28	-2504	-3197	86	V3	1500	-4119
23	SEG20	-2504	790	55	COM29	-2504	-3322	87	V2	1625	-4119
24	SEG19	-2504	665	56	COM30	-2504	-3447	88	V1	1750	-4119
25	SEG18	-2504	540	57	COM31	-2504	-3572	89	COM24	2504	-3822
26	SEG17	-2504	415	58	COM32	-2504	-3697	90	COM23	2504	-3697
27	SEG16	-2504	290	59	COM33	-2504	-3822	91	COM22	2504	-3572
28	SEG15	-2504	165	60	VDD	-1750	-4119	92	COM21	2504	-3447
29	SEG14	-2504	40	61	OSC2	-1625	-4119	93	COM20	2504	-3322
30	SEG13	-2504	-84	62	OSC1	-1500	-4119	94	COM19	2504	-3197
31	SEG12	-2504	-209	63	RESET	-1375	-4119	95	COM18	2504	-3072
32	SEG11	-2504	-334	64	TEST2	-1250	-4119	96	COM17	2504	-2947

Table 1. Pad Location (Continued)

Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y	Pad No.	Pad Name	Coordinate X	Coordinate Y
97	COM8	2504	-2822	130	SEG96	2504	1415	163	SEG63	312	4119
98	COM7	2504	-2697	131	SEG95	2504	1540	164	SEG62	187	4119
99	COM6	2504	-2572	132	SEG94	2504	1665	165	SEG61	62	4119
100	COM5	2504	-2447	133	SEG93	2504	1790	166	SEG60	-62	4119
101	COM4	2504	-2322	134	SEG92	2504	1915	167	SEG59	-187	4119
102	COM3	2504	-2197	135	SEG91	2504	2040	168	SEG58	-312	4119
103	COM2	2504	-2072	136	SEG90	2504	2165	169	SEG57	-437	4119
104	COM1	2504	-1947	137	SEG89	2504	2290	170	SEG56	-562	4119
105	COM0	2504	-1822	138	SEG88	2504	2415	171	SEG55	-687	4119
106	SEG120	2504	-1584	139	SEG87	2504	2540	172	SEG54	-812	4119
107	SEG119	2504	-1459	140	SEG86	2504	2665	173	SEG53	-937	4119
108	SEG118	2504	-1334	141	SEG85	2504	2790	174	SEG52	-1062	4119
109	SEG117	2504	-1209	142	SEG84	2504	2915	175	SEG51	-1187	4119
110	SEG116	2504	-1084	143	SEG83	2504	3040	176	SEG50	-1312	4119
111	SEG115	2504	-959	144	SEG82	2504	3165	177	SEG49	-1437	4119
112	SEG114	2504	-834	145	SEG81	2504	3290	178	SEG48	-1562	4119
113	SEG113	2504	-709	146	SEG80	2504	3415	179	SEG47	-1687	4119
114	SEG112	2504	-584	147	SEG79	2504	3540	180	SEG46	-1812	4119
115	SEG111	2504	-459	148	SEG78	2187	4119	181	SEG45	-1937	4119
116	SEG110	2504	-334	149	SEG77	2062	4119	182	SEG44	-2062	4119
117	SEG109	2504	-209	150	SEG76	1937	4119	183	SEG43	-2187	4119
118	SEG108	2504	-84	151	SEG75	1812	4119				
119	SEG107	2504	40	152	SEG74	1687	4119				
120	SEG106	2504	165	153	SEG73	1562	4119				
121	SEG105	2504	290	154	SEG72	1437	4119				
122	SEG104	2504	415	155	SEG71	1312	4119				
123	SEG103	2504	540	156	SEG70	1187	4119				
124	SEG102	2504	665	157	SEG69	1062	4119				
125	SEG101	2504	790	158	SEG68	937	4119				
126	SEG100	2504	915	159	SEG67	812	4119				
127	SEG99	2504	1040	160	SEG66	687	4119				
128	SEG98	2504	1165	161	SEG65	562	4119				
129	SEG97	2504	1290	162	SEG64	437	4119				

PAD DESCRIPTION

Table 2. Pad Description

Pad (No)	Input/ Output	Name	Description	Interface
VDD (60)	–	Power supply	For logical circuit (+3V, +5V)	Power supply
VSS1, VSS2 (66, 81)			0V (GND)	
V1-V5 (88-84)			Bias voltage level for LCD driving	
Vci (78)	Input		Input voltage to the voltage converter to generate LCD drive voltage (Vci = 1.0 - 4.5V).	
SEG1-SEG120 (1-42, 106-183)	Output	Segment output	Segment signal output for LCD drive	LCD
COM0-COM33 (105-89, 43-59)	Output	Common output	Common signal output for LCD drive	LCD
OSC1, OSC2 (61, 62)	Input (OSC1), Output (OSC2)	Oscillator	When use internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1.	External resistor/oscillator (OSC1)
C1,C2 (80, 79)	Input	External capacitance input	To use the voltage converter (2 times/3 times), these pins must be connected to the external capacitance.	External capacitance
RESET (63)	Input	Reset pin	Initialized to low	–
TEST1 (65)	Input	Test pin	When TEST1 = "High", Test mode When TEST1 = "Low", Normal operation mode This pin must be set to V_{SS}	–
V5OUT2 (82)	Output	Two times converter output	The value of Vci is converted two times. To use three times converter, the same capacitance as that of C1-C2 should be connected here.	V5 capacitance
V5OUT3 (83)		Three times converter output	The value of Vci is converted three times.	V5
TEST2 (64)	Input	Test pin	When TEST2 = "High" : Normal mode When TEST2 = "Low": Test mode This pin must be set to V_{DD}	–
RS (67)	Input	Register select	Register selection input In RS = "High", Data register is selected. In RS = "Low", Instruction register is selected.	MPU

Table 2. Pad Description (Continued)

Pad (No)	Input/ Output	Name	Description	Interface
RW (68)	Input	Read/write	Read/write selection input. In RW= "High", read operation. When RW = "Low", write operation.	MPU
E (69)	Input	Read/write enable	Read/write enable signal.	MPU
DB0-DB3 (70-73)	Input Output	Data bus 0-7	In 8-bit bus mode, used as low order bi-directional data bus. During 4-bit bus mode, open these pins.	MPU
DB4-DB7 (74-77)			In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for busy flag output.	MPU

FUNCTION DESCRIPTION

SYSTEM INTERFACE

This chip has all two kinds interface type with MPU : 4-bit bus and 8-bit bus. 4-bit bus and 8-bit bus is selected by DL bit in the instruction register. During read or write operation, two 8-bit registers are used. one is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.

Hence, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode.

RS	R/W	Operation
0	0	Instruction write operation (MPU writes instruction code into IR)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	Data write operation (MPU writes data into DR)
1	1	Data read operation (MPU reads data from DR)

BUSY FLAG (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not high.

DISPLAY DATA RAM (DDRAM)

DDRAM stores display data of maximum 96 x 8 bits (96 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (refer to Figure 1.)

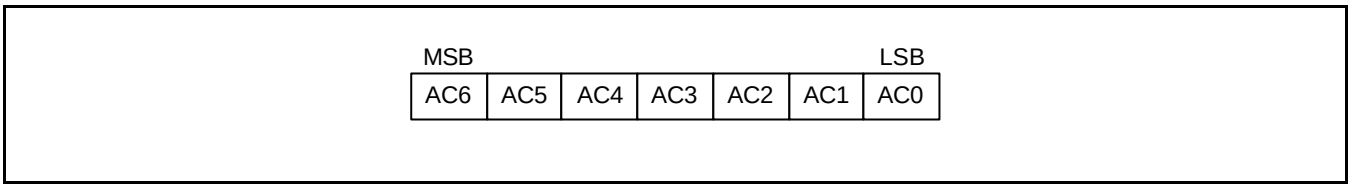


Figure 1. DDRAM Address

5-dot 2-line Display

In case of 2-line display with 5-dot font, the address range of DDRAM is 00H-2FH, 40H-6FH. (refer to Figure 2)

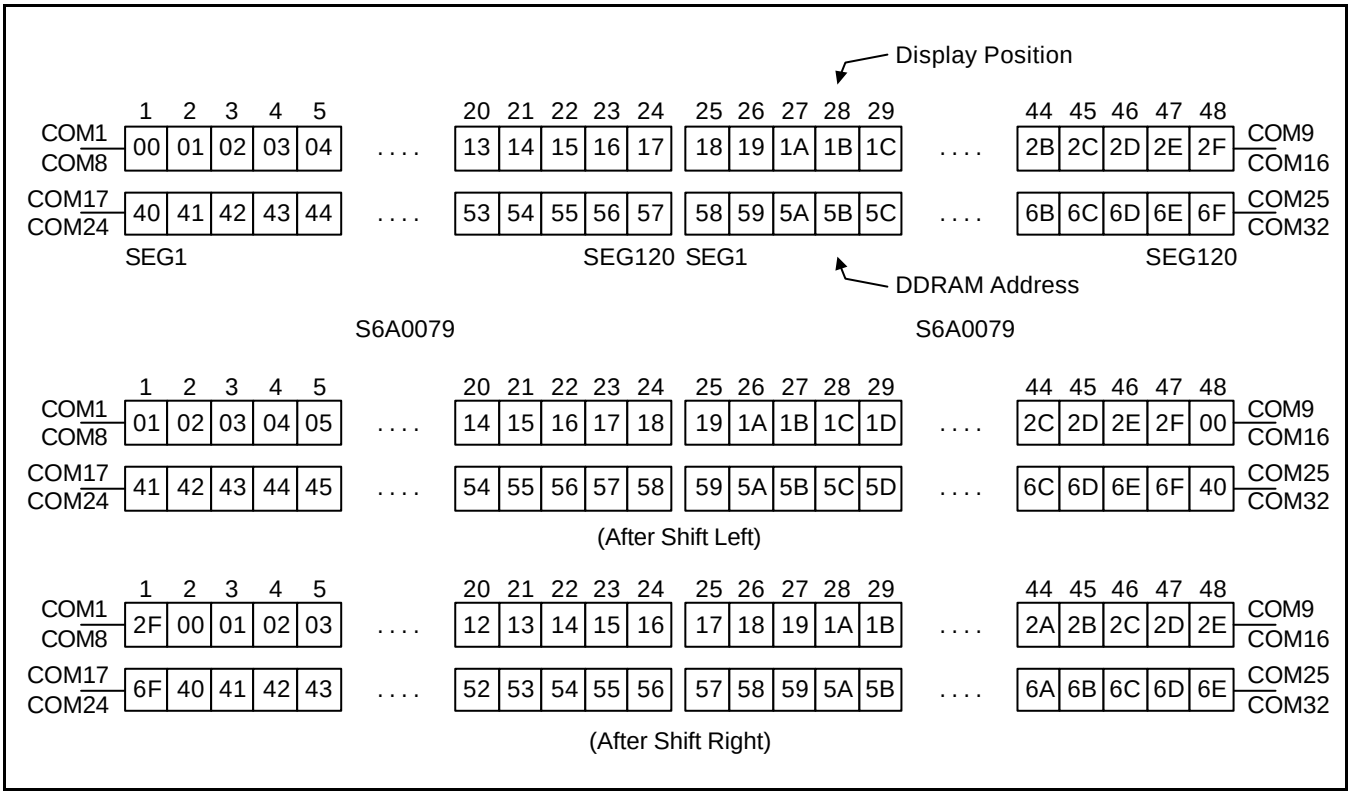


Figure 2. 2-line X 48ch. Display (5-dot Font Width)

5-dot 4-line Display

In case of 4-line display with 5-dot font, the address range of DDRAM is 00H-17H, 20H-37H, 40H-57H, 60H-77H. (refer to Figure 3)

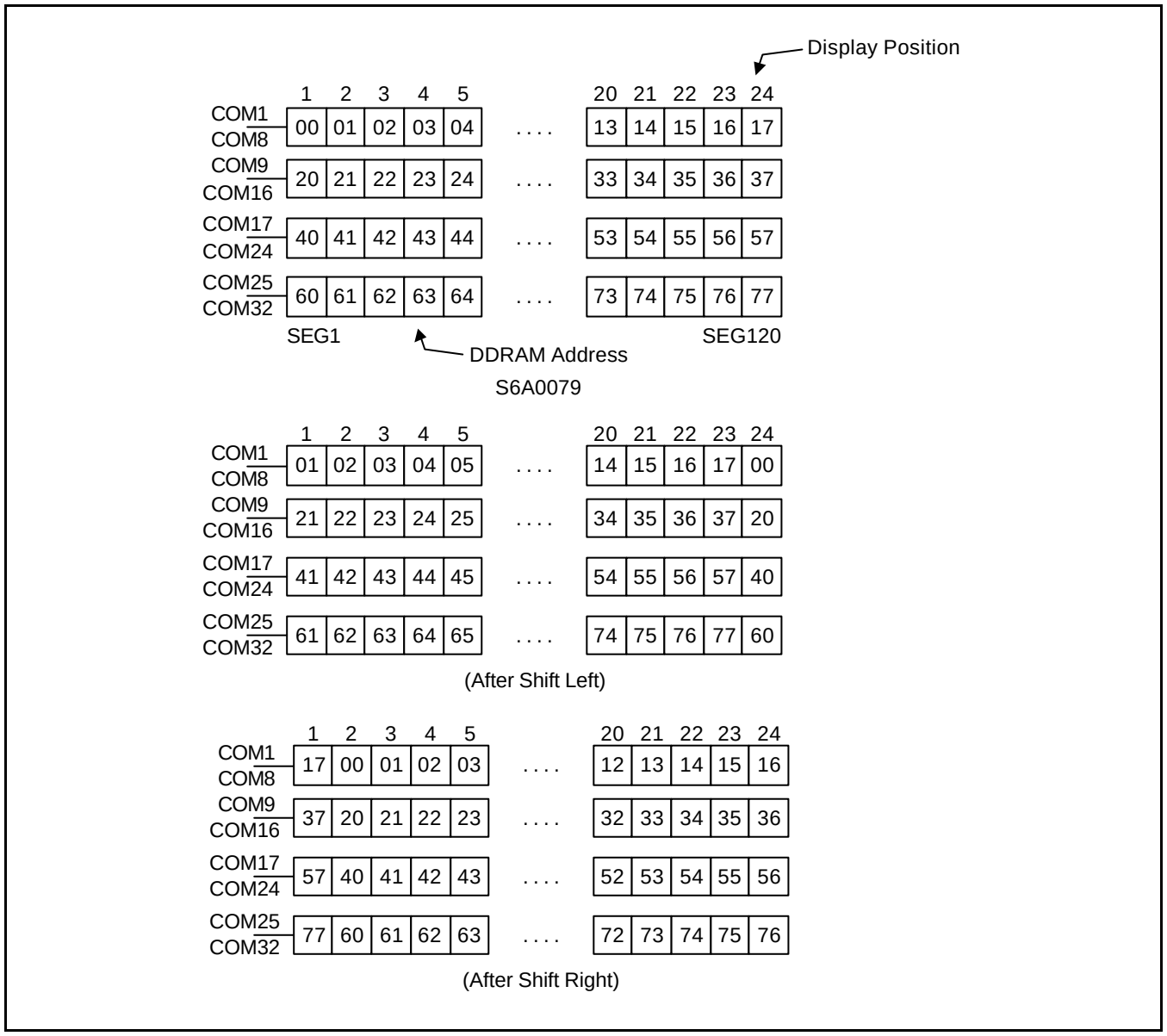


Figure 3. 4-line X 24ch. Display (5-dot Font Width)

TIMING GENERATION CIRCUIT

Timing generation circuit generates clock signals for the internal operations.

ADDRESS COUNTER (AC)

Address Counter(AC) stores DDRAM/CGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0 - DB6.

CURSOR/BLINK CONTROL CIRCUIT

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

LCD DRIVER CIRCUIT

LCD Driver circuit has 34 common and 120 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 120-bit segment latch serially, which is stored to 120-bit shift latch. When each common is selected by 34-bit common register, segment data also output through segment driver from 120-bit segment latch. In case of 2-line or 4-line mode, COM0-COM33 have 1/33 duty ratio. COM0 (COM33) makes the data of CGRAM (Icon RAM) enable to display icons.

CGROM (CHARACTER GENERATOR ROM)

CGROM has 5 X 8 dots 240 characters pattern.

CGRAM (Character Generator RAM)

5 x 8 Dot Character Pattern

By writing font data to CGRAM, user defined character can be used. (refer to Table 4) pattern 7 and pattern 8 to CGRAM can be used in common by CGRAM and IconRAM. But CGRAM and IconRAM is used exclusively to pattern 7 or pattern 8 of CGRAM. CGRAM has up to 5 X 8-dot 6 - 8 characters.

Table 4. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM Address			CGRAM Data								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	x	x	x	0	1	1	1	0	Pattern 1
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	
0	0	0	0	x	1	1	0	1	1	0	0	0	0	x	x	x	0	1	1	1	0	Pattern 7
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	0	
											0	1	1				1	0	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				0	1	1	1	1	
											1	1	1				0	0	0	0	0	
0	0	0	0	x	1	1	1	1	1	1	0	0	0	x	x	x	1	0	0	0	1	Pattern 8
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

CGRAM (ICON RAM)

CGRAM (Icon RAM) has segment control data and segment pattern data. COM0(COM33) makes the data of CGRAM (Icon RAM) enable to display icons. Its lower 5-bit are pattern data. (refer to Table 5 and Figure 4)

Table 5. Relationship Between CGRAM (Icon RAM) Address and Display Pattern

CGRAM Address						CGRAM Data Display Pattern								
						5-Dot Font Width								
A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
1	1	0	0	0	0	X	X	X	S76	S77	S78	S79	S80	CGRAM pattern 7
1	1	0	0	0	1	X	X	X	S71	S72	S73	S74	S75	
1	1	0	0	1	0	X	X	X	S66	S67	S68	S69	S70	
1	1	0	0	1	1	X	X	X	S61	S62	S63	S64	S65	
1	1	0	1	0	0	X	X	X	S56	S57	S58	S59	S60	
1	1	0	1	0	1	X	X	X	S51	S52	S53	S54	S55	
1	1	0	1	1	0	X	X	X	S46	S47	S48	S49	S50	
1	1	0	1	1	1	X	X	X	S41	S42	S43	S44	S45	
1	1	1	0	0	0	X	X	X	S36	S37	S38	S39	S40	CGRAM pattern 8
1	1	1	0	0	1	X	X	X	S31	S32	S33	S34	S35	
1	1	1	0	1	0	X	X	X	S26	S27	S28	S29	S30	
1	1	1	0	1	1	X	X	X	S21	S22	S23	S24	S25	
1	1	1	1	0	0	X	X	X	S16	S17	S18	S19	S20	
1	1	1	1	0	1	X	X	X	S11	S12	S13	S14	S15	
1	1	1	1	1	0	X	X	X	S6	S7	S8	S9	S10	
1	1	1	1	1	1	X	X	X	S1	S2	S3	S4	S5	

NOTES:

1. S1 - S80: Icon pattern ON/OFF in 5-dot font width.
2. "X": Don't care

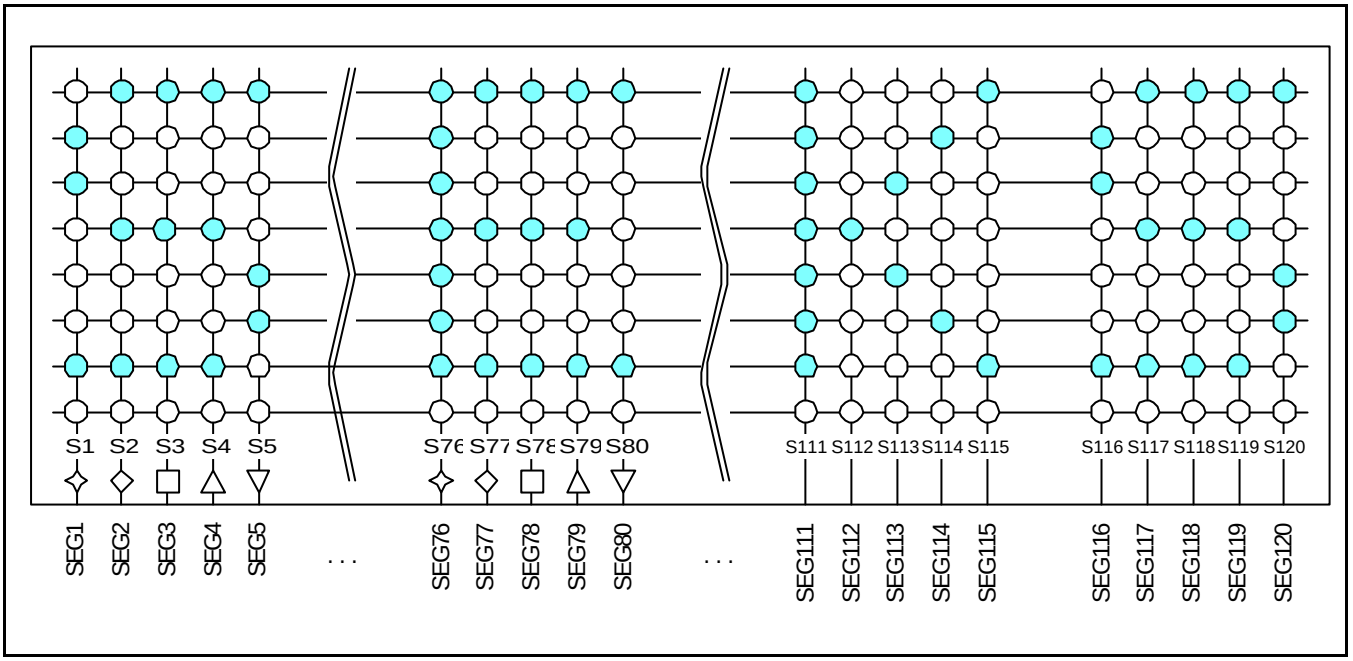


Figure 4. Relationship between CGRAM (Icon RAM) and Segment Display

INSTRUCTION DESCRIPTION

OUTLINE

To overcome the speed difference between internal clock of S6A0079 and MPU clock, S6A0079 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. (refer to Table 6) Instruction can be divided largely four kinds,

— S6A0079 function set instructions (set display methods, set data length, etc.)

— Address set instructions to internal RAM

— Data transfer instructions with internal RAM

— Others

The address of internal RAM is automatically increased or decreased by 1.

NOTE: During internal operation, Busy Flag (DB7) is read High. Busy Flag check must precede the next instruction. When you make a MPU program with checking the Busy Flag (DB7), it must be necessary 1/2 fosc for executing the next instruction by falling E signal after the Busy Flag (DB7) goes to "Low".

INSTRUCTION DESCRIPTION

Table 6. Instruction Set

Instruction	Instruction Code										Description	Execution Time (fosc = 270kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.	1.53ms
Return home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction. I/D = "1": increment, I/D = "0": decrement and display shift enable bit. S = "1": make entire display shift of all lines during DDRAM write. S = "0": display shift disable	39µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off D = "1": display on, D = "0": display off, C = "1": cursor on, C = "0": cursor off, B = "1": blink on, B = "0": blink off.	39µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	X	X	Cursor or display shift. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left.	39µs
Function set	0	0	0	0	1	DL	N	X	X	X	Set interface data length (DL = "1": 8-bit, DL = "0": 4-bit), numbers of display line when (N = "1": 4-line, N = "0": 2-line).	39µs
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39µs
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39µs

Table 6. Instruction Set (Continued)

Instruction	Instruction Code										Description	Execution Time (fosc = 270kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Read busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can be known whether during internal operation or not by reading BF. The contents of address counter can also be read. BF = "1": busy state, BF = "0": ready state.	0µs
Write data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43µs
Read data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43µs

NOTES:

1. When an MPU program with busy flag (DB7) checking is made, 1/2 fosc is necessary for executing the next instruction by the "E" signal after the busy flag (DB7) goes to "Low".
2. "X": Don' t care.

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, hence, bring the cursor to the left edge on first line of the display. Entry mode is set to increment mode (I/D = "1")

Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

I/D: Increment/decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
- CGRAM operates the same as DDRAM, when read from or write to CGRAM.

When S = "High", after DDRAM write, the entire display of all lines is shifted to the right (I/D = "0")or to the left (I/D = "1") but it will seem as if the cursor does not move. When S = "Low", or DDRAM read, or CGRAM read/write operation, shift of entire display is not performed.

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1bit register.

D: Display ON/OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

C: Cursor ON/OFF control bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON/OFF control bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 270kHz frequency, blinking has 370 ms interval.
When B = "Low", blink is off.

Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data (refer to Table 7). During 2-line mode display, cursor moves to the 2nd line after 48th digit of 1st line. In 4-line mode, cursor moves to the next line, only after every 24th digit of the current line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

Table 7. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, address counter is decreased by 1
0	1	Shift cursor to the right, address counter is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	X	X	X

DL: Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
In 4-bit bus mode, it is required to transfer 4-bit data by two times.

N: Display line number control bit
When N = "Low", it means 2-line display mode.
When N = "High", 4-line display mode is set.

Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU.

In 2-line display mode (N = 0) DDRAM address in the 1st line is from "00H" to "2FH", and DDRAM address in the 2nd line is from "40H to 6FH".
In 4-line display mode (N = 1), DDRAM address is from "00H to "17H" in the 1st line, from "20H" to "37H" in the 2nd line, from "40H" to "57H" in the 3rd line and from "60H" to "77H" in the 4th line.

Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether S6A0079 is in internal operation or not. If the resultant BF is high, the internal operation is in progress and you have to wait until BF to be low, which by then the next instruction can be performed. In this instruction you can read the value of address counter.

Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM. The selection of RAM from DDRAM, CGRAM is set by the previous address set instruction : DDRAM address set, CGRAM address set. RAM set instruction can also determines the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

Read Data From RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, as the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, the correct RAM data can be from the second, but the first data would be incorrect, as there is no time margin to transfer RAM data. In DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, AC is increased/decreased by 1 as in read operation after this. In this time, AC indicates the next address position, but you can read only the previous data can only be read by read instruction.

INTERFACE WITH MPU

S6A0079 can transfer data in bus mode (4-bit or 8-bit) with MPU. Hence, both types of 4 or 8-bit MPU can be used. In case of 4-bit bus mode, data transfer is performed by twice to transfer 1 byte data.

— When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus.
At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by twice. busy flag outputs "High" after the second transfer is ended.

— When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.

INTERFACE WITH MPU IN BUS MODE

Interface with 8-bit MPU

If 8-bit MPU is used, S6A0079 can connect directly with that. In this case, port E, RS, R/W and DB0 to DB7 need to interface each other. Example of timing sequence is shown below.

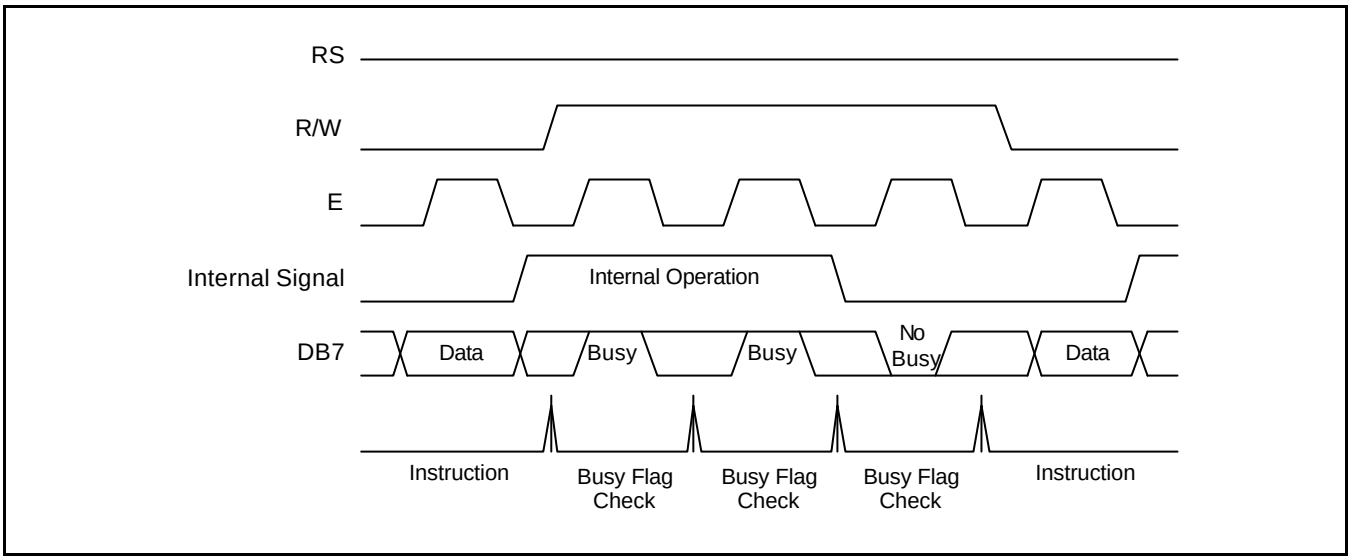


Figure 5. Example of 8-bit Bus Mode Timing Sequence

Interface with 4-bit MPU

If 4-bit MPU is used, S6A0079 can connect directly with this. In this case, port E, RS, R/W and DB4 to DB7 need to interface each other. The transfer is performed by twice. Example of timing sequence is shown below.

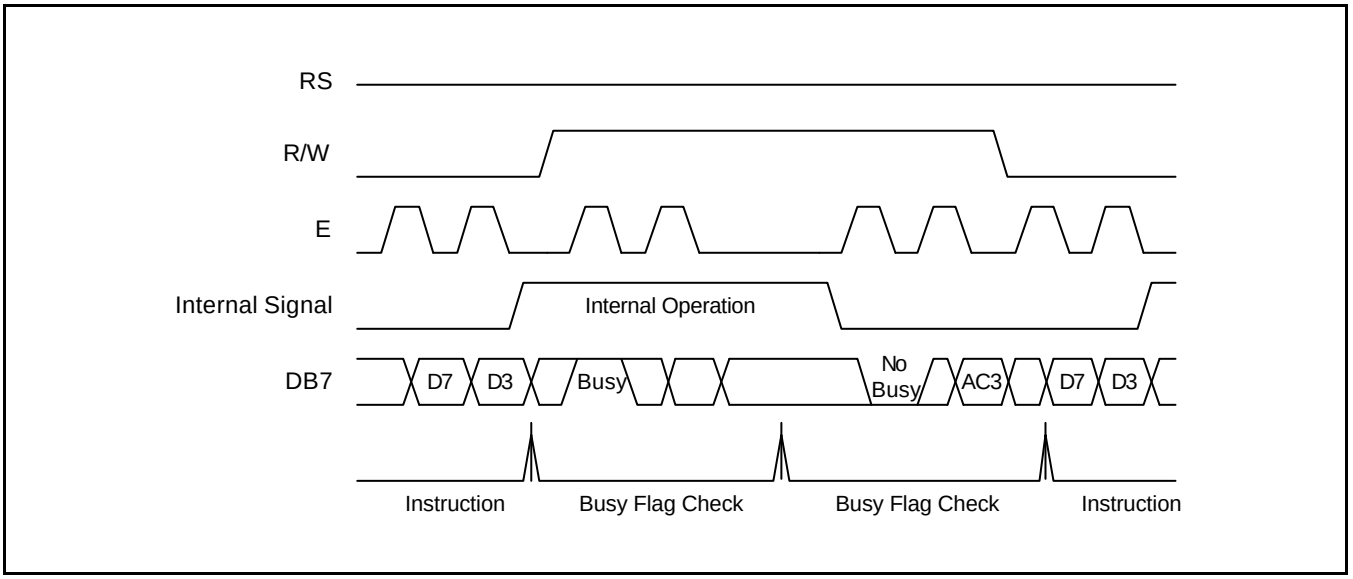
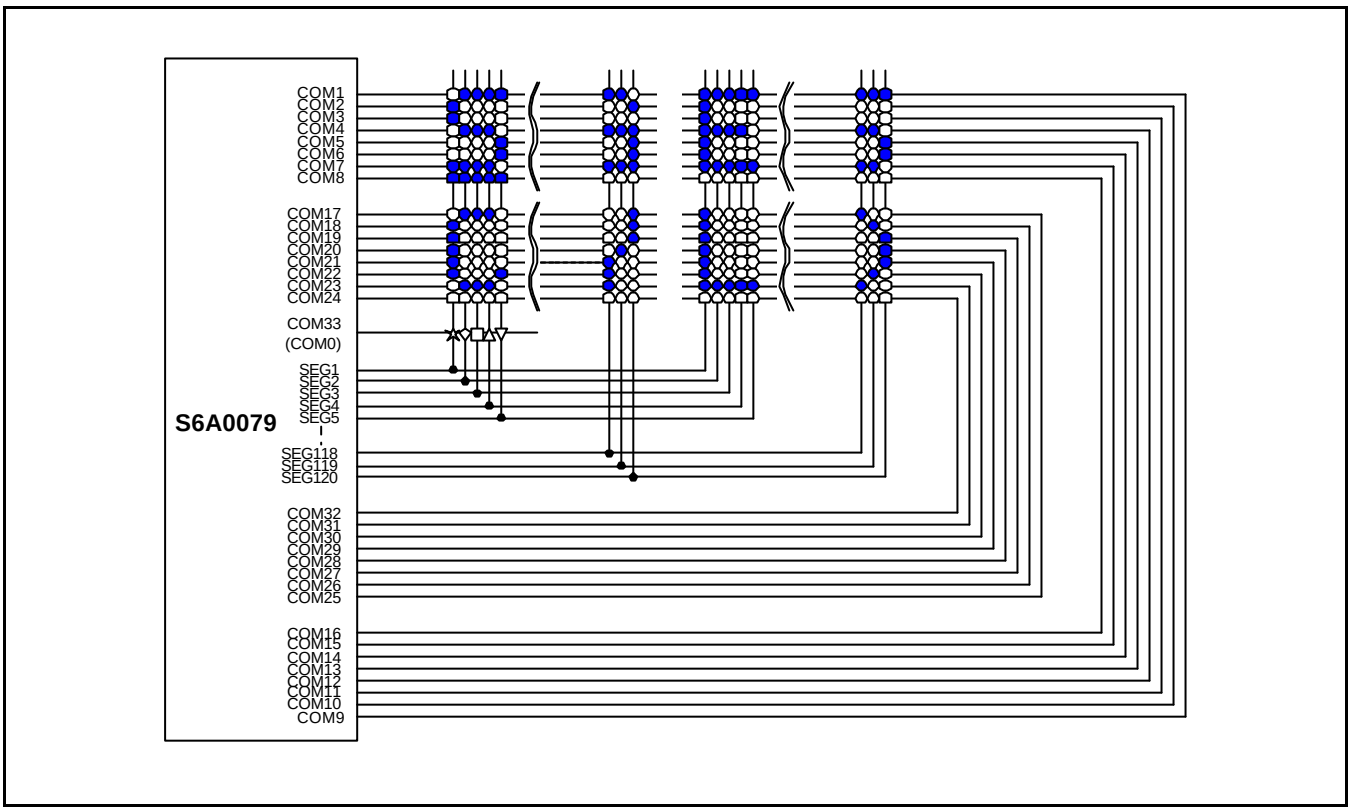


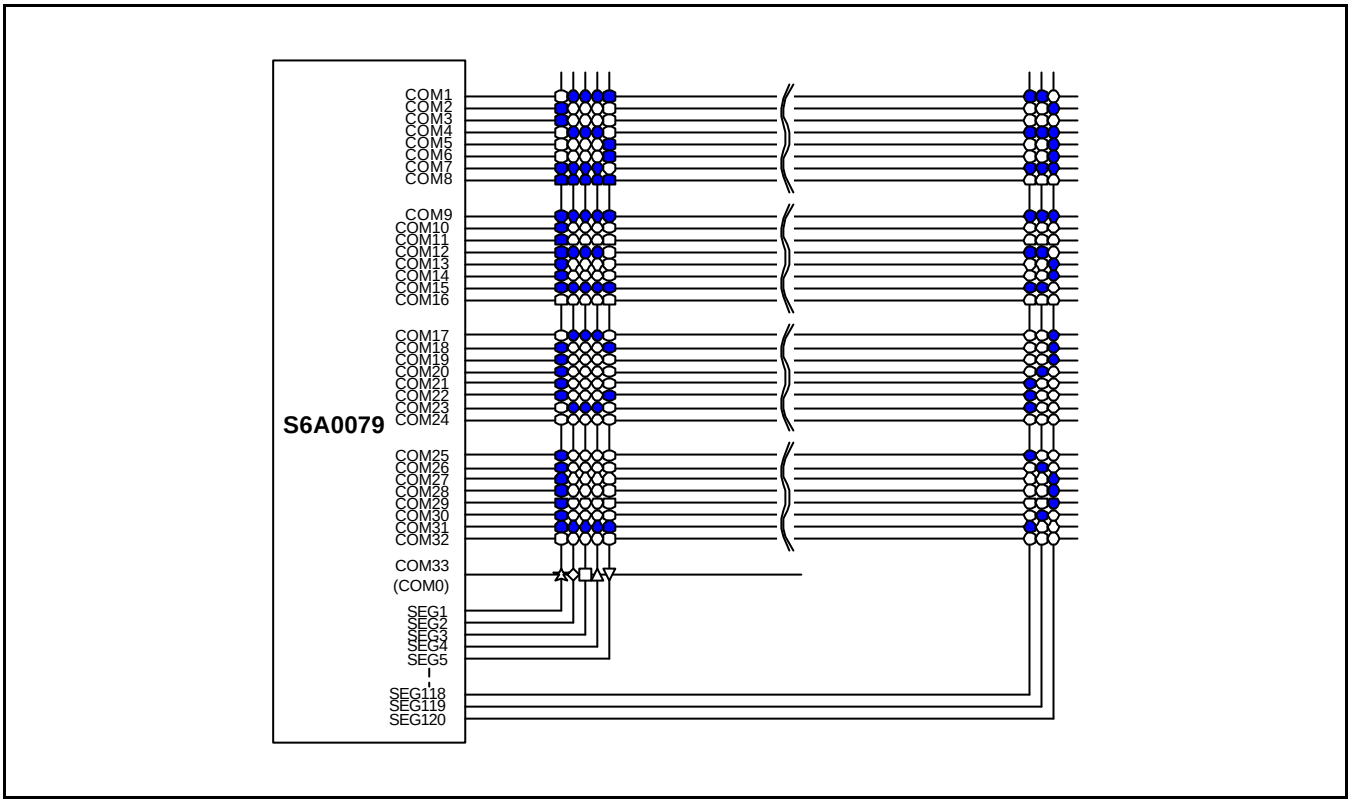
Figure 6. Example of 4-bit Bus Mode Timing Sequence

APPLICATION INFORMATION ACCORDING TO LCD PANEL

LCD Panel: 48 Character x 2-line Format



LCD Panel: 24 Character x 4-line Format



INITIALIZING

INITIALIZING BY INTERNAL RESET CIRCUIT

When the power is turned on, S6A0079 is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High" (busy state) to the end of initialization.

Display Clear Instruction

Write "20H" to all DDRAM

Set Functions Instruction

DL = 1: 8-bit bus mode
N = 0: 2-line display mode

Control Display ON/OFF Instruction

D = 0: Display OFF
C = 0: Cursor OFF
B = 0: Blink OFF

Set Entry Mode Instruction

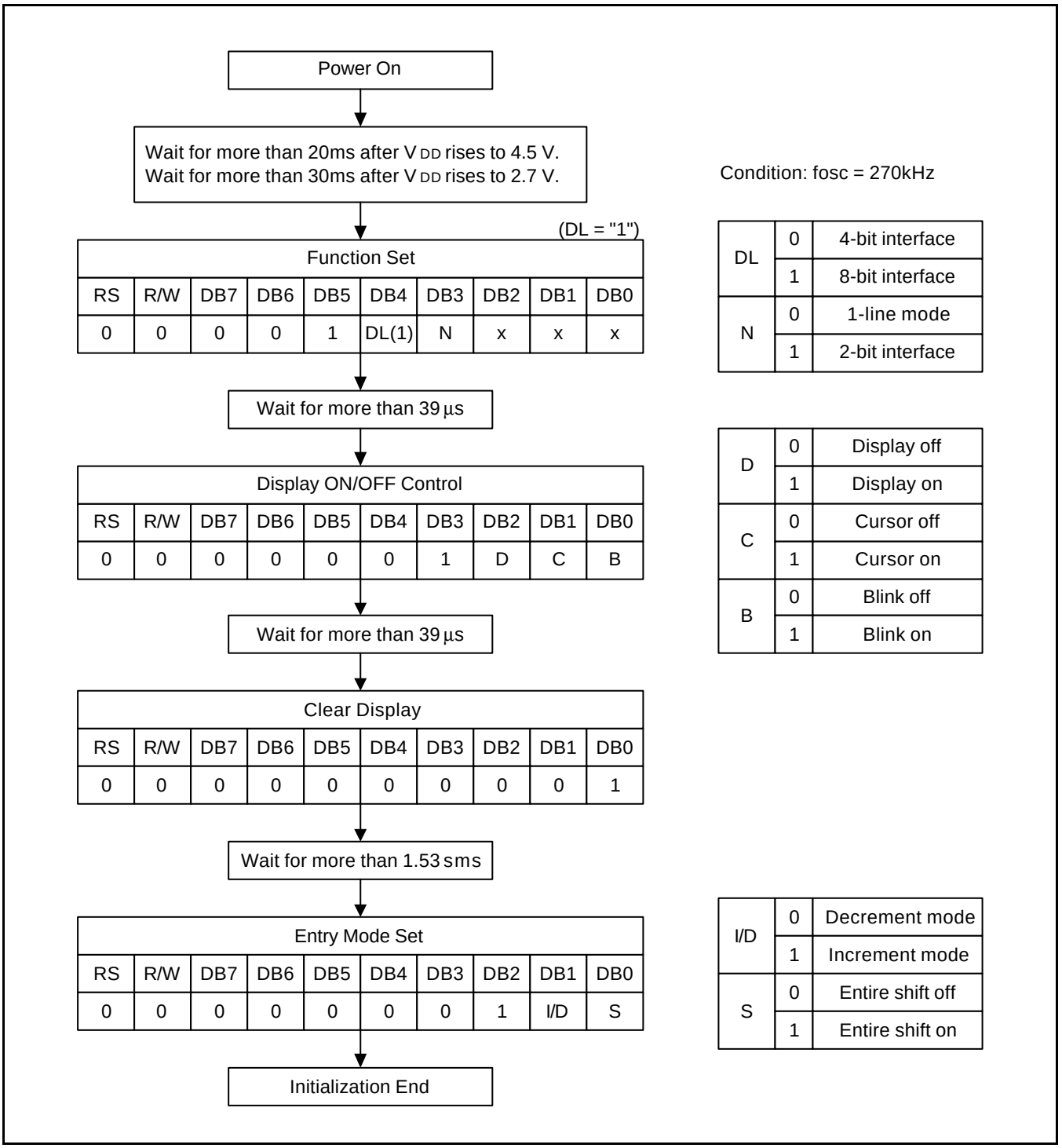
I/D = 1: Increment by 1
S = 0: No entire display shift

INITIALIZING BY HARDWARE RESET INPUT

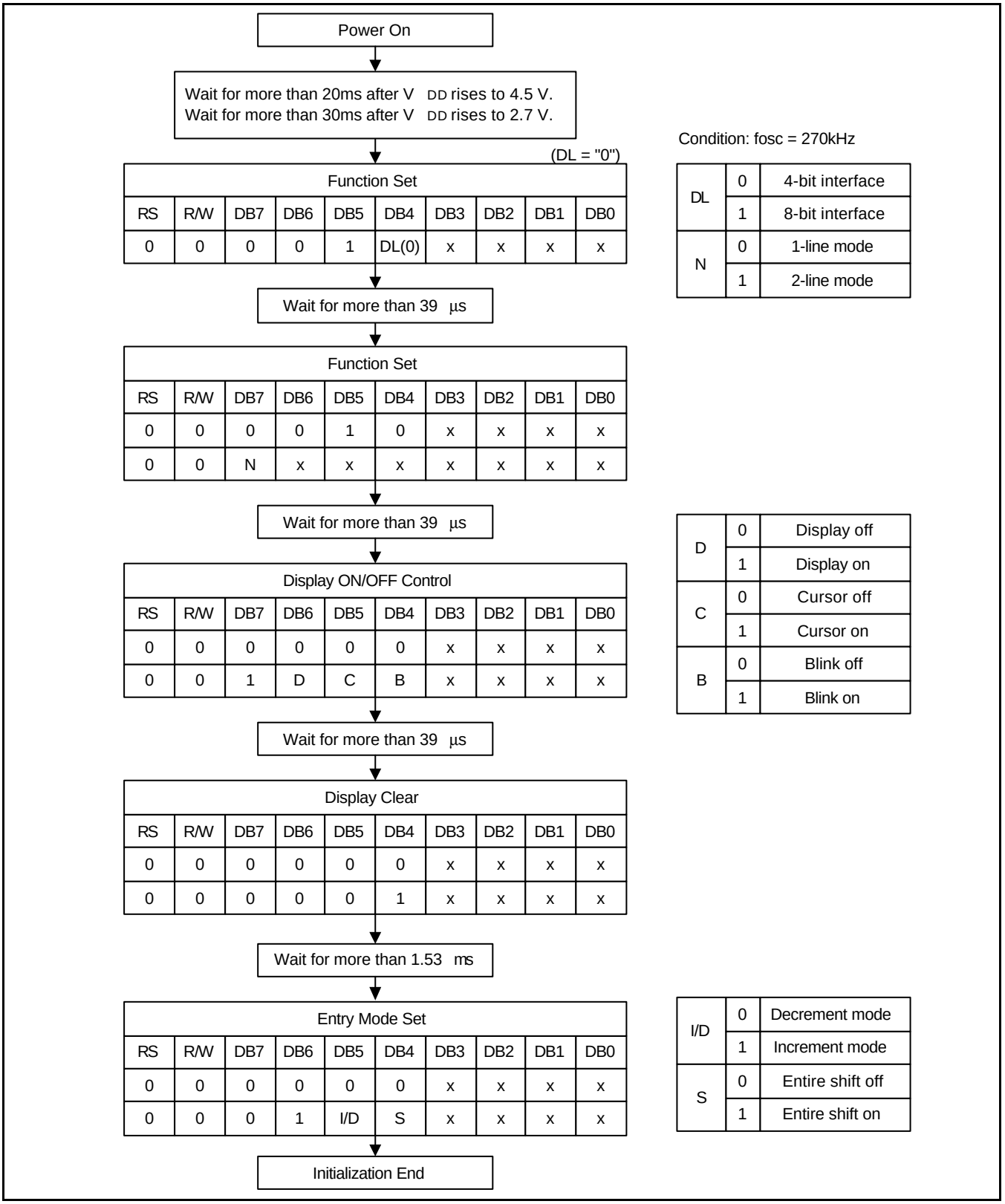
When RESET pin = "Low", S6A0079 can be initialized like the case of power on reset. During the power on reset operation, this pin is ignored.

INITIALIZING BY INSTRUCTION

8-BIT INTERFACE MODE

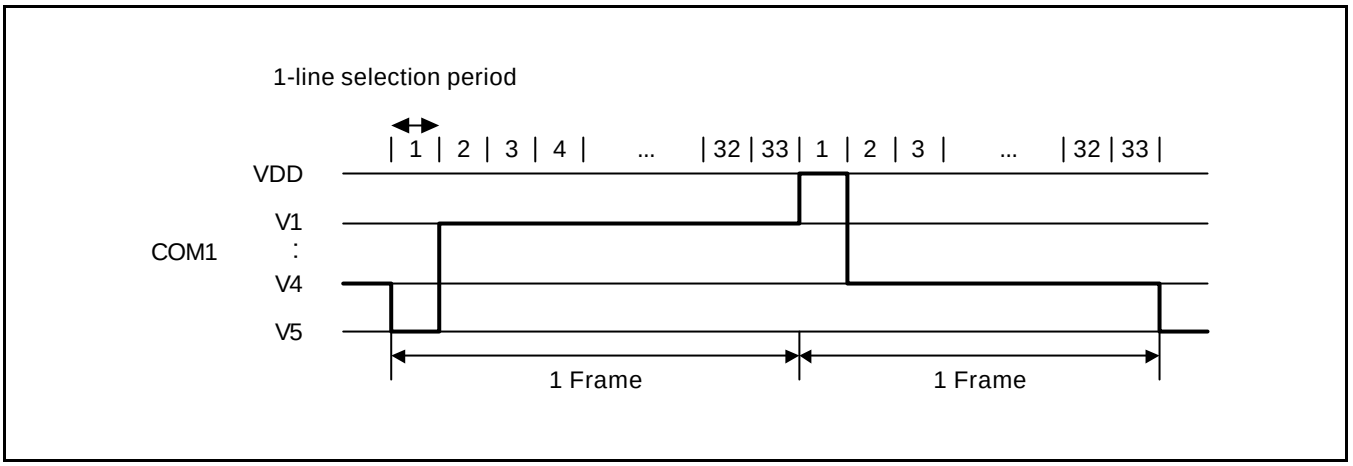


4-BIT INTERFACE MODE



FRAME FREQUENCY

1/33 DUTY CYCLE

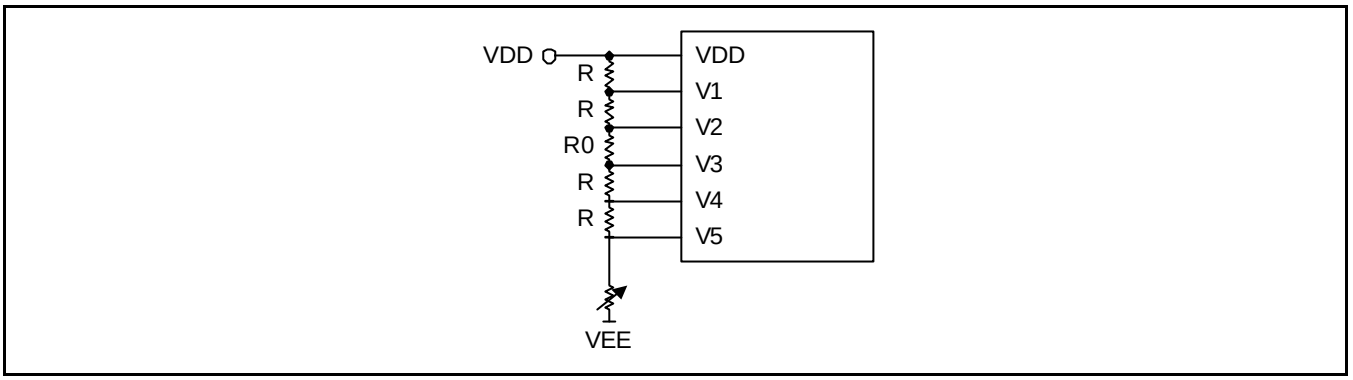


1-line selection period	120 clocks
Frame frequency	68.2Hz

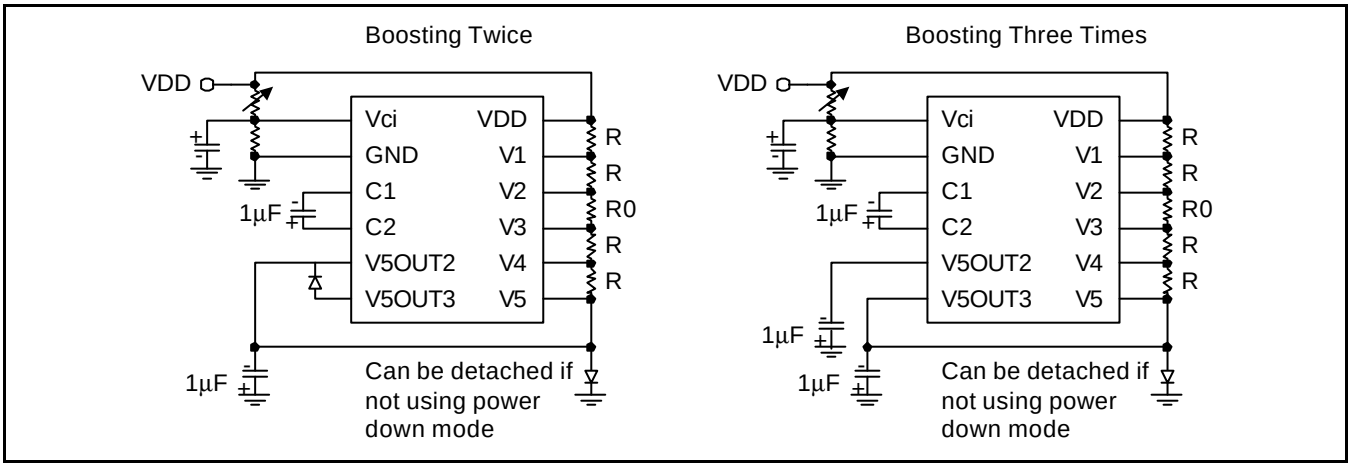
NOTE: f_{OSC} = 270kHz (1 clock = 3.7μs)

POWER SUPPLY FOR DRIVING LCD PANEL

WHEN AN EXTERNAL POWER SUPPLY IS USED



WHEN AN INTERNAL BOOSTER IS USED



NOTES:

1. Boosted output voltage should not exceed the maximum value (13 V) of the LCD driving voltage. Especially, a voltage of over 4.3V should not be input to the reference voltage (Vci) when boosting three times.
2. A voltage of over 5.5V should not be input to the reference voltage (Vci) when boosting twice.
2. The value of resistance, according to the number of lines, duty ratio and the bias, is shown below. (refer to Table 8)

Table 8. Duty Ratio and Power Supply for LCD Driving

Item		Data
Number of lines		2 or 4
Duty ratio		1/33
Bias		1/6.7
Divided resistance	R	R
	R0	2.7R

MAXIMUM ABSOLUTE RATE

Characteristic	Symbol	Value	Unit
Power supply voltage (1)	V_{DD}	-0.3 to +7.0	V
Power supply voltage (2)	V_{LCD}	V_{DD} -15.0 to V_{DD} +0.3	V
Input voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Operating temperature	T_{OPR}	-30 to +85	°C
Storage temperature	T_{STG}	-55 to +125	°C

NOTE: Voltage greater than above may damage to the circuit ($V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, T_A = -30 to +85°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Operating voltage	V_{DD}	–	2.7	–	5.5	V
Supply current	I_{DD}	Internal oscillation or external clock. (V_{DD} = 3.0V, f_{OSC} = 270kHz)	–	0.15	0.3	mA
Input voltage (1) (Except OSC1)	V_{IH1}	–	0.7V_{DD}	–	V_{DD}	–
	V_{IL1}	V_{DD} = 2.7 - 3.0	-0.3	–	0.2V_{DD}	
		V_{DD} = 3.0 - 5.5	-0.3	–	0.6	
Input voltage (2) (OSC1)	V_{IH2}	–	0.7V_{DD}	–	V_{DD}	V
	V_{IL2}	–	–	–	0.2V_{DD}	
Output voltage (1) (DB0 - DB7)	V_{OH1}	I_{OH} = -0.1mA	0.75V_{DD}	–	–	V
	V_{OL1}	I_{OL} = 0.1mA	–	–	0.2V_{DD}	
Output voltage (2) (except DB0 - DB7)	V_{OH2}	I_O = -40µA	0.8V_{DD}	–	–	V
	V_{OL1}	I_O = 40µA	–	–	0.2V_{DD}	
Voltage drop	Vd_{COM}	I_O = ±0.1mA	–	–	1	V
	Vd_{SEG}		-	–	1	
Input leakage current	I_{IL}	V_{IN} = 0V - V_{DD}	-1	–	1	µA
Low input current	I_{IN}	V_{IN} = 0V, V_{DD} = 3V (pull up)	-10	-50	-120	
Internal clock (external Rf)	f_{OSC}	Rf = 91kΩ ±2% (V_{DD} = 5V)	190	270	350	kHz
External clock	f_{EC}	–	125	270	410	kHz
	duty		45	50	55	%
	tr, tf		–	–	0.2	µs
Voltage converter OUT2 (Vci = 4.5V)	V_{OUT2}	T_A = 25°C, C = 1µF, I_{OUT} = 0.25mA, f_{OSC} = 270kHz	-3.0	-4.2	–	V
Voltage converter OUT3 (Vci = 2.7V)	V_{OUT3}		-4.3	-5.1	–	
Voltage converter input	Vci	–	1.0	–	4.5	V
LCD driving voltage	V_{LCD}	V_{DD}-V5 1/6.7 bias	3.0	–	13.0	

AC CHARACTERISTICS

(V_{DD} = 4.5 to 5.5V, T_A = -30 to + 85°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
Write mode (1)	E cycle time	t_C	500	–	–	ns
(refer to Figure 7)	E rise/fall time	t_r, t_f	–	–	20	
	E pulse width (high, low)	t_W	230	–	–	
	R/W and RS setup time	t_{su1}	40	–	–	
	R/W and RS hold time	th1	10	–	–	
	Data setup time	tsu2	60	–	–	
	Data hold time	th2	10	–	–	
Read mode (2)	E cycle time	tc	500	–	–	ns
(refer to Figure 8)	E rise/fall time	tr, tf	–	–	20	
	E pulse width (high, low)	tw	230	–	–	
	R/W and RS setup time	tsu	40	–	–	
	R/W and RS hold time	th	10	–	–	
	Data output delay time	t_D	–	–	160	
	Data hold time	t_{DH}	5	–	–	

(V_{DD} = 2.7 to 4.5V, T_A = -30 to + 85°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
Write mode (3)	E cycle time	tc,	1000	–	–	ns
(refer to Figure 7)	E rise/fall time	tr, tf	–	–	25	
	E pulse width (high, low)	tw	450	–	–	
	R/W and RS setup time	tsu1	60	–	–	
	R/W and RS hold time	th1	20	–	–	
	Data setup time	tsu2	195	–	–	
	Data hold time	th2	10	–	–	
Read mode (4)	E cycle time	tc	1000	–	–	ns
(refer to Figure 8)	E rise/fall time	tr, tf	–	–	25	
	E pulse width (high, low)	tw	450	–	–	
	R/W and RS setup time	tsu	60	–	–	
	R/W and RS hold time	th	20	–	–	
	Data output delay time	t_D	–	–	360	
	Data hold time	t_{DH}	5	–	–	

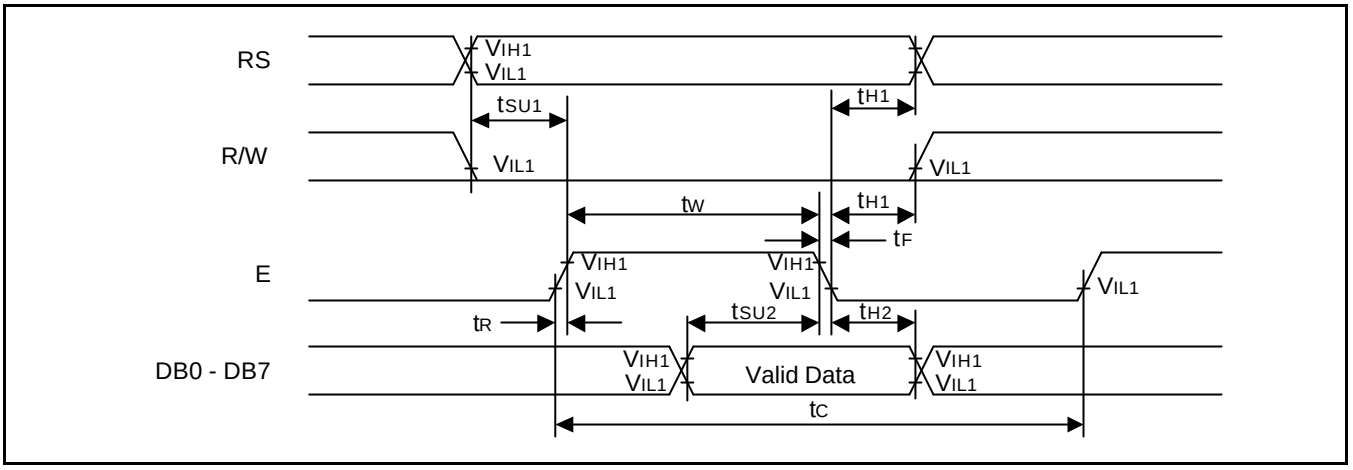


Figure 7. Write Mode

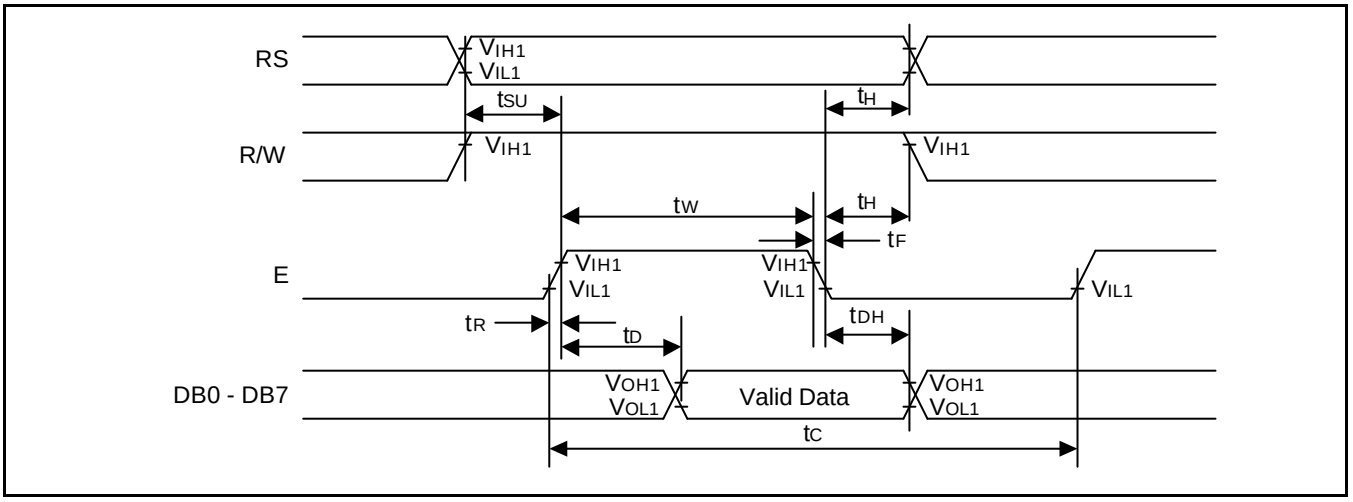


Figure 8. Read Mode

RESET TIMING

(V_{DD} = 2.7 to 5.5V, T_A = -30 to +85°C)

Item	Symbol	Min	Typ	Max	Unit
Reset low level width (refer to Figure 9)	t_{RES}	10	–	–	ms

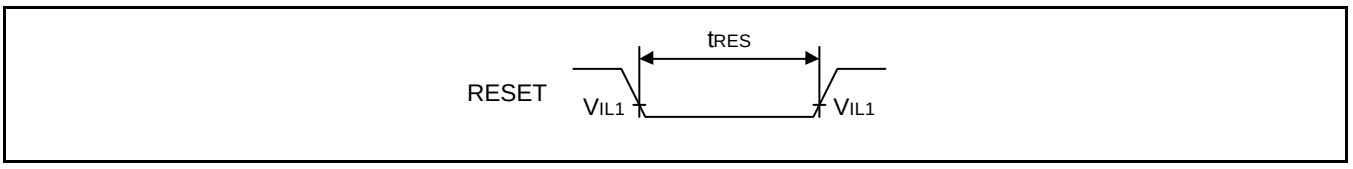


Figure 9. Reset Timing Diagram