HARRIS SEMICONDUCTOR

RFV10N50BE

10A, 500V, Fast Switching N-Channel Enhancement-Mode Power MOSFETs

August 1995

Features

- **10A, 500V**
- **$r_{DS(ON)}$ = 0.480Ω**
- **Very Fast Turn-Off Characteristics**
- **Nanosecond Switching Speeds**
- **Electrostatic Discharge Protected**
- **UIS Rating Curve**
- **SOA is Power Dissipation Limited**
- **High Input Impedance**

Description

The RFV10N50BE is an N-Channel fast switching MOSFET transistor that is designed for switching regulators, inverters and motor drivers. The RFV10N50BE is a monolithic structure incorporating a high voltage, high current MOSFET, a control MOSFET and ESD protection diodes. As indicated in the symbol to the right, the turn-on of the main MOSFET is controlled by Gate 1 (G_1). The control MOSFET, controlled by Gate 2 (G_2), is distributed throughout the structure. Gate 2 provides a very low impedance and inductive path to rapidly discharge the gate of the main MOSFET. Gate 2 affords very fast turn-off (typically less than 25ns) when desired. A separate return connection, Source Kelvin (S_K), is supplied for the gate drive circuit to avoid voltage induced transients from the output circuit during switching. The RFV10N50BE can be operated directly from integrated circuits.

PACKAGE AVAILABILITY

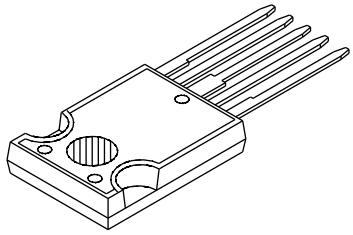
PART NUMBER	PACKAGE	BRAND
RFV10N50BE	TO-247	V10N50BE

NOTE: When ordering use the entire part number.

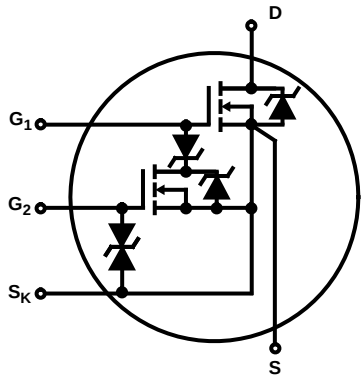
Formerly developmental type TA9881.

Package

JEDEC STYLE 5 LEAD TO-247



Terminal Diagram



Absolute Maximum Ratings $T_C = +25^oC$

			UNITS
Drain Source Voltage	V_{DSS}	500	V
Gate Source Voltage	V_{GS}	+14, -0.3	V
Control FET Gate Source Voltage	V_{GS}	+14, -0.3	V
Electrostatic Discharge Rating, MIL-STD-883, Category B(2)	ESD	2	KV
Drain Current			
RMS Continuous	I_D	10	A
Pulsed Drain Current	I_{DM}	25	A
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Control FET Avalanche Current	I_{AS}	1.5	A
Control FET Single Pulse Avalanche Rating	E_{AS}	50	mJ
Power Dissipation			
$T_C = +25^oC$	P_D	156	W
Derate Above $+25^oC$		1.25	$W/^oC$
Control FET Power Dissipation			
$T_C = +25^oC$	P_D	21	W
Derate Above $+25^oC$		0.17	$W/^oC$
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

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File Number **3377.1**

Electrical Specifications

Case Temperature (T_C) = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		500	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500V, V_{GS} = 0V	T_C = +25°C	-	-	1	µA
			T_C = +125°C	-	-	250	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +12V, V_{GS} = -0.3V		-	-	±500	nA
On Resistance	$r_{DS(ON)}$	I_D = 10A, V_{GS} = 10V		-	-	0.480	Ω
Turn-On Time	t_{ON}	V_{DD} = 250V, I_D = 10A, R_L = 25Ω, V_{GS1} = V_{GS2} = +10V, R_{GS1} = 6.25Ω, R_{GS2} = 20Ω		-	-	75	ns
Turn-On Delay Time	$t_{D(ON)}$			-	20	-	ns
Rise Time	t_R			-	30	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	21	-	ns
Fall Time	t_F			-	5	-	ns
Turn-Off Time	t_{OFF}			-	-	50	ns
Total Gate Charge	Q_{G10}	V_{GS} = 0V to 10V	V_{DD} = 400V, I_D = 10A, R_L = 40Ω	-	145	190	nC
Gate Source Charge	Q_{GS}			-	17	22	nC
Gate Drain (“Miller”) Charge	Q_{GD}			-	57	74	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	3800	-	pF
Output Capacitance	C_{OSS}			-	290	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	75	-	pF
Thermal Resistance	$R_{\theta JC}$	Junction to Case		-	-	0.8	°C/W
Thermal Resistance	$R_{\theta JA}$	Junction to Ambient		-	-	40	°C/W

Control FET Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Static Drain to Source	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.0A	-	1.6	-	Ω
Drain Source Breakdown Voltage	BV_{DSS}	I_D = 1.0mA, V_{GS} = 0V	14	15	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 0.25mA	2	-	4	V
Total Gate Charge	Q_{G10}	I_D = 1.0A, V_{GS} = 10V	-	-	5	nC

Source-Drain Diode Ratings and Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Continuous Source Current	I_S		-	-	10	A
Pulsed Source Current	I_{SM}		-	-	25	A
Forward Voltage	V_{SD}	I_{SD} = 10A, V_{GS} = 0V	-	-	1.4	V
Reverse Recovery Time	t_{RR}	I_{SD} = 10A, V_{GS} = 0V, dI_{SD}/dt = 100A/µs	-	-	750	ns

Typical Performance Curves

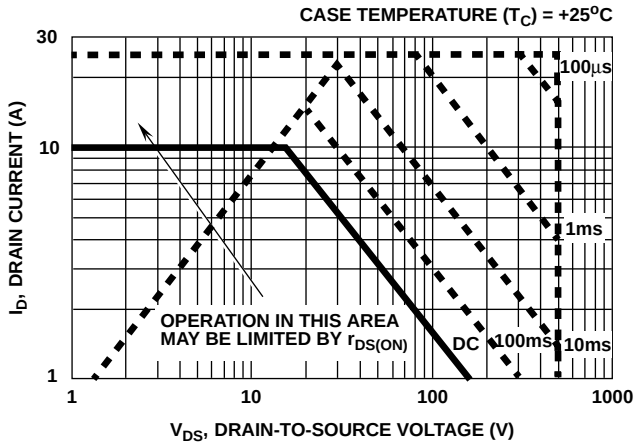


FIGURE 1. SAFE OPERATING AREA CURVE

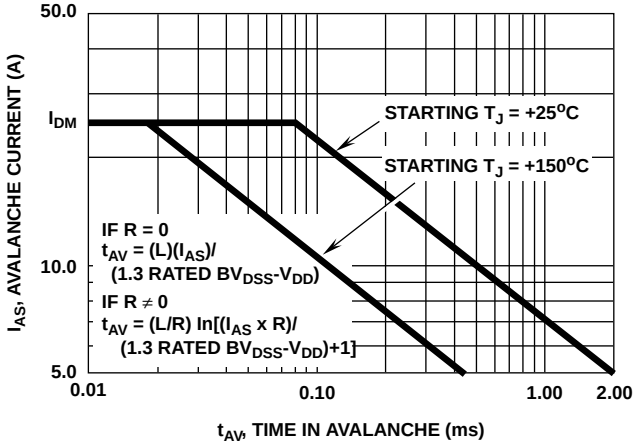


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING

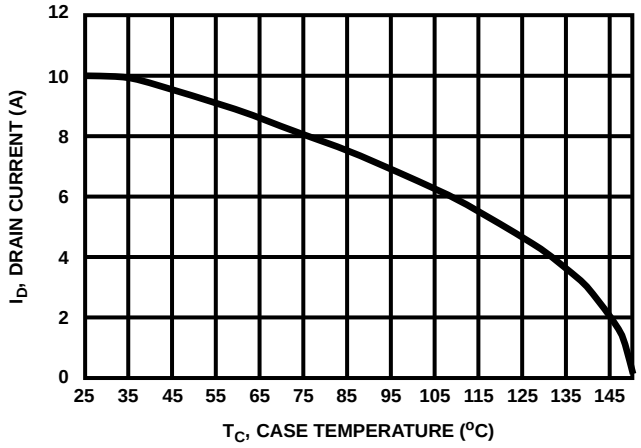


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

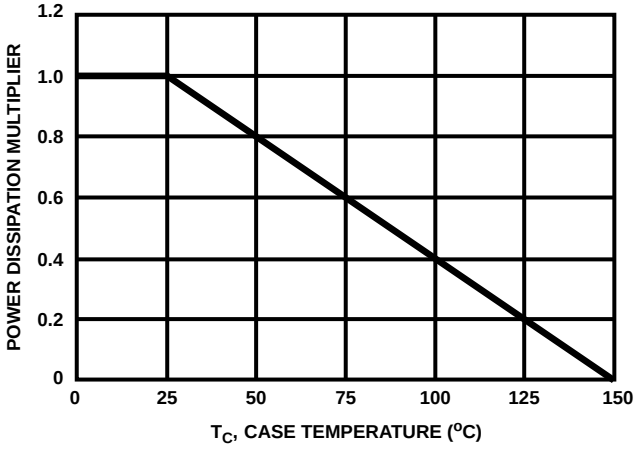


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERTURE DERATING CURVE

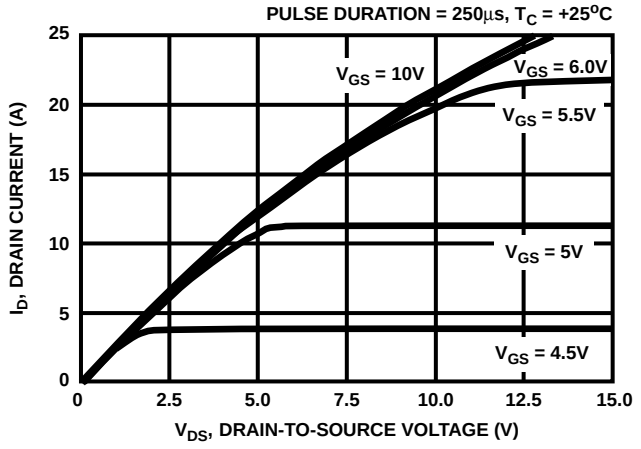


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

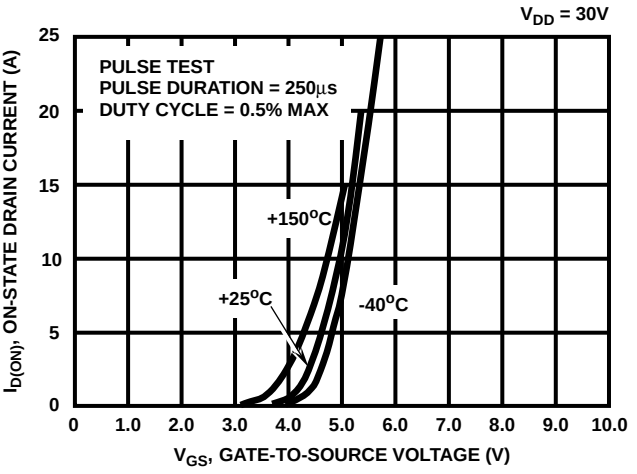


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

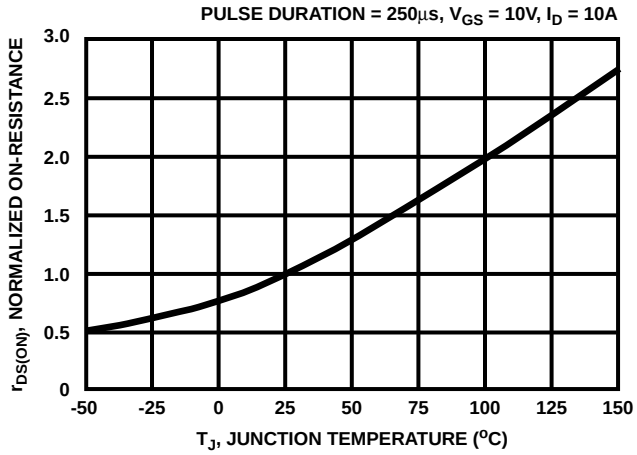


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

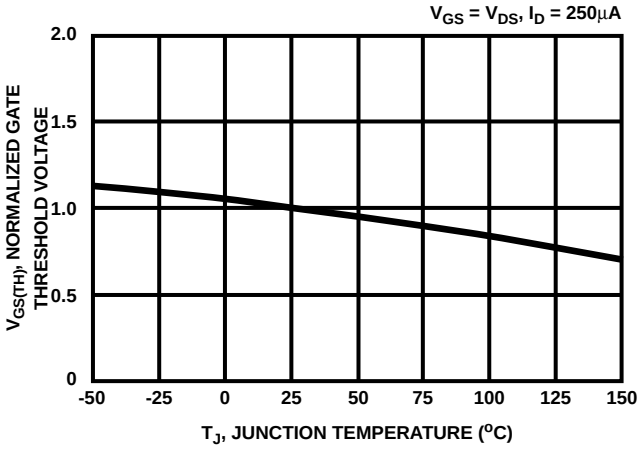


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

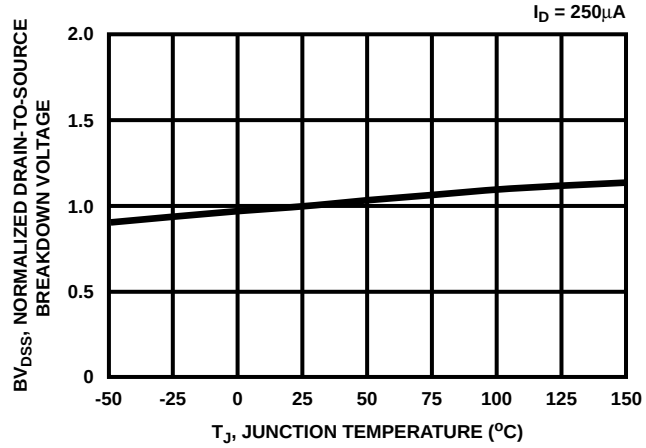


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

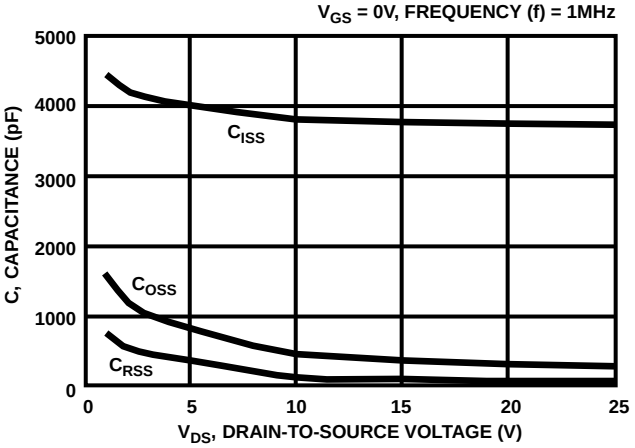


FIGURE 10. TYPICAL CAPACITANCE vs VOLTAGE

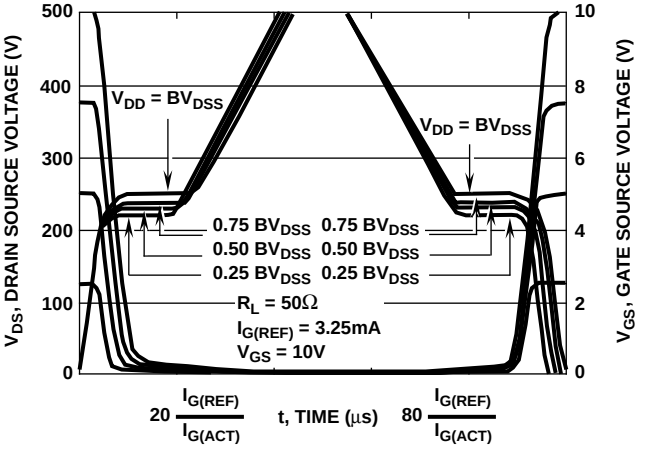


FIGURE 11. TYPICAL SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTES AN7254 AND AN7260

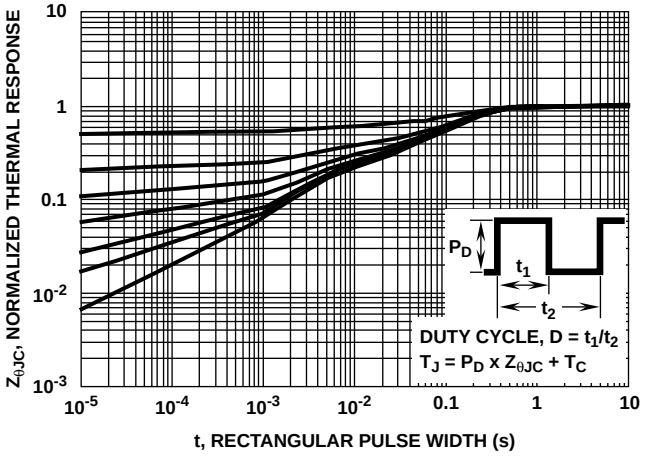


FIGURE 12. MAXIMUM NORMALIZED TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

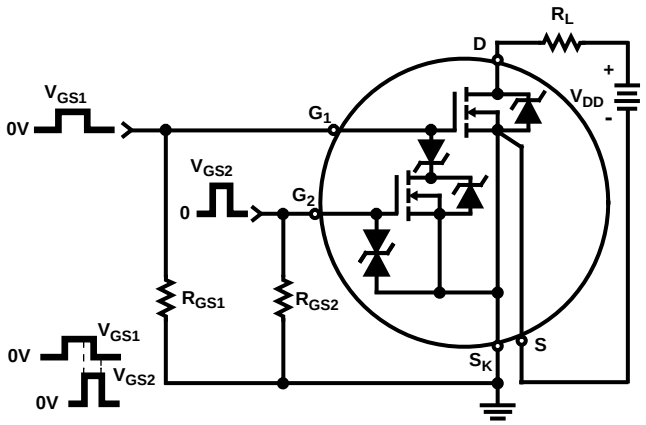


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUITS

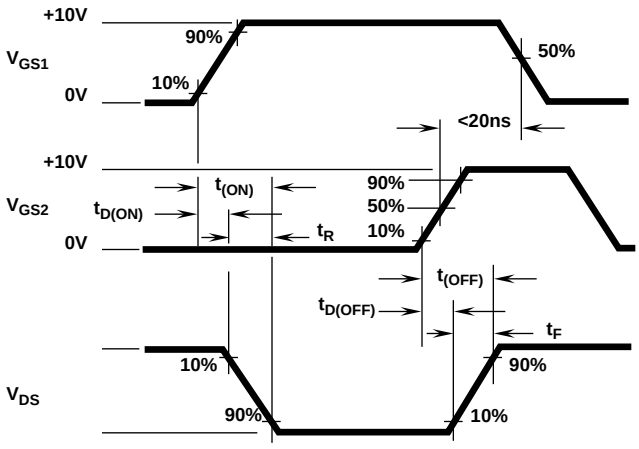


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

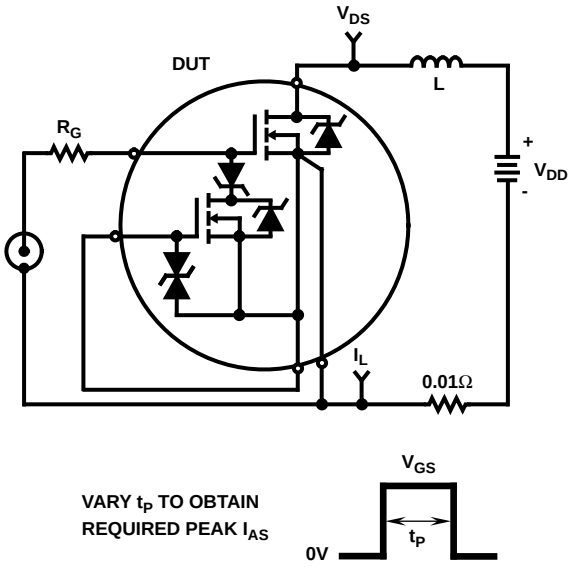


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

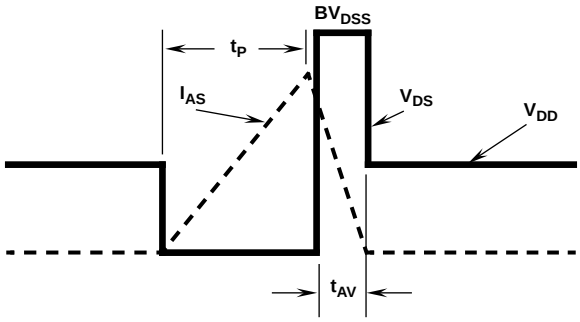
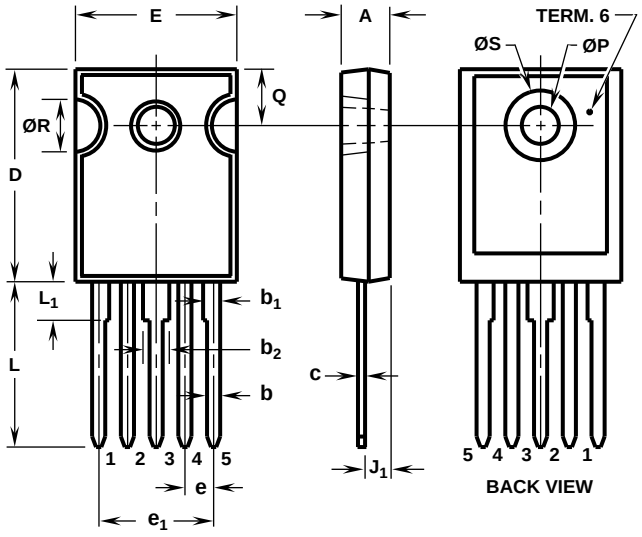


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

Packaging



TO-247

5 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.110 TYP		2.79 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

TERMINAL CONNECTIONS

Lead No. 1	-	Gate 1 (G_1)
Lead No. 2	-	Gate 2 (G_2)
Lead No. 3 and Mounting Flange	-	Drain (D)
Lead No. 4	-	Source Kelvin (S_K)
Lead No. 5	-	Source (S)

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