GUARANTEED LOW SKEW CMOS 20 OUTPUT CLOCK DRIVER/BUFFER

QS5820T

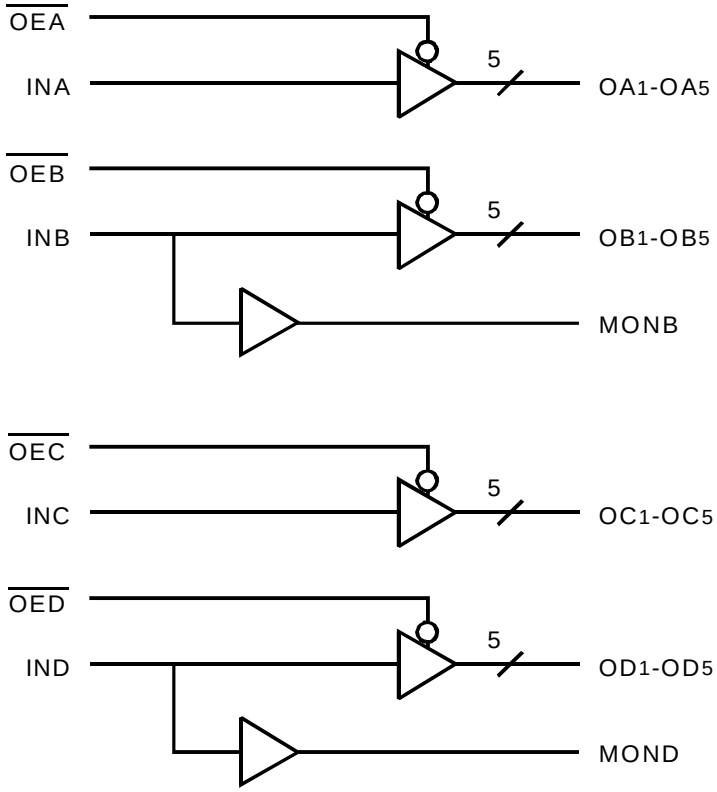
FEATURES:

- 20 output, low skew clock signal buffer
- High drive FCT-type outputs
- Reduced swing TTL outputs for low noise
- Input hysteresis for better noise margin
- Monitor output
- Guaranteed low skew
  - 0.5ns output skew
  - 0.7ns pulse skew
  - 1ns part-to-part skew
- Available in 40-pin QVSOP

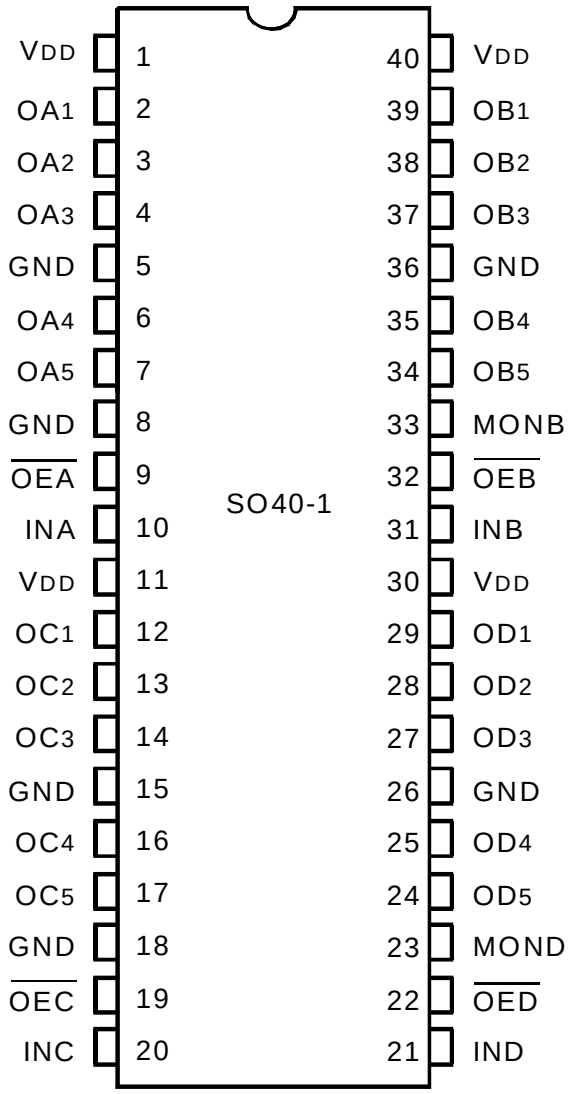
DESCRIPTION:

The QS5820T clock driver/buffer circuits can be used for clock distribution schemes where low skew, high speed, and small footprint are primary concerns. The QS5820T offers four banks of five non-inverting outputs. Designed in IDT's proprietary QCMOS process, this device provides low propagation delay buffering with on-chip skew of 0.5ns for same-transition, same-bank signals. The QS5820T provides major skew advantages over octal type devices where total part-to-part skew ($t_{SK(t)}$) of >1ns is unacceptable. Furthermore, board area consumed by the QVSOP package is almost one-third that of the typical SOIC package offered for octal devices. This clock buffer product is designed for use in high performance workstation, multi-board computing and telecommunications systems. The QS5820T is available in the 40-pin QVSOP package which offers the world's smallest logic footprint.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Max.	Unit
V_{TERM}(2)	Supply Voltage to Ground	–0.5 to +7	V
V_{TERM}(3)	DC Switch Voltage V_S	–0.5 to +7	V
V_{TERM}(3)	DC Input Voltage V_{IN}	–0.5 to +7	V
V_{AC}	AC Input Voltage (pulse width ≤20ns)	–3	V
	DC Input Diode Current with V_{IN} < 0	–20	mA
I_{OUT}	DC Output Current Max Sink Current/Pin	120	mA
P_{MAX}	Maximum Power Dissipation	1.2	W
T_{STG}	Storage Temperature Range	–65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} Terminals.
3. All terminals except V_{DD}.

CAPACITANCE (T_A = 25° C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V)

Pins	Typ.	Max.	Unit
All Pins	5	8	pF

NOTE:
1. Capacitance is characterized but not tested.

PIN DESCRIPTION

Pin Name	Type	Description
$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$, $\overline{OED}$	I	Output Enable Inputs
INA, INB, INC, IND	I	Clock Inputs
OAn, OBn, OCn, ODn	O	Clock Outputs
MONB, MOND	O	Non-disable Monitor Outputs

RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Min.	Max.	Unit
V_{DD}	Power Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	5.5	V
V_{OUT}	Voltage Applied to Outputs	0	5.5	V
T_A	Ambient Operating Temperature	0	+70	°C

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Inputs	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Inputs	—	—	0.8	V
V_{IC}	Clamp Diode Voltage (3)	V_{DD} = Min., I_{IN} = –18mA	—	– 0.7	– 1.2	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –24mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 64mA	—	—	0.55	V
I_{IN}	Input Leakage Current	V_{DD} = Max., V_{IN} = V_{DD} or GND	—	—	±1	µA
I_{OZ}	Output Leakage Current	V_{DD} = Max., Outputs High-Z	—	—	±1	µA
I_{OS}	Short Circuit Current (2,3)	V_{DD} = Max., V_{OUT} = GND	– 60	—	—	mA

NOTES:
1. Typical values are at V_{DD} = 5.0V, T_A = 25°C.
2. Not more than one output should be used to test this high power condition. Duration is ≤1 second.
3. Guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Typ. (3)	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{DD} = Max., V_{IN} = GND or V_{DD}	0.4	3	mA
ΔI_{CC}	Supply Current per Input HIGH	V_{DD} = Max., V_{IN} = 3.4V, f_i = 0MHz	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current per Output (2)	V_{DD} = Max., V_{IN} = GND or V_{DD} Outputs Enabled, 50% duty cycle	0.1	0.2	mA/MHz

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Guaranteed but not tested.
3. Typical values are for reference only. Conditions are V_{DD} = 5.0V and T_A = 25°C.
4. $I_C = I_{CC} + (\Delta I_{CC})(D_H)(N_T) + I_{CCD}(f_O)(N_O)$
   where:
   D_H = Input duty cycle
   N_T = Number of TTL HIGH inputs at D_H
   f_O = Output frequency
   N_O = Number of outputs at f_O

SKEW CHARACTERISTICS OVER OPERATING RANGE

Symbol	Description [1]	QS5820AT		QS5820BT		Unit
		Min.	Max.	Min.	Max.	
$t_{SK(01)}$	Skew between two outputs, same transition, same bank	—	0.5	—	0.5	ns
$t_{SK(02)}$	Skew between two outputs, same transition, different bank	—	0.6	—	0.6	ns
$t_{SK(p)}$	Duty cycle distortion (pulse skew) on a single output opposite transitions (t_{PHL} - t_{PLH})	—	1	—	0.7	ns
$t_{SK(t)}$	Part-to-part skew, same transition [2]	—	1.5	—	1	ns

NOTES:
1. Skew parameters are guaranteed across temperature range, but not production tested. Skew parameters apply to propagation delays only.
2. $t_{SK(t)}$ only applies to devices of the same transition, same V_{DD}, same temperature, same speed grade, and same loading.

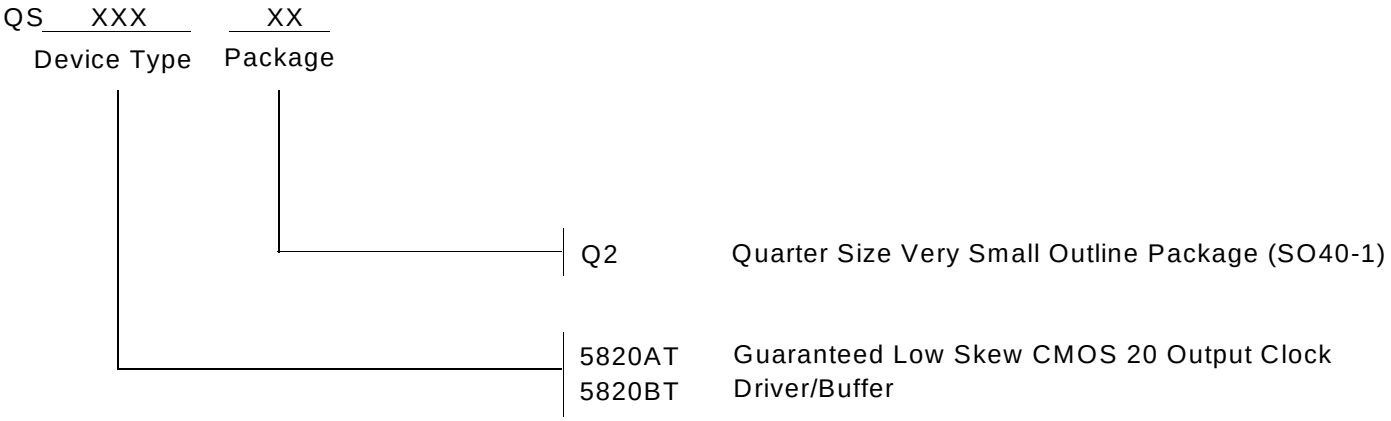
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description [1]	QS5820AT		QS5820BT		Unit
		Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay [1,2]	1.5	5.8	1.5	5	ns
t_R	Output Rise Time, 0.8V to 2V	—	1.5	—	1.5	ns
t_F	Output Fall Time, 2V to 0.8V	—	1.5	—	1.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5	8	1.5	7	ns
t_{PLZ} t_{PHZ}	Output Disable Time	1.5	7	1.5	6	ns

NOTES:
1. Minimums guaranteed but not tested.
2. The propagation delay range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delay limits do not imply skew.

ORDERING INFORMATION



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