



3.3V CMOS 16-BIT EDGE-TRIGGERED D-TYPE FLIP- FLOP WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O

IDT74LVC162374A

FEATURES:

- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Available in SSOP, TSSOP, and TVSOP packages

DRIVE FEATURES:

- Balanced Output Drivers: $\pm 12mA$
- Low switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

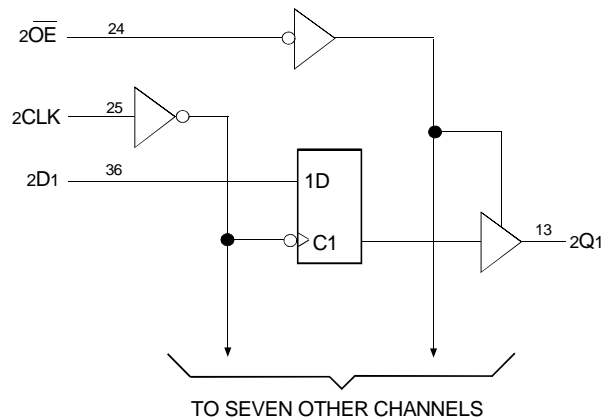
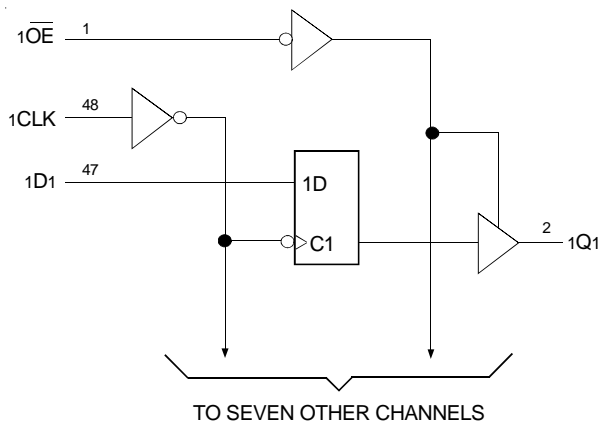
DESCRIPTION:

The LVC162374A 16-bit edge-triggered D-type flip-flop is built using advanced dual metal CMOS technology. This high-speed, low-power register is ideal for use as a buffer register for data synchronization and storage. The output enable (\overline{OE}) and clock (CLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

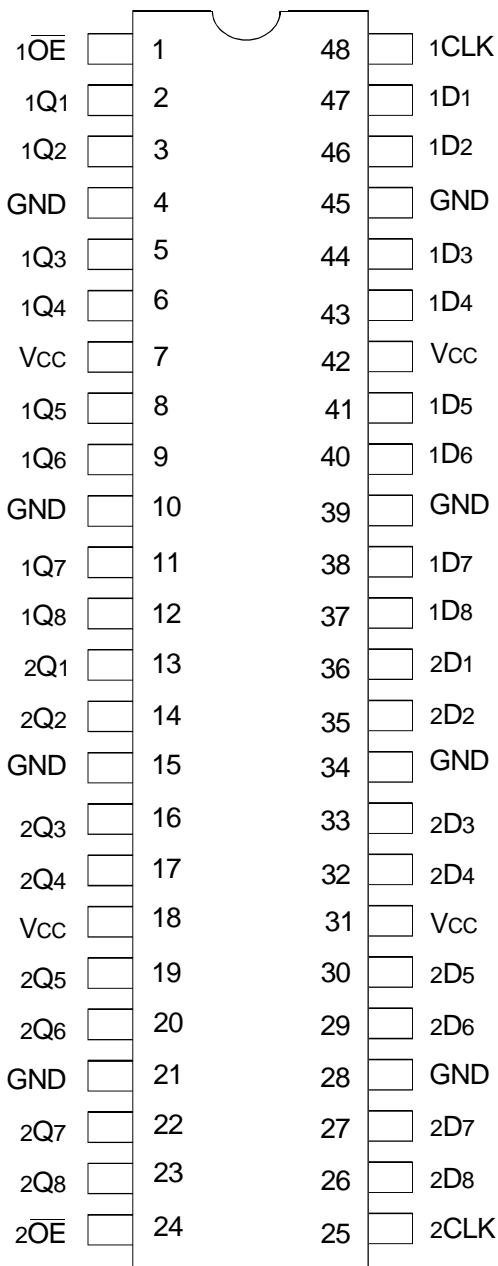
All pins of the LVC162374A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC162374A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been developed to drive $\pm 12mA$ at the designated thresholds.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|----------------------|---|--------------|------|
| VTERM ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +6.5 | V |
| VTERM ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to +6.5 | V |
| TSTG | Storage Temperature | -65 to +150 | °C |
| IOUT | DC Output Current | -50 to +50 | mA |
| IIK IOK | Continuous Clamp Current, Vi < 0 or Vo < 0 | -50 | mA |
| ICC ISS | Continuous Current through each Vcc or GND | ±100 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|--------|--------------------------|------------|------|------|------|
| CIN | Input Capacitance | VIN = 0V | 4.5 | 6 | pF |
| COUT | Output Capacitance | VOUT = 0V | 6.5 | 8 | pF |
| CIO | I/O Port Capacitance | VIN = 0V | 6.5 | 8 | pF |

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

| Pin Names | Description |
|-----------|---|
| xDx | Data Inputs |
| xCLK | Clock Inputs |
| xQx | 3-State Outputs |
| xOE | 3-State Output Enable Inputs (Active LOW) |

FUNCTION TABLE (EACH FLIP-FLOP)⁽¹⁾

| Inputs | | | Outputs |
|--------|--------|-----|------------------|
| xOE | xCLK | xDx | xQx |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q ⁽²⁾ |
| H | X | X | Z |

NOTES:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High-Impedance
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--|--|---|---|------|---------------------|------|------|
| V _{IH} | Input HIGH Voltage Level | V _{CC} = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | V _{CC} = 2.7V to 3.6V | | 2 | — | — | |
| V _{IL} | Input LOW Voltage Level | V _{CC} = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | V _{CC} = 2.7V to 3.6V | | — | — | 0.8 | |
| I _{IH} I _{IL} | Input Leakage Current | V _{CC} = 3.6V | V _I = 0 to 5.5V | — | — | ±5 | μA |
| I _{OZH} I _{OZL} | High Impedance Output Current (3-State Output pins) | V _{CC} = 3.6V | V _O = 0 to 5.5V | — | — | ±10 | μA |
| I _{OFF} | Input/Output Power Off Leakage | V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V | | — | — | ±50 | μA |
| V _{IK} | Clamp Diode Voltage | V _{CC} = 2.3V, I _{IN} = -18mA | | — | -0.7 | -1.2 | V |
| V _H | Input Hysteresis | V _{CC} = 3.3V | | — | 100 | — | mV |
| I _{CC1} I _{CC2} I _{CC3} | Quiescent Power Supply Current | V _{CC} = 3.6V | V _{IN} = GND or V _{CC} | — | — | 10 | μA |
| | | | 3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾ | — | — | 10 | |
| ΔI _{CC} | Quiescent Power Supply Current Variation | One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND | | — | — | 500 | μA |

NOTES:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|-----------------|-------------------------|--------------------------------|--------------------------|-----------------------|------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} = 2.3V to 3.6V | I _{OH} = -0.1mA | V _{CC} - 0.2 | — | V |
| | | V _{CC} = 2.3V | I _{OH} = -4mA | 1.9 | — | |
| | | | I _{OH} = -6mA | 1.7 | — | |
| | | V _{CC} = 2.7V | I _{OH} = -4mA | 2.2 | — | |
| | | | I _{OH} = -8mA | 2 | — | |
| | | V _{CC} = 3V | I _{OH} = -6mA | 2.4 | — | |
| | I _{OH} = -12mA | 2 | — | | | |
| V _{OL} | Output LOW Voltage | V _{CC} = 2.3V to 3.6V | I _{OL} = 0.1mA | — | 0.2 | V |
| | | V _{CC} = 2.3V | I _{OL} = 4mA | — | 0.4 | |
| | | | I _{OL} = 6mA | — | 0.55 | |
| | | V _{CC} = 2.7V | I _{OL} = 4mA | — | 0.4 | |
| | | | I _{OL} = 8mA | — | 0.6 | |
| | | V _{CC} = 3V | I _{OL} = 6mA | — | 0.55 | |
| | I _{OL} = 12mA | — | 0.8 | | | |

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

| Symbol | Parameter | Test Conditions | Typical | Unit |
|--------|--|---------------------------|---------|------|
| CPD | Power Dissipation Capacitance per Flip-Flop Outputs enabled | $C_L = 0pF$, $f = 10MHz$ | — | pF |
| CPD | Power Dissipation Capacitance per Flip-Flop Outputs disabled | | — | |

SWITCHING CHARACTERISTICS⁽¹⁾

| Symbol | Parameter | $V_{CC} = 2.7V$ | | $V_{CC} = 3.3V \pm 0.3V$ | | Unit |
|------------------------|---|-----------------|------|--------------------------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t_{PLH} t_{PHL} | Propagation Delay xCLK to xQx | 2 | 6.5 | 2 | 6.2 | ns |
| t_{PZH} t_{PZL} | Output Enable Time x \overline{OE} to xQx | 1.5 | 6.3 | 1.5 | 6.1 | ns |
| t_{PHZ} t_{PLZ} | Output Disable Time x \overline{OE} to xQx | 1.5 | 6.2 | 1.5 | 6 | ns |
| t_{SU} | Set-up Time HIGH or LOW, xDx before xCLK \uparrow | 2.5 | — | 2.5 | — | ns |
| t_H | Hold Time HIGH or LOW, xDx after xCLK \uparrow | 1.5 | — | 1.5 | — | ns |
| t_W | xCLK Pulse Width HIGH or LOW | 3 | — | 3 | — | ns |
| $t_{SK(0)}$ | Output Skew ⁽²⁾ | — | — | — | 500 | ps |

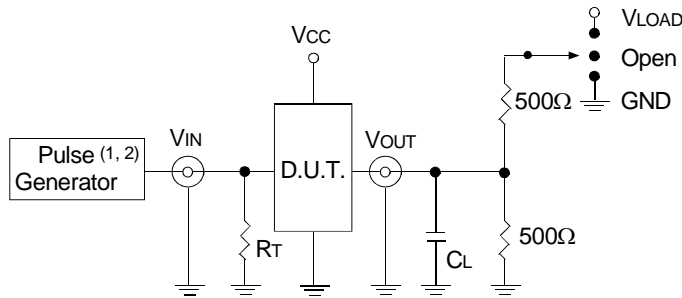
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. $T_A = -40^\circ C$ to $+85^\circ C$.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

| Symbol | V _{CC} ⁽¹⁾ =3.3V±0.3V | V _{CC} ⁽¹⁾ =2.7V | V _{CC} ⁽²⁾ =2.5V±0.2V | Unit |
|-------------------|---|--------------------------------------|---|------|
| V _{LOAD} | 6 | 6 | 2 x V _{CC} | V |
| V _{IH} | 2.7 | 2.7 | V _{CC} | V |
| V _T | 1.5 | 1.5 | V _{CC} / 2 | V |
| V _{LZ} | 300 | 300 | 150 | mV |
| V _{HZ} | 300 | 300 | 150 | mV |
| C _L | 50 | 50 | 30 | pF |



Test Circuit for All Outputs

DEFINITIONS:

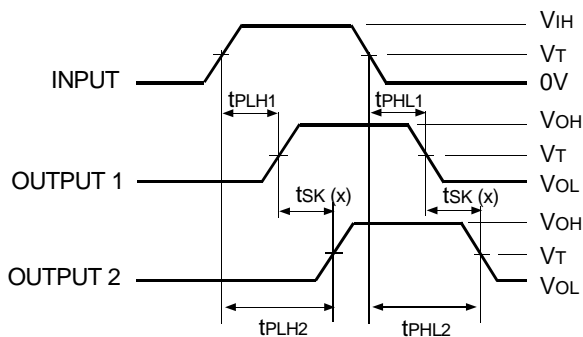
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

| Test | Switch |
|---|-------------------|
| Open Drain Disable Low Enable Low | V _{LOAD} |
| Disable High Enable High | GND |
| All Other Tests | Open |

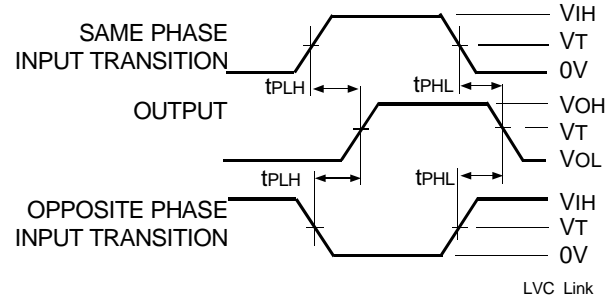


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

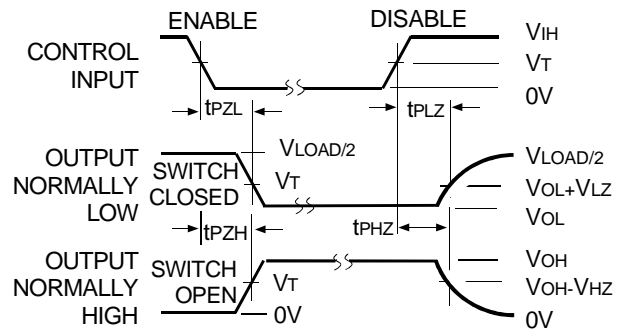
Output Skew - tsk(x)

NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



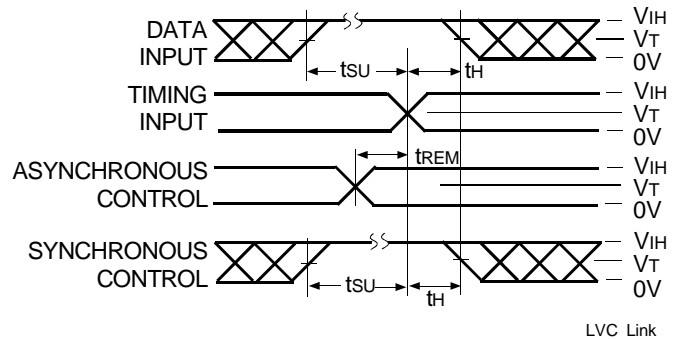
Propagation Delay



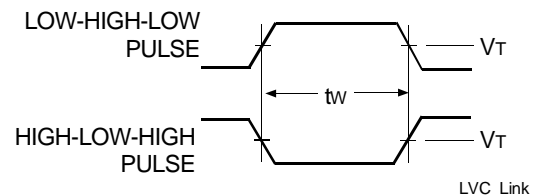
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

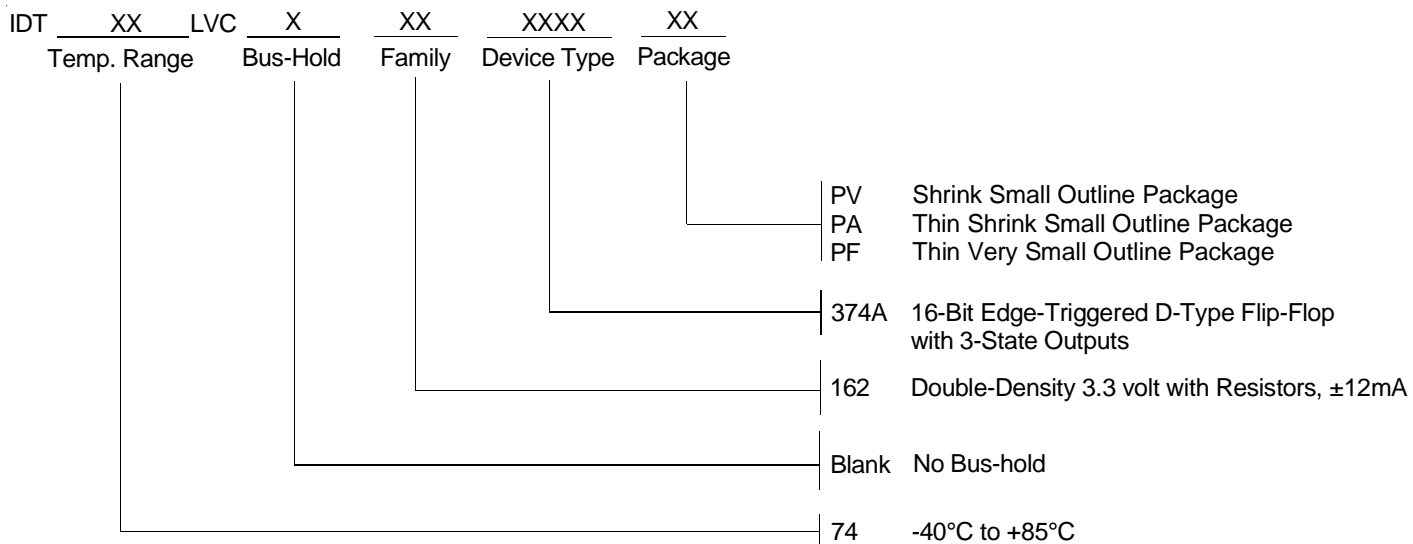


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
 (408) 654-6459