



3.3V CMOS DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET, 5 VOLT TOLERANT I/O

IDT74LVC112A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Vcc = 3.3V ± 0.3V, Normal Range
- Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs, and I/Os are 5V tolerant
- Supports hot insertion
- Available in QSOP, SOIC, SSOP, and TSSOP packages

DRIVE FEATURES:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

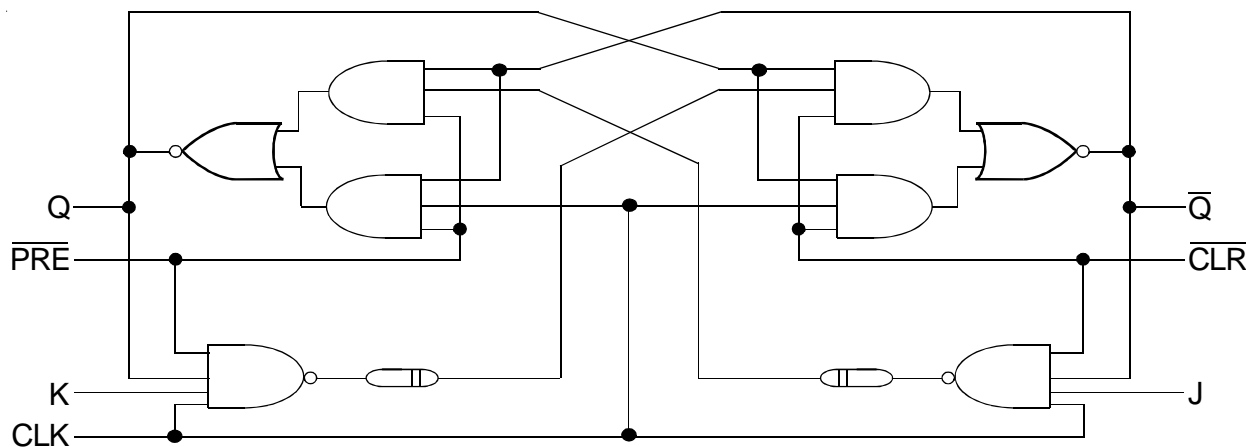
DESCRIPTION:

This dual negative-edge-triggered J-K flip-flop is built using advanced dual metal CMOS technology. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and K inputs meeting the setup time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs can be changed without affecting the levels at the outputs. The LVC112A can perform as a toggle flip-flop by tying J and K high.

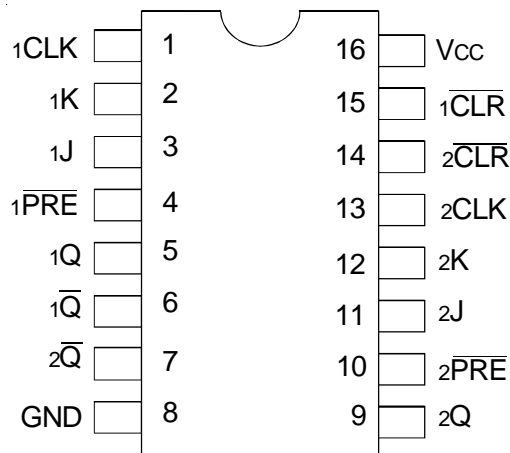
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC112A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP/ SOIC/ SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
IK Iok	Continuous Clamp Current, Vi < 0 or Vo < 0	-50	mA
ICC Iss	Continuous Current through each Vcc or GND	±100	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOU = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	VIN = 0V	6.5	8	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xCLK	CLK Inputs
xCLR-bar	Clear Inputs (Active LOW)
xPRE-bar	Preset Inputs (Active LOW)
xJ, xK	Data Inputs
xQ, xQ-bar	Data Outputs

FUNCTION TABLE⁽¹⁾

Inputs					Outputs	
xPRE-bar	xCLR-bar	xCLK	xJ	xK	xQ	xQ-bar
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H ⁽²⁾	H ⁽²⁾
H	H	↓	L	L	Q ⁽³⁾	Q-bar ⁽⁴⁾
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q ⁽³⁾	Q-bar ⁽⁴⁾

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↓ = HIGH-to-LOW transition
- The output levels in this configuration may not meet the minimum levels for VOH. Furthermore, this configuration is unstable; that is, it does not persist when either PRE-bar or CLR-bar returns to its inactive (HIGH) level.
- Level of Q before the indicated steady-state input conditions were established.
- Complement of Q or level of Q-bar before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V, V _{IN} = GND or V _{CC}		—	—	10	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	500	μA

NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = -12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3V		2.4	—	
		V _{CC} = 3V	I _{OH} = -24mA	2.2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3V	I _{OL} = 24mA	—	0.55	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range.
T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Flip-Flop	$C_L = 0pF$, $f = 10MHz$	24	pF

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
f_{MAX}		150	—	150	—	MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{x}CLR$ or \overline{PRE} to xQ or $x\overline{Q}$	—	5.5	1	4.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{x}CLK$ to xQ or $x\overline{Q}$	—	7.1	1	5.9	ns
t_{SU}	Setup Time, Data before $CLK\downarrow$	2.3	—	3.1	—	ns
t_{SU}	Setup Time, \overline{PRE} or \overline{CLR} inactive	1.1	—	2.4	—	ns
t_H	Hold Time, data after $CLK\downarrow$	0.7	—	2.5	—	ns
t_W	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	ns
$t_{sk(0)}$	Output Skew ⁽²⁾	—	—	—	500	ps

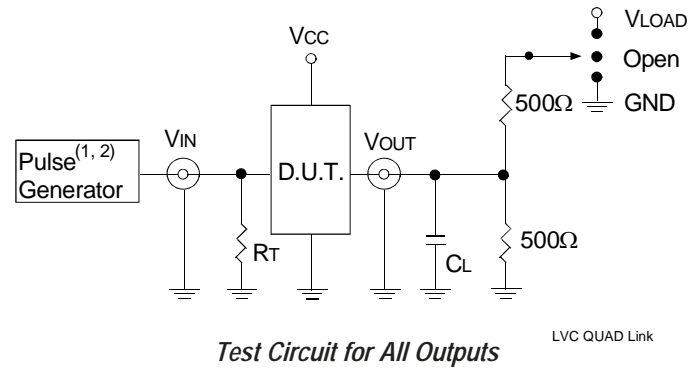
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. $T_A = -40^\circ C$ to $+85^\circ C$.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{cc} ⁽¹⁾ = 2.5V ± 0.2V	V _{cc} ⁽²⁾ = 3.3V ± 0.3V & 2.7V	Unit
V _{LOAD}	2 x V _{cc}	6	V
V _{IH}	V _{cc}	2.7	V
V _T	V _{cc} / 2	1.5	V
V _{LZ}	150	300	mV
V _{HZ}	150	300	mV
C _L	30	50	pF



DEFINITIONS:

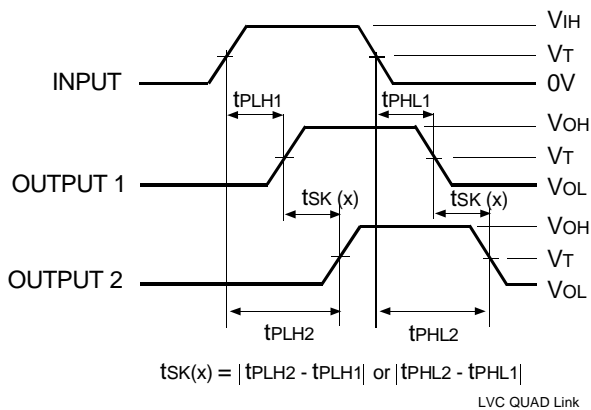
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{out} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.

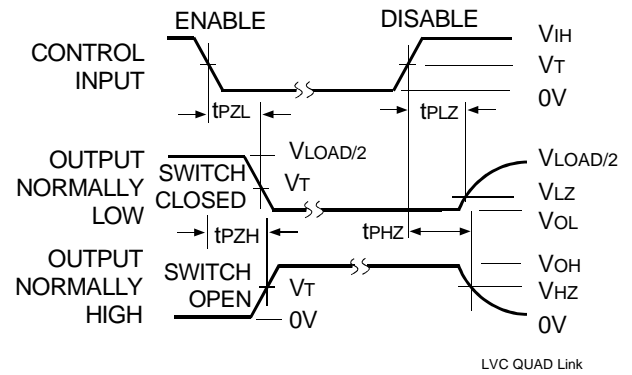
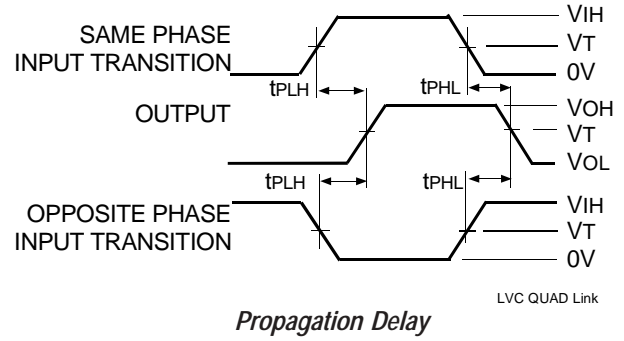
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



NOTES:

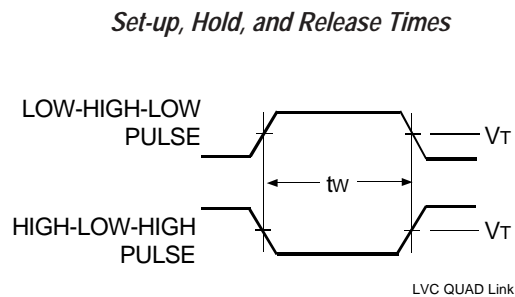
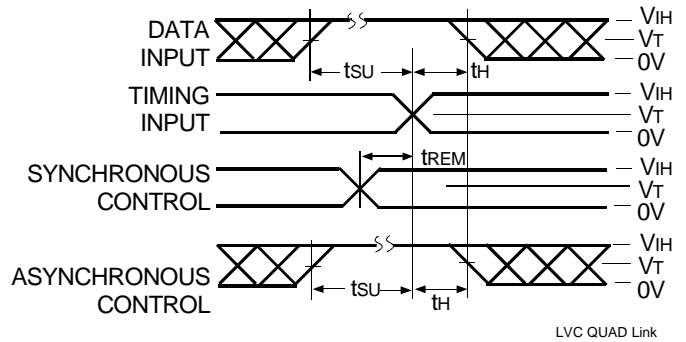
1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



NOTE:

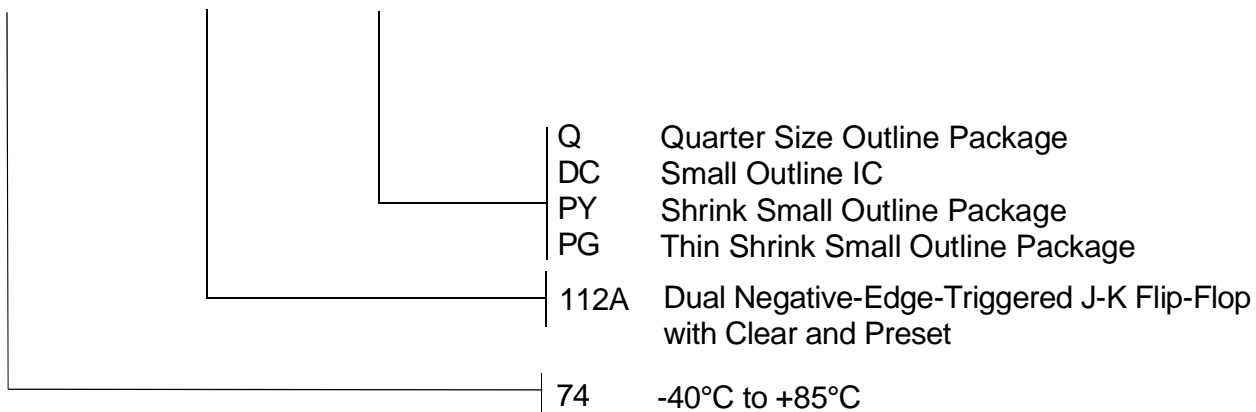
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times



ORDERING INFORMATION

IDT XX LVC XXXX XX
Temp. Range Device Type Package



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