



CMOS Static RAM 64K (8K x 8-Bit)

IDT7164S
IDT7164L

Features

- ◆ High-speed address/chip select access time
 - Military: 20/25/35/45/55/70/85/100ns (max.)
 - Industrial: 25/35ns (max.)
 - Commercial: 15/20/25/35ns (max.)
- ◆ Low power consumption
- ◆ Battery backup operation – 2V data retention voltage (L Version only)
- ◆ Produced with advanced CMOS high-performance technology
- ◆ Inputs and outputs directly TTL-compatible
- ◆ Three-state outputs
- ◆ Available in 28-pin DIP, CERDIP and SOJ
- ◆ Military product compliant to MIL-STD-883, Class B

Description

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

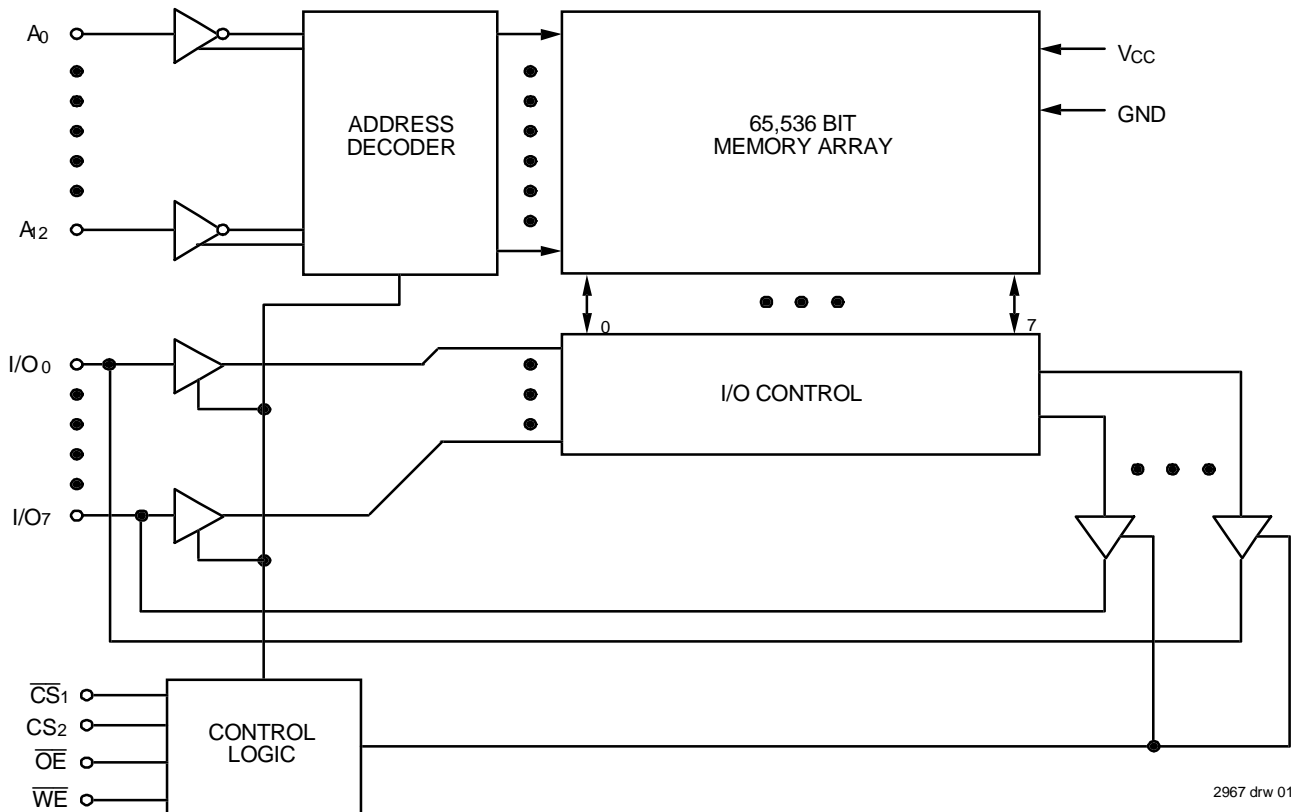
Address access times as fast as 15ns are available and the circuit offers a reduced power standby mode. When \overline{CS}_1 goes HIGH or CS_2 goes LOW, the circuit will automatically go to, and remain in, a low-power standby mode. The low-power (L) version also offers a battery backup data retention capability at power supply levels as low as 2V.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin 300 mil DIP and SOJ and a 28-pin 600 mil CERDIP.

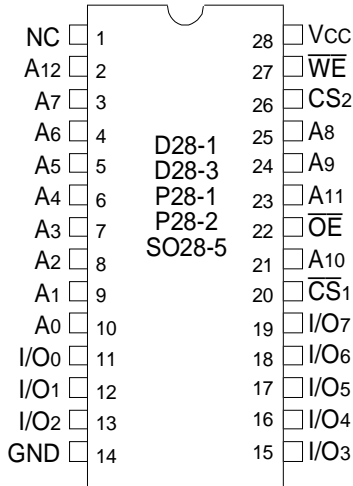
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Functional Block Diagram



DECEMBER 2001

Pin Configurations



2967 drw 02

DIP/SOJ Top View

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Com'l. | Mil. | Unit |
|------------------|--------------------------------------|--------------|--------------|------|
| $V_{TERM}^{(2)}$ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V |
| T_A | Operating Temperature | 0 to +70 | -55 to +125 | °C |
| T_{BIAS} | Temperature Under Bias | -55 to +125 | -65 to +135 | °C |
| T_{STG} | Storage Temperature | -55 to +125 | -65 to +150 | °C |
| P_T | Power Dissipation | 1.0 | 1.0 | W |
| I_{OUT} | DC Output Current | 50 | 50 | mA |

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed $V_{CC} + 0.5V$.

Pin Descriptions

| Name | Description |
|-------------------|-------------------|
| $A_0 - A_{12}$ | Address |
| $I/O_0 - I/O_7$ | Data Input/Output |
| \overline{CS}_1 | Chip Select |
| CS_2 | Chip Select |
| \overline{WE} | Write Enable |
| \overline{OE} | Output Enable |
| GND | Ground |
| V_{CC} | Power |

2967 tbl 01

Truth Table^(1,2,3)

| \overline{WE} | \overline{CS}_1 | CS_2 | \overline{OE} | I/O | Function |
|-----------------|-------------------|----------------------|-----------------|--------------|-----------------------------|
| X | H | X | X | High-Z | Deselected - Standby (ISB) |
| X | X | L | X | High-Z | Deselected - Standby (ISB) |
| X | V_{HC} | V_{HC} or V_{LC} | X | High-Z | Deselected - Standby (ISB1) |
| X | X | V_{LC} | X | High-Z | Deselected - Standby (ISB1) |
| H | L | H | H | High-Z | Output Disabled |
| H | L | H | L | $DATA_{OUT}$ | Read Data |
| L | L | H | X | $DATA_{IN}$ | Write Data |

2967 tbl 03

NOTES:

- CS_2 will power-down \overline{CS}_1 , but \overline{CS}_1 will not power-down CS_2 .
- H = V_{IH} , L = V_{IL} , X = don't care.
- $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------|--------------------|---------------------|------|----------------|------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| V_{IH} | Input HIGH Voltage | 2.2 | — | $V_{CC} + 0.5$ | V |
| V_{IL} | Input LOW Voltage | -0.5 ⁽¹⁾ | — | 0.8 | V |

2967 tbl 05

NOTE:

- V_{IL} (min.) = -1.5V for pulse width less than 10ns, once per cycle.

Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | GND | V_{CC} |
|------------|-----------------|-----|---------------|
| Military | -55°C to +125°C | 0V | $5V \pm 10\%$ |
| Industrial | -40°C to +85°C | 0V | $5V \pm 10\%$ |
| Commercial | 0°C to +70°C | 0V | $5V \pm 10\%$ |

2967 tbl 04

Capacitance (TA = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|-----------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 8 | pF |
| C _{VO} | I/O Capacitance | V _{OUT} = 0V | 8 | pF |

2967 tbl 06

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

DC Electrical Characteristics⁽¹⁾ (V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

| Symbol | Parameter | Power | 7164S15 7164L15 | 7164S20 7164L20 | 7164S25 7164L25 | | | Unit | |
|--------|---|-------|--------------------|--------------------|--------------------|--------|------|------|------|
| | | | Com'l. | Com'l. | Mil. | Com'l. | Ind. | | Mil. |
| ICC1 | Operating Power Supply Current CS ₁ = V _{IL} , CS ₂ = V _H , Outputs Open V _{CC} = Max., f = 0 ⁽²⁾ | S | 110 | 100 | 110 | 90 | 90 | 110 | mA |
| | | L | 100 | 90 | 100 | 80 | 80 | 100 | |
| ICC2 | Dynamic Operating Current CS ₁ = V _{IL} , CS ₂ = V _H , Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾ | S | 180 | 170 | 180 | 170 | 170 | 180 | mA |
| | | L | 150 | 150 | 160 | 150 | 150 | 160 | |
| ISB | Standby Power Supply Current (TTL Level), CS ₁ ≥ V _H , CS ₂ ≤ V _{IL} , Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾ | S | 20 | 20 | 20 | 20 | 20 | 20 | mA |
| | | L | 3 | 3 | 5 | 3 | 3 | 5 | |
| ISB1 | Full Standby Power Supply Current (CMOS Level), f = 0 ⁽²⁾ , V _{CC} = Max. 1. CS ₁ ≥ V _{HC} and CS ₂ ≥ V _{HC} , or 2. CS ₂ ≤ V _{LC} | S | 15 | 15 | 20 | 15 | 15 | 20 | mA |
| | | L | 0.2 | 0.2 | 1 | 0.2 | 0.2 | 1 | |

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| Symbol | Parameter | Power | 7164S35 7164L35 | | | 7164S45 7164L45 | 7164S55 7164L55 | 7164S70 7164L70 | 7164S85/100 7164L85/100 | Unit |
|--------|---|-------|--------------------|------|------|--------------------|--------------------|--------------------|----------------------------|------|
| | | | Com'l. | Ind. | Mil. | Mil. | Mil. | Mil. | Mil. | |
| ICC1 | Operating Power Supply Current CS ₁ = V _{IL} , CS ₂ = V _H , Outputs Open V _{CC} = Max., f = 0 ⁽²⁾ | S | 90 | 90 | 100 | 100 | 100 | 100 | 100 | mA |
| | | L | 80 | 80 | 90 | 90 | 90 | 90 | 90 | |
| ICC2 | Dynamic Operating Current CS ₁ = V _{IL} , CS ₂ = V _H , Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾ | S | 150 | 150 | 160 | 160 | 160 | 160 | 160 | mA |
| | | L | 130 | 130 | 140 | 130 | 125 | 120 | 120 | |
| ISB | Standby Power Supply Current (TTL Level), CS ₁ ≥ V _H , CS ₂ ≤ V _{IL} , Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾ | S | 20 | 20 | 20 | 20 | 20 | 20 | 20 | mA |
| | | L | 3 | 3 | 5 | 5 | 5 | 5 | 5 | |
| ISB1 | Full Standby Power Supply Current (CMOS Level), f = 0 ⁽²⁾ , V _{CC} = Max. 1. CS ₁ ≥ V _{HC} and CS ₂ ≥ V _{HC} , or 2. CS ₂ ≤ V _{LC} | S | 15 | 15 | 20 | 20 | 20 | 20 | 20 | mA |
| | | L | 0.2 | 0.2 | 1 | 1 | 1 | 1 | 1 | |

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NOTES:

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/trc (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%)

| Symbol | Parameter | Test Conditions | IDT7164S | | IDT7164L | | Unit | |
|-----------------|------------------------|---|----------------------|--------|----------|--------|--------|----|
| | | | Min. | Max. | Min. | Max. | | |
| I _{LI} | Input Leakage Current | V _{CC} = Max., V _{IN} = GND to V _{CC} | MIL. COM'L. & IND | — 5 | 10 5 | — 2 | 5 2 | μA |
| I _{LO} | Output Leakage Current | V _{CC} = Max., $\overline{CS}_1 = V_{IH}$, V _{OUT} = GND to V _{CC} | MIL. COM'L. & IND | — 5 | 10 5 | — 2 | 5 2 | μA |
| V _{OL} | Output Low Voltage | IoL = 8mA, V _{CC} = Min. | — | 0.4 | — | 0.4 | V | |
| | | IoL = 10mA, V _{CC} = Min. | — | 0.5 | — | 0.5 | | |
| V _{OH} | Output High Voltage | IoH = -4mA, V _{CC} = Min. | 2.4 | — | 2.4 | — | V | |

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Data Retention Characteristics Over All Temperature Ranges (L Version Only) (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

| Symbol | Parameter | Test Condition | Min. | Typ. ⁽¹⁾ V _{CC} @ | | Max. V _{CC} @ | | Unit |
|----------------------------------|--------------------------------------|--|--------------------------------|--|----------|---------------------------|-----------|------|
| | | | | 2.0V | 3.0V | 2.0V | 3.0V | |
| V _{DR} | V _{CC} for Data Retention | — | 2.0 | — | — | — | — | V |
| I _{CCDR} | Data Retention Current | MIL. COM'L. & IND | — — | 10 10 | 15 15 | 200 60 | 300 90 | μA |
| t _{CDR} ⁽³⁾ | Chip Deselect to Data Retention Time | 1. $\overline{CS}_1 \geq V_{HC}$ CS ₂ ≥ V _{HC} , or 2. CS ₂ ≤ V _{LC} | 0 | — | — | — | — | ns |
| t _R ⁽³⁾ | Operation Recovery Time | | t _{RC} ⁽²⁾ | — | — | — | — | ns |
| I _{LI} ⁽³⁾ | Input Leakage Current | | — | — | — | 2 | 2 | μA |

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NOTES:

- TA = +25°C.
- t_{RC} = Read Cycle Time.
- This parameter is guaranteed by device characterization, but is not production tested.

AC Test Conditions

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figures 1 and 2 |

2967 tbl 11

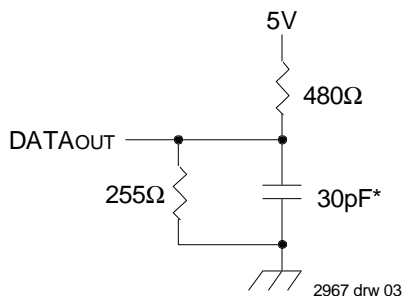


Figure 1. AC Test Load

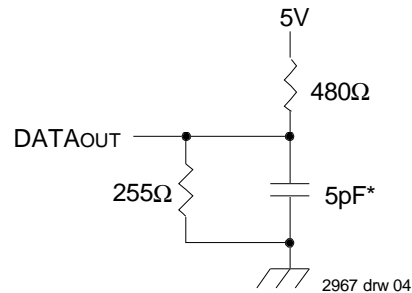


Figure 2. AC Test Load

(for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Includes scope and jig capacitances

AC Electrical Characteristics (Vcc = 5.0V ± 10%, All Temperature Ranges)

| Symbol | Parameter | 7164S15 ⁽¹⁾ 7164L15 ⁽¹⁾ | | 7164S20 ⁽²⁾ 7164L20 ⁽²⁾ | | 7164S25 7164L25 | | 7164S35 7164L35 | | Unit |
|------------------------------------|--|--|------|--|------|--------------------|------|--------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 15 | — | 20 | — | 25 | — | 35 | — | ns |
| t _{AA} | Address Access Time | — | 15 | — | 19 | — | 25 | — | 35 | ns |
| t _{ACS1} ⁽³⁾ | Chip Select-1 Access Time | — | 15 | — | 20 | — | 25 | — | 35 | ns |
| t _{ACS2} ⁽³⁾ | Chip Select-2 Access Time | — | 20 | — | 25 | — | 30 | — | 40 | ns |
| t _{CLZ1,2} ⁽⁴⁾ | Chip Select-1, 2 to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{OE} | Output Enable to Output Valid | — | 7 | — | 8 | — | 12 | — | 18 | ns |
| t _{OLZ} ⁽⁴⁾ | Output Enable to Output in Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{CHZ1,2} ⁽⁴⁾ | Chip Select-1,2 to Output in High-Z | — | 8 | — | 9 | — | 13 | — | 15 | ns |
| t _{OHZ} ⁽⁴⁾ | Output Disable to Output in High-Z | — | 7 | — | 8 | — | 10 | — | 15 | ns |
| t _{OH} | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{PU} ⁽⁴⁾ | Chip Select to Power Up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} ⁽⁴⁾ | Chip Deselect to Power Down Time | — | 15 | — | 20 | — | 25 | — | 35 | ns |
| Write Cycle | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 15 | — | 20 | — | 25 | — | 35 | — | ns |
| t _{CW1,2} | Chip Select to End-of-Write | 14 | — | 15 | — | 18 | — | 25 | — | ns |
| t _{AW} | Address Valid to End-of-Write | 14 | — | 15 | — | 18 | — | 25 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 14 | — | 15 | — | 21 | — | 25 | — | ns |
| t _{WR1} | Write Recovery Time ($\overline{CS}_1, \overline{WE}$) | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WR2} | Write Recovery Time (CS ₂) | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{WHZ} ⁽⁴⁾ | Write Enable to Output in High-Z | — | 6 | — | 8 | — | 10 | — | 14 | ns |
| t _{DW} | Data to Write Time Overlap | 8 | — | 10 | — | 13 | — | 15 | — | ns |
| t _{DH1} | Data Hold from Write Time ($\overline{CS}_1, \overline{WE}$) | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{DH2} | Data Hold from Write Time (CS ₂) | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{OW} ⁽⁴⁾ | Output Active from End-of-Write | 4 | — | 4 | — | 4 | — | 4 | — | ns |

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NOTES:

- 0° to +70°C temperature range only.
- 0° to +70°C and -55°C to +125°C temperature ranges only.
- Both chip selects must be active for the device to be selected.
- This parameter is guaranteed by device characterization, but is not production tested.

AC Electrical Characteristics (con't.) (V_{cc} = 5.0V ± 10%, Military Temperature Ranges)

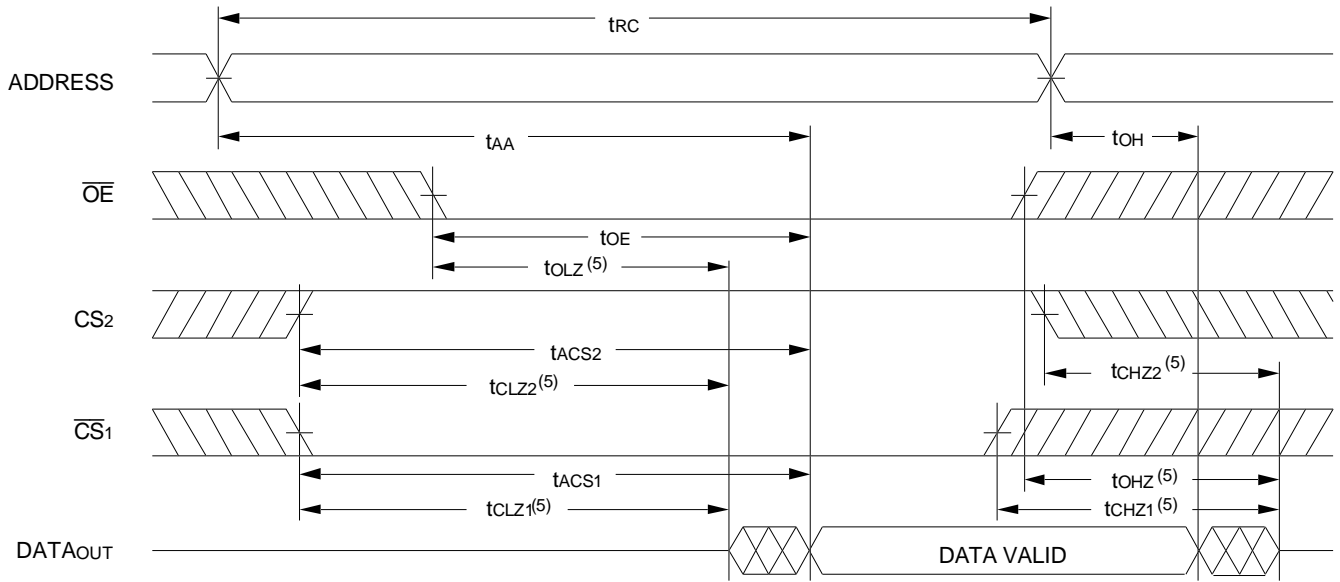
| Symbol | Parameter | 7164S45 7164L45 | | 7164S55 7164L55 | | 7164S70 7164L70 | | 7164S85/100 7164L85/100 | | Unit |
|------------------------------------|--|--------------------|------|--------------------|------|--------------------|------|----------------------------|--------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 45 | — | 55 | — | 70 | — | 85/100 | — | ns |
| t _{AA} | Address Access Time | — | 45 | — | 55 | — | 70 | — | 85/100 | ns |
| t _{ACS1} ⁽¹⁾ | Chip Select-1 Access Time | — | 45 | — | 55 | — | 70 | — | 85/100 | ns |
| t _{ACS2} ⁽¹⁾ | Chip Select-2 Access Time | — | 45 | — | 55 | — | 70 | — | 85/100 | ns |
| t _{CLZ1,2} ⁽²⁾ | Chip Select-1, 2 to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{OE} | Output Enable to Output Valid | — | 25 | — | 30 | — | 35 | — | 40 | ns |
| t _{OLZ} ⁽²⁾ | Output Enable to Output in Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{CHZ1,2} ⁽²⁾ | Chip Select-1,2 to Output in High-Z | — | 20 | — | 25 | — | 30 | — | 35 | ns |
| t _{OHZ} ⁽²⁾ | Output Disable to Output in High-Z | — | 20 | — | 25 | — | 30 | — | 35 | ns |
| t _{OH} | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{PU} ⁽²⁾ | Chip Select to Power Up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} ⁽²⁾ | Chip Deselect to Power Down Time | — | 45 | — | 55 | — | 70 | — | 85/100 | ns |
| Write Cycle | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 45 | — | 55 | — | 70 | — | 85/100 | — | ns |
| t _{OW1,2} | Chip Select to End-of-Write | 33 | — | 50 | — | 60 | — | 75 | — | ns |
| t _{AW} | Address Valid to End-of-Write | 33 | — | 50 | — | 60 | — | 75 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 25 | — | 50 | — | 60 | — | 75 | — | ns |
| t _{WR1} | Write Recovery Time ($\overline{CS}_1, \overline{WE}$) | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WR2} | Write Recovery Time (CS ₂) | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{WHZ} ⁽²⁾ | Write Enable to Output in High-Z | — | 18 | — | 25 | — | 30 | — | 35 | ns |
| t _{DW} | Data to Write Time Overlap | 20 | — | 25 | — | 30 | — | 35 | — | ns |
| t _{DH1} | Data Hold from Write Time ($\overline{CS}_1, \overline{WE}$) | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{DH2} | Data Hold from Write Time (CS ₂) | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{OW} ⁽²⁾ | Output Active from End-of-Write | 4 | — | 4 | — | 4 | — | 4 | — | ns |

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NOTES:

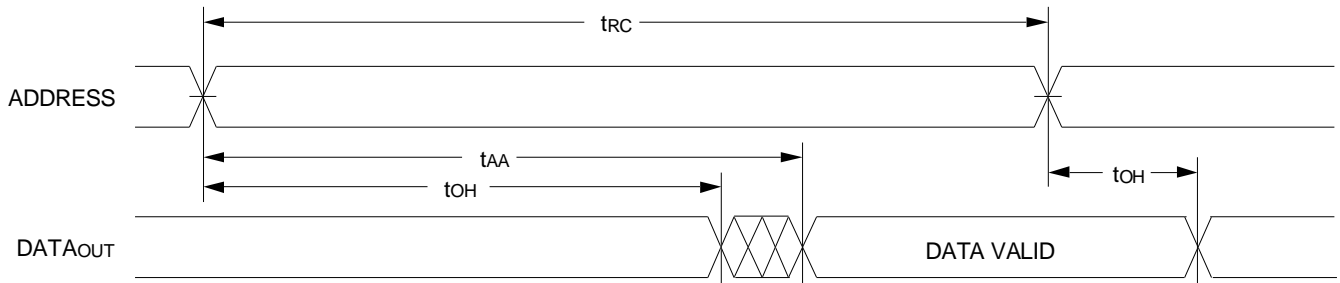
- Both chip selects must be active for the device to be selected.
- This parameter is guaranteed by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1⁽¹⁾



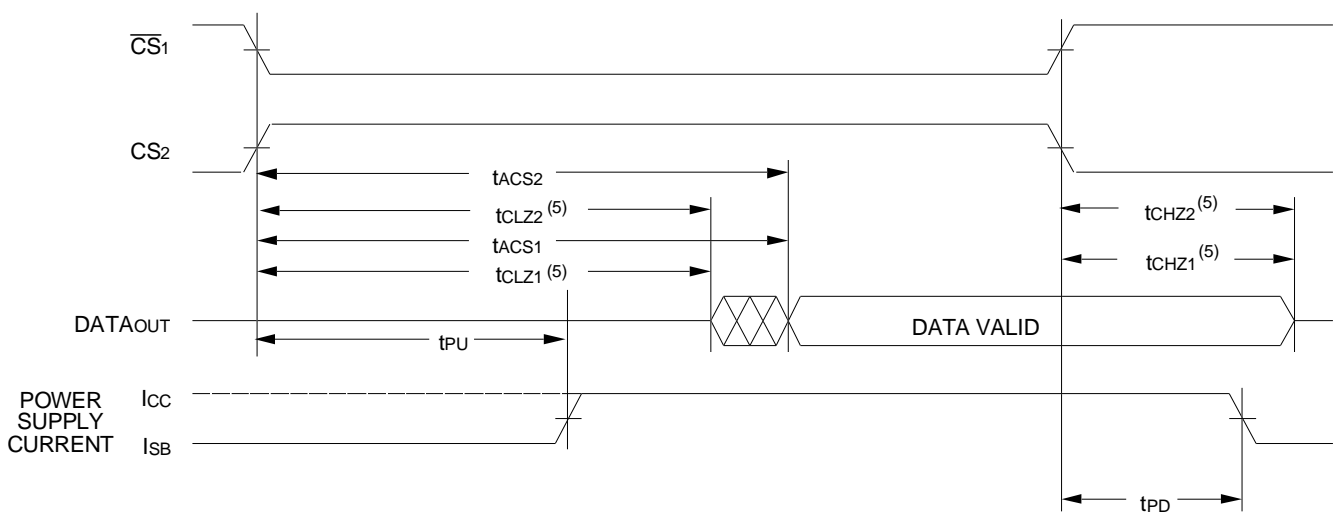
2967 drw 05

Timing Waveform of Read Cycle No. 2^(1,2,4)



2967 drw 06

Timing Waveform of Read Cycle No. 3^(1,3,4)

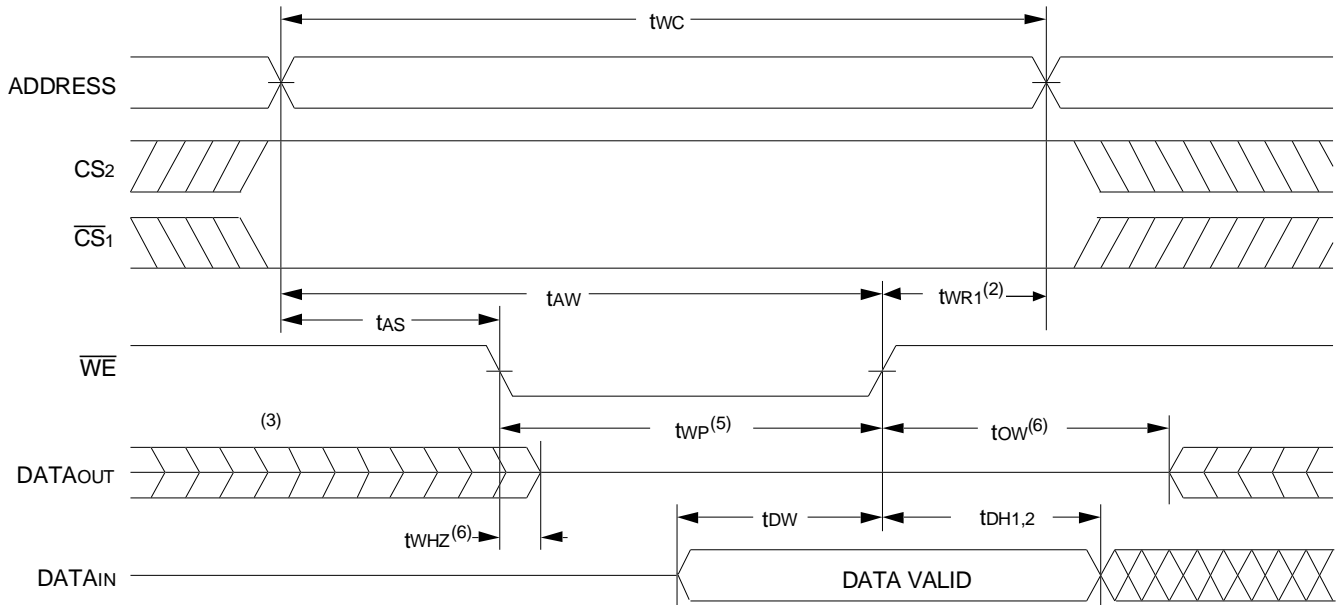


NOTES:

1. \overline{WE} is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS1}$ is LOW, CS2 is HIGH.
3. Address valid prior to or coincident with $\overline{CS1}$ transition LOW and CS2 transition HIGH.
4. \overline{OE} is LOW.
5. Transition is measured $\pm 200mV$ from steady state.

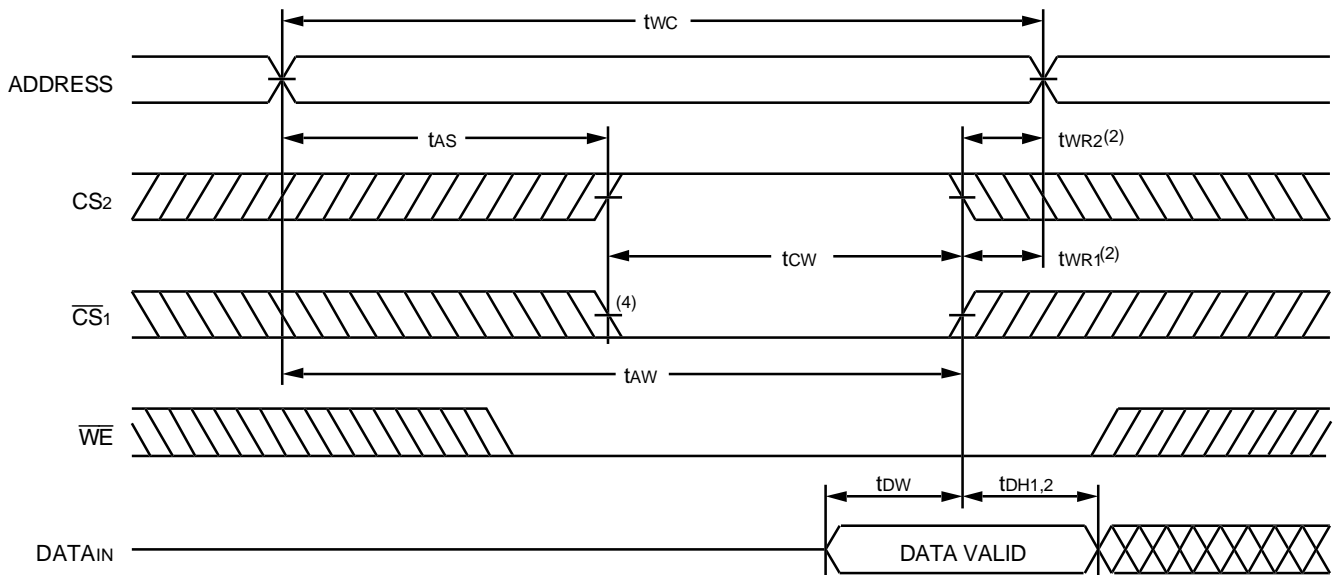
2967 drw 07

Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled Timing)^(1,5)



2967 drw 08

Timing Waveform of Write Cycle No. 2 (\overline{CS} Controlled Timing)⁽¹⁾

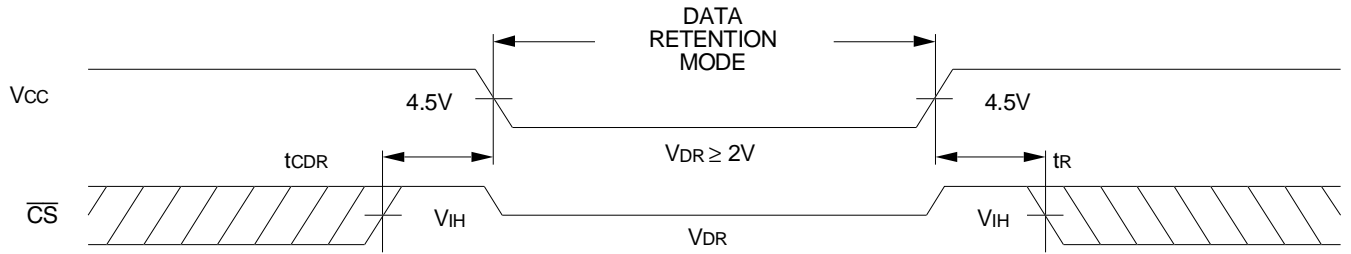


2967 drw 09

NOTES:

1. A write occurs during the overlap of a LOW \overline{WE} , a LOW $\overline{CS1}$ and a HIGH $CS2$.
2. $t_{WR1,2}$ is measured from the earlier of $\overline{CS1}$ or \overline{WE} going HIGH or $CS2$ going LOW to the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals must not be applied.
4. If the $\overline{CS1}$ LOW transition or $CS2$ HIGH transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
5. \overline{OE} is continuously HIGH. If \overline{OE} is LOW during a \overline{WE} controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{DW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified t_{WP} .
6. Transition is measured $\pm 200mV$ from steady state.

Low Vcc Data Retention Waveform



2967 drw 10

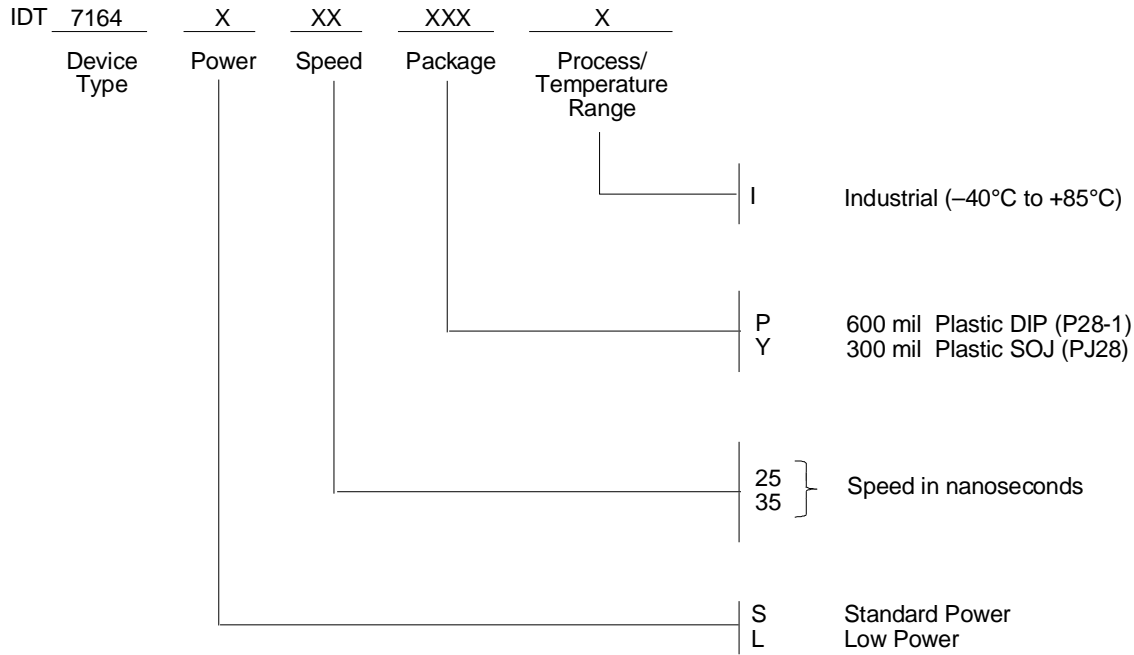
Ordering Information — Commercial

| IDT | 7164 | X | XX | XXX | X | |
|-------------|--------|----------------------|---------|----------------------------|-------|-----------------------------|
| Device Type | Power | Speed | Package | Process/ Temperature Range | | |
| | | | | | Blank | Commercial (0°C to +70°C) |
| | | | | | Y* | 300 mil SOJ (SO28-5) |
| | | | | | P** | 600 mil Plastic DIP (P28-1) |
| | | | | | TP* | 300 mil Plastic DIP (P28-2) |
| | | 15 20 25 35 | | | | Speed in nanoseconds |
| | S L | | | | | Standard Power Low Power |

* Available for 15ns and 20ns speed grades only.
** Available for 25ns and 35ns speed grades only.

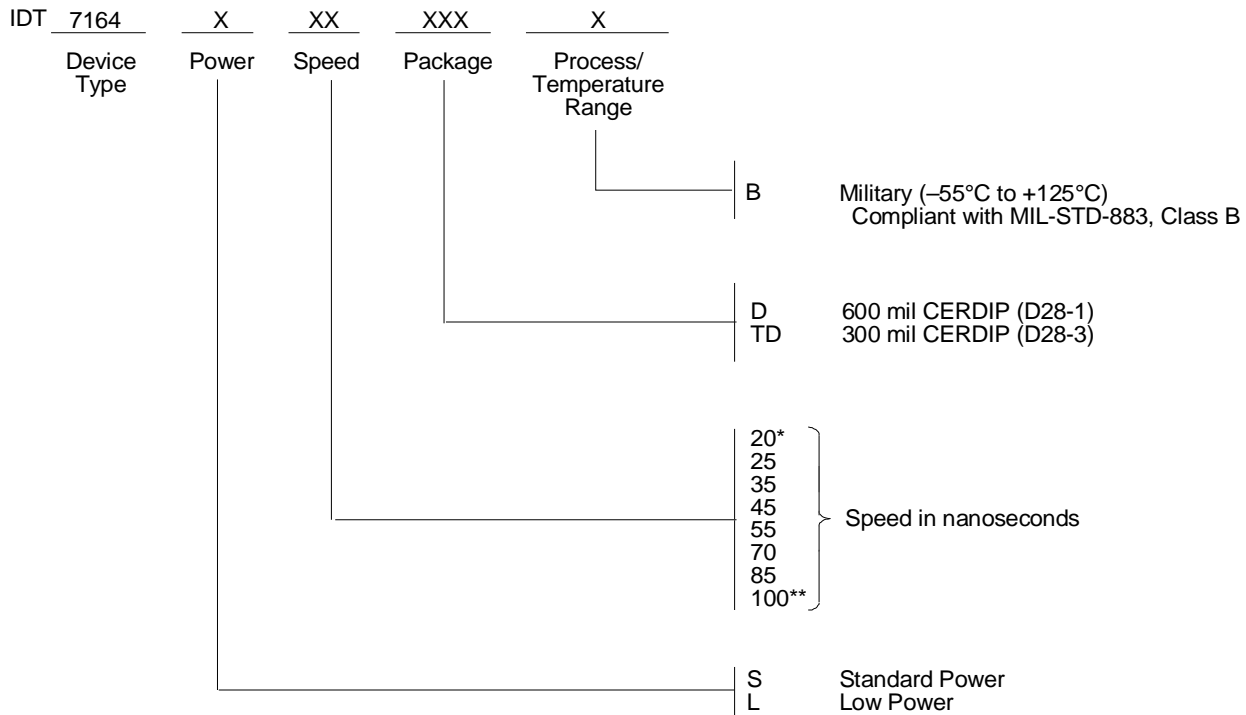
2967 drw 11

Ordering Information — Industrial



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Ordering Information — Military



* Available only in 600mil CERDIP (D28-1) and 300mil CERDIP (D28-1) and 300mil CERDIP (D28-3) packaging for a low power.
** Available only in 600 mil CERDIP (D28-1) packaging.

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Datasheet Document History

| | | |
|-----------|--------------------|--|
| 1/13/2000 | | Updated to new format |
| | Pp. 1, 2, 3, 5, 10 | Added Industrial Temperature range offerings |
| | Pp. 1, 3, 9 | Removed commercial 70ns speed grade offering |
| | Pp. 1, 3, 6, 10 | Added 100ns speed grade specification details |
| | Pg. 3 | Revised notes and footnotes in DC Electrical tables |
| | Pp. 5, 6 | Revised notes and footnotes in AC Electrical tables |
| | Pg. 8 | Removed Note 1 from Write Cycle No. 1 and No. 2 diagrams; renumbered notes and footnotes |
| | Pp. 9, 10 | Separated Ordering Information into commercial, industrial, and military offerings |
| | Pg. 11 | Added Datasheet Document History |
| 08/09/00 | | Not recommended for new designs |
| 02/01/01 | | Removed "Not recommended for new designs" |
| 12/07/01 | Pg. 10 | Add PJ28 to Industrial temperature. |



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