HT23C040

CMOS 512K×8-Bit Mask ROM

Features

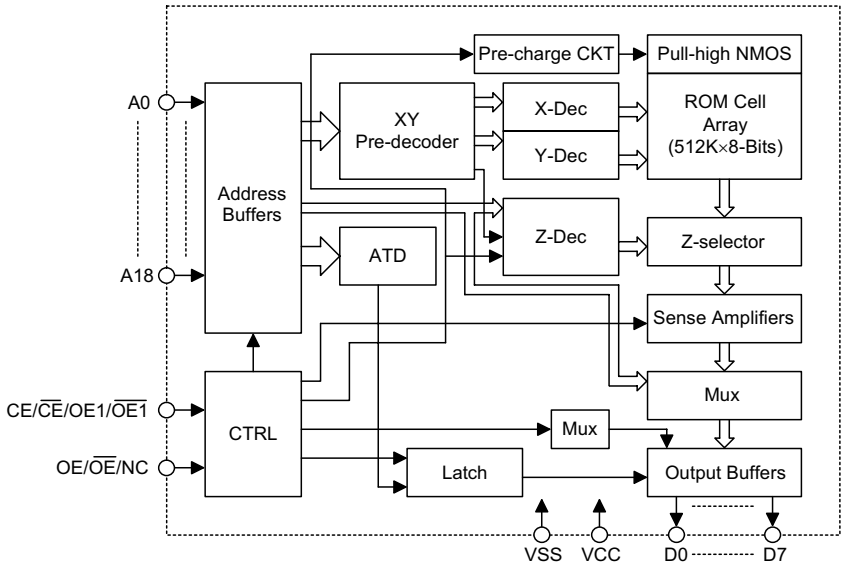
- Operating voltage: 2.7V~5.5V
- Low power consumption
  - Operation: 25mA max. (V_{CC}=5V)
    10mA max. (V_{CC}=3V)
  - Standby: 30μA max. (V_{CC}=5V)
    10μA max. (V_{CC}=3V)
- Access time: 120ns max. (V_{CC}=5V)
  250ns max. (V_{CC}=3V)
- 524288×8-bit of mask ROM
- Mask option: chip enable CE/$\overline{CE}$/OE1/$\overline{OE1}$, and output enable OE/$\overline{OE}$/NC
- TTL compatible inputs and outputs
- Tristate outputs
- Fully static operation
- Package type: 32-pin DIP/SOP

General Description

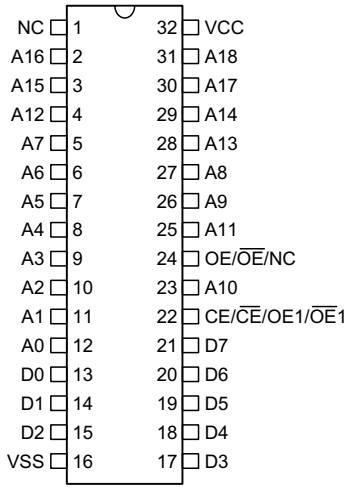
The HT23C040 is a read-only memory with high performance CMOS storage device whose 4096K of memory is arranged into 524288 word by 8 bits.

For application flexibility, the chip enable and output enable control pins can be selected as active high or active low. This flexibility not only allows easy interface with most microprocessors, but also eliminates bus contention in multiple bus microprocessor systems. An additional feature of the HT23C040 is its ability to enter the standby mode whenever the chip enable (CE/$\overline{CE}$) is inactive, thus reducing current consumption to below 30μA. The combination of these functions makes the chip suitable for high density low power memory applications.

Block Diagram



Pin Assignment



HT23C040
– 32 DIP/SOP

Pin Description

Pin Name	I/O	Description
NC	—	No connection
A0~A18	I	Address inputs
D0~D7	O	Data outputs
VSS	—	Negative power supply
CE/$\overline{CE}$/OE1/$\overline{OE1}$	I	Chip enable/Output enable input
OE/$\overline{OE}$/NC	I	Output enable input
VCC	—	Positive power supply

Operation Truth Table

Mode	CE/$\overline{CE}$	OE/$\overline{OE}$	A0~A18	D0~D7
Read	H/L	H/L	Valid	Data Out
Deselect	H/L	L/H	X	High Z
Standby	L/H	X	X	High Z

Note: H=V_{IH}, L=V_{IL}, X=V_{IH} or V_{IL}

Absolute Maximum Ratings

Supply Voltage.....–0.3V to 6V

Input Voltage .....–0.3V to V_{CC}+0.3V

Storage Temperature.....–50°C to 125°C

Operating Temperature .....–40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Supply voltage: 4.5V~5.5V T_a=–40°C to 85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{CC}	Operating Voltage	—	—	4.5	—	5.5	V
I_{CC1}	Operating Current	5V	O/P Unload, f=5MHz	—	—	25	mA
V_{IL1}	Input Low Voltage	5V	—	V_{SS}	—	0.8	V
V_{IH1}	Input High Voltage	5V	—	2.2	—	V_{CC}	V
V_{OL1}	Output Low Voltage	5V	I_{OL}=3.2mA	—	—	0.4	V
V_{OH1}	Output High Voltage	5V	I_{OH}=–1mA	2.4	—	V_{CC}	V
I_{LI}	Input Leakage Current	5V	V_{IN}=0 to V_{CC}	—	—	10	μA
I_{LO}	Output Leakage Current	5V	V_{OUT}=0 to V_{CC}	—	—	10	μA
I_{STB1}	Standby Current	5V	$\overline{CE}$=V_{IL} $\overline{CE}$=V_{IH}	—	—	1.5	mA
I_{STB2}	Standby Current	5V	$\overline{CE}$≤0.2V $\overline{CE}$≥V_{CC}–0.2V	—	—	30	μA
C_{IN}	Input Capacitance (See note)	—	f=1MHz	—	—	10	pF
C_{OUT}	Output Capacitance (See note)	—	f=1MHz	—	—	10	pF

Supply voltage: 2.7V~3.3V T_a=–40°C to 85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{CC}	Operating Voltage	—	—	2.7	—	3.3	V
I_{CC2}	Operating Current	3V	O/P Unload, f=5MHz	—	—	10	mA
V_{IL2}	Input Low Voltage	3V	—	V_{SS}	—	0.4	V
V_{IH2}	Input High Voltage	3V	—	1.5	—	V_{CC}	V
V_{OL2}	Output Low Voltage	3V	I_{OL}=2mA	—	—	0.4	V
V_{OH2}	Output High Voltage	3V	I_{OH}=–0.6mA	1.5	—	V_{CC}	V
I_{LI}	Input Leakage Current	3V	V_{IN}=0 to V_{CC}	—	—	10	μA
I_{LO}	Output Leakage Current	3V	V_{OUT}=0 to V_{CC}	—	—	10	μA
C_{IN}	Input Capacitance (See Note)	—	f=1MHz	—	—	10	pF
C_{OUT}	Output Capacitance (See Note)	—	f=1MHz	—	—	10	pF

Note: These parameters are periodically sampled but not 100% tested.

A.C. Characteristics

T_a=–40°C to 85°C

Symbol	Parameter	3V±10%		5V±10%		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	200	—	120	—	ns
t_{AA}	Address Access Time	—	250	—	120	ns
t_{ACE}	Chip Enable Access Time	—	250	—	120	ns
t_{AOE}	Output Enable Access Time	—	150	—	80	ns
t_{OH}	Output Hold Time	—	—	10	—	ns
t_{OD}	Output Disable Time (See Note)	—	—	—	70	ns
t_{OE}	Output Enable Time (See Note)	—	—	10	—	ns

Note: These parameters are periodically sampled but not 100% tested.

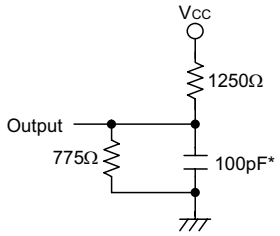
A.C. test condition

Output load: see figure right

Input rise and fall time: 10ns

Input pulse levels: 0.4V to 2.4V

Input and output timing reference levels:
0.8V and 2.0V (V_{CC}=5V)
1.5V (V_{CC}=3V)



* Including scope and jig

Output load circuit

Functional Description

The HT23C040 has two modes, namely data read mode and standby mode, controlled by CE/$\overline{CE}$/OE1/$\overline{OE1}$ and OE/$\overline{OE}$/NC inputs.

- Standby mode

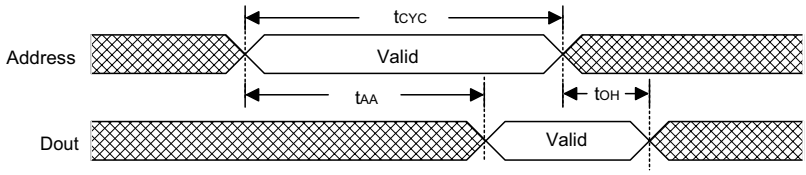
  The HT23C040 has lower current consumption, controlled by the chip enable input (CE/$\overline{CE}$). When a low/high level is applied to the CE/$\overline{CE}$ input regardless of the output enable (OE/$\overline{OE}$/NC) states, the chip will enter the standby mode.

- Data read mode

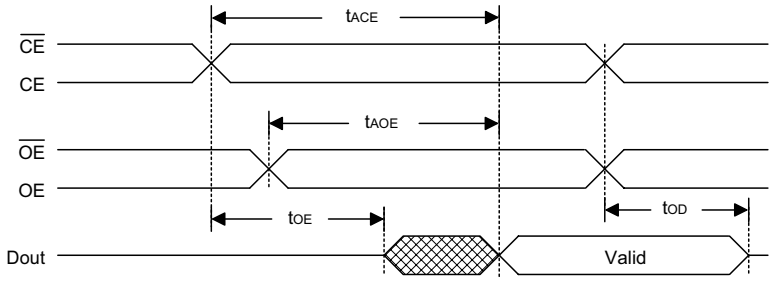
  When both the chip enable (CE/$\overline{CE}$/OE1/$\overline{OE1}$) and the output enable (OE/$\overline{OE}$/NC) are active, the chip is in data read mode. Otherwise, active CE/$\overline{CE}$ and inactive OE/$\overline{OE}$/NC result in deselect mode. The output will remain in Hi-Z state.

Timing Diagrams

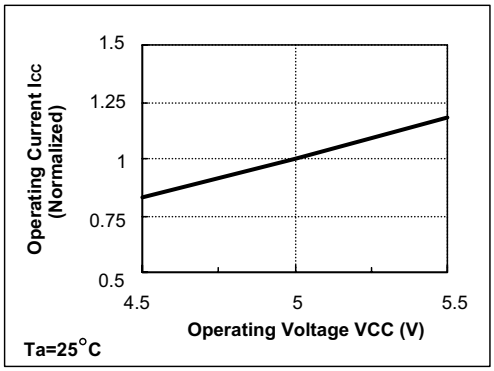
- Propagation delay due to address (CE/$\overline{CE}$/OE1/$\overline{OE1}$ and OE/$\overline{OE}$ are active)

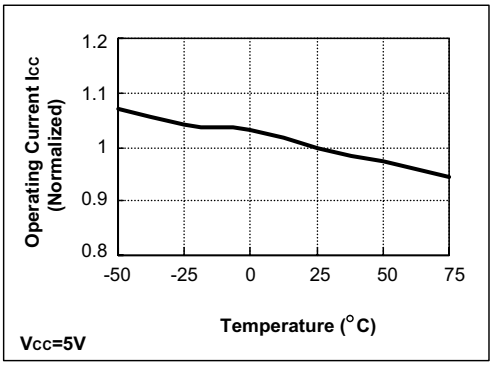


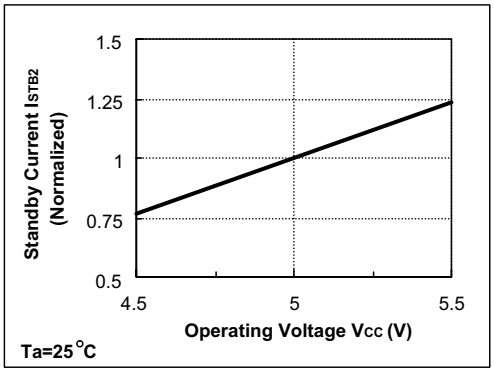
- Propagation delay due to chip and output enable (address valid)

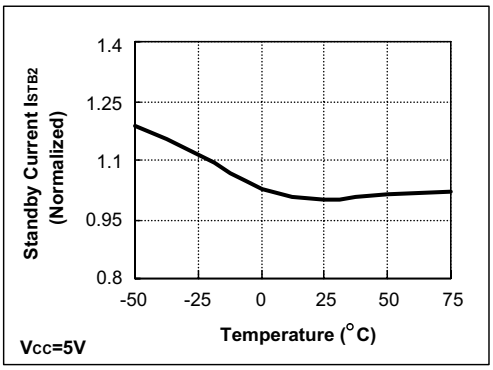


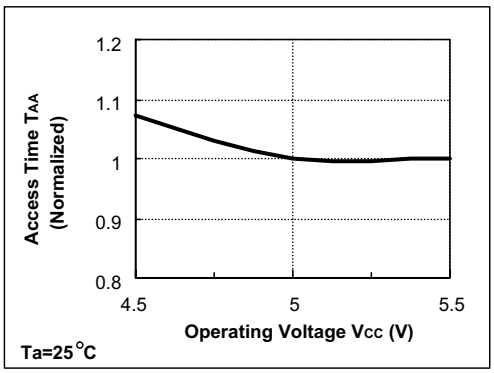
Characteristic Curves

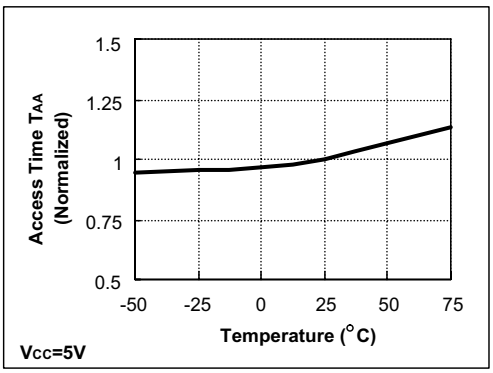


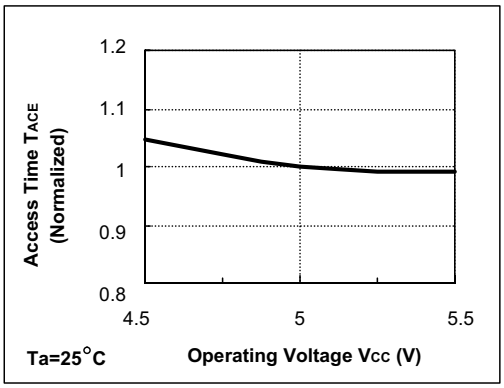


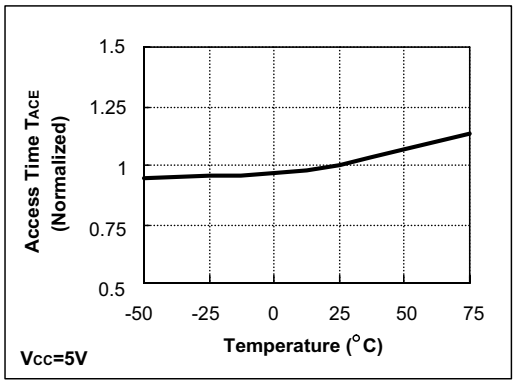


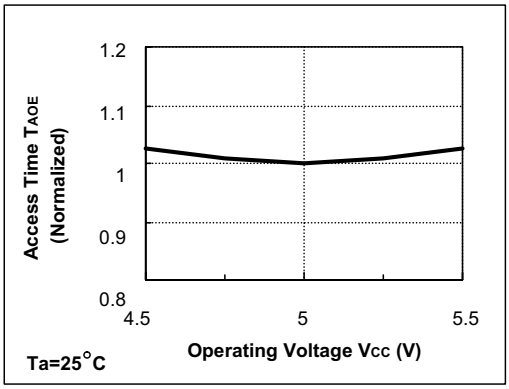


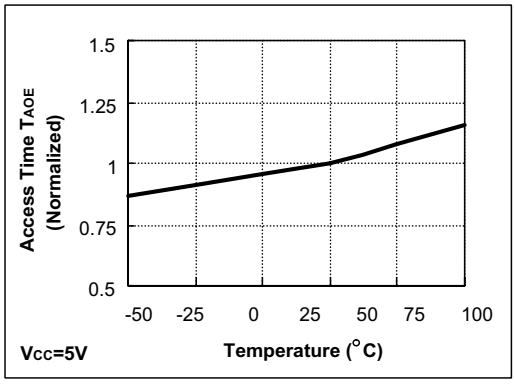





Access Time TACE (Normalized)
1.2
1.1
1
0.9
0.8
4.5
5
5.5
Ta=25°C
Operating Voltage VCC (V)


Access Time TACE (Normalized)
1.5
1.25
1
0.75
0.5
-50
-25
0
25
50
75
VCC=5V
Temperature (°C)


Access Time TAOE (Normalized)
1.2
1.1
1
0.9
0.8
4.5
5
5.5
Ta=25°C
Operating Voltage VCC (V)


Access Time TAOE (Normalized)
1.5
1.25
1
0.75
0.5
-50
-25
0
25
50
75
100
VCC=5V
Temperature (°C)

HT23C040 MASK ROM ORDERING SHEET

Custom:_____

Input Medium:

☐ **EPROM** ☐ **DISK** ☐ **File (Mail Address: romfile@holtek.com.tw)** ☐ **OTHER**_____

User No.	Type/Ref. Name	Q'ty	Check Sum	Memory Address	
				Start	End

Control Pin and Package Form Option:

(a) 32 Pin Type Pin 22:_____ **(1) CE (2)** $\overline{\textbf{CE}}$ **(3) OE1 (4)** $\overline{\textbf{OE1}}$

Pin 24:_____ **(1) OE (2)** $\overline{\textbf{OE}}$ **(3) NC**

(b) Package Form:_____ **(1) Chip Form (2) 32 DIP (3) 32 SOP**

Companion User No._____

Package Marking :_____

Delivery Date :_____ **Q'ty:** _____

CUSTOM CONFIRMED BY:

_____

(NAME, DATE, POSITION & CO. CHOP)

HOLTEK CONFIRMED BY:

_____ _____

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