

IR 3/16 Encode/Decode IC

Technical Data

**HSDL-7001-2500 pc, tape
and reel**
**HSDL-7001#100-100pc,
50/tube**

Features

- **Compliant with IrDA 1.0 Physical Layer Specs**
- **Interfaces with IrDA 1.0 Compliant IR Transceivers**
- **Used in Conjunction with Standard 16550 UART**
- **Transmits/Receives either 1.63 μ s or 3/16 Pulse Mode**
- **Internal or External Clock Modes**
- **Programmable Baud Rate**
- **2.7-5.5 V Operation**
- **16 Pin SOIC Package**

Applications

- **Interfaces with IR Transceivers in:**
 - **Computer Applications:**
 - Notebook Computers
 - Sub-notebooks
 - Desktop PCs
 - PDA's
 - Printers
 - Dongle or other RS-232 adapter
 - **Telecom Applications:**
 - Modems
 - Fax Machines
 - Pagers
 - Phones
 - **Handheld Data Collection:**
 - Industrial
 - Medical
 - Transportation

Description

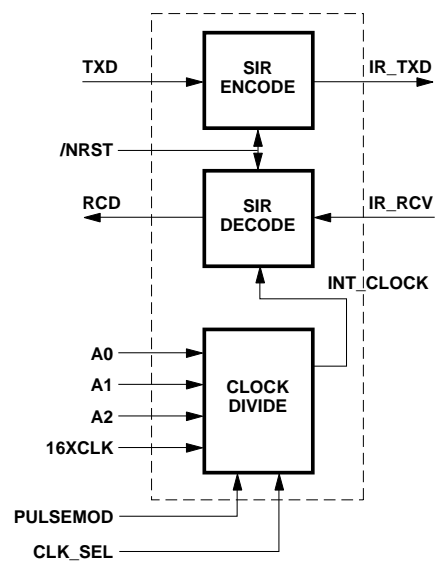
The HSDL-7001 modulates and demodulates electrical pulses from Hewlett-Packard's HSDL-1001 Infrared transceiver module and other IrDA-compliant transceivers. The HSDL-7001 can be used with a microcontroller/microprocessor that has a serial communication interface (UART). Prior to communication, the processor selects the transmission baud rate. Serial data is then transmitted or received at the prescribed data rate.

The HSDL-7001 consists of two state machines – the SIR (Serial InfraRed) Encode and SIR Decode blocks. It also contains a sequential block Clock Divide which synthesizes the required internal signal.

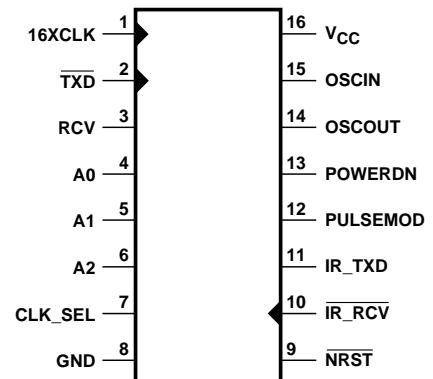
The HSDL-7001 can be placed into the Internal Clock Mode or External Clock Mode. An external crystal is needed for the Internal Clock Mode. In applications where the external 16XCLK signal is provided, a crystal is not needed.

There are two data transmission modes. Data can be transmitted and received in either a standard 3/16 modulation mode or a 1.63 μ s pulse mode.

Schematic



Pin Out



I/O Pinout List

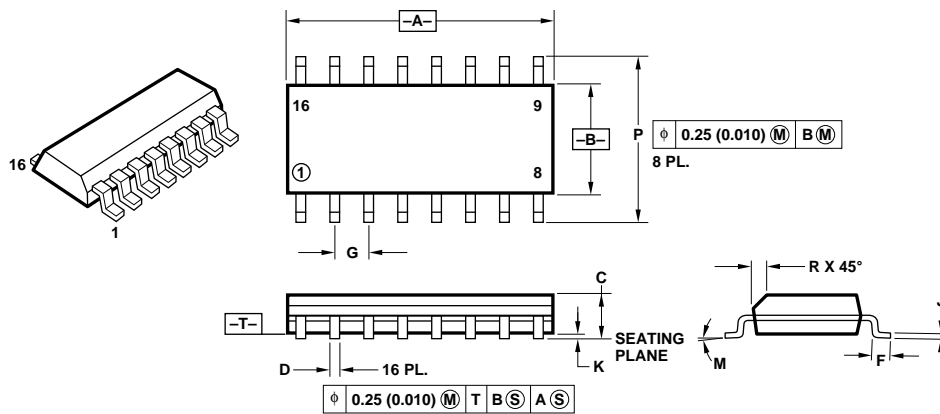
| Pin | Name | Type | Function |
|-----|---------------------|-----------------------------|--|
| 1 | 16XCLK (SIXTNCK) | DIGIN | Positive edge triggered input clock that is set to 16 times the data transmission baud rate. The encode and decode schemes require this signal. The signal is usually tied to a UART's BAUDOUT signal. The 16XCLK may be provided by application circuitry if BAUDOUT is not available. This signal is required when the internal clock is not used. |
| 2 | /TXD | DIGIN | Negative edge triggered input signal that is normally tied to the SOUT signal of the UART (serial data to be transmitted). Data is modulated and output as IR_TXD. |
| 3 | RCV | DIGOUT | Output signal normally tied to SIN signal of a UART (received serial data). RCV is the demodulated output of IR_RVC. |
| 4 | A0 | DIGIN | Clock Multiplex Signal |
| 5 | A1 | DIGIN | Clock Multiplex Signal |
| 6 | A2 | DIGIN | Clock Multiplex Signal |
| 7 | CLK_SEL | DIGIN | Used to activate either the Internal or External Clock. A high on this line activates the External clock (16XCLK) and a low activates the Internal clock. When the External clock is activated, the internal oscillator is put in POWERDOWN MODE. |
| 8 | GND | | Chip Ground |
| 9 | /NRST | DIGIN | Active low signal used to reset the IrDA-SIR ENCODE & DECODE state machine. This signal can be tied to POR (Power On Reset) or V _{CC} . |
| 10 | /IR_RCV | DIGIN | Input from SIR optoelectronics. Input signal is a 3/16th or 1.6 μs pulse which is demodulated to generate RCV output signal. |
| 11 | IR_TXD | DIGOUT | This is the modulated TXD signal. |
| 12 | PULSEMOD | DIGIN (with pulldown) | A high level on this input puts the chip into the monoshot transmit mode. In this mode, when there is a negative transition on the TXD input, a rising edge on the internal transmit modulation state machine will activate a high pulse on IR_TXD for 6 crystal clock cycles. With a 3.6864 MHz crystal, this corresponds to 1.63 μs. This mode cannot be used in conjunction with the 16XCLK clock. It is meant to be used with the external crystal clock. By default, this input pin is pulled to GND. |
| 13 | POWERDN | DIGIN (with pulldown) | A high on this input puts only the internal oscillator cell (OSCII) in POWERDOWN MODE. The cell is normally not powered down. |
| 14 | OSCOUT | ANAOOUT | Oscillator Output |
| 15 | OSCIN | ANAIN | Oscillator Input |
| 16 | V _{CC} | | Power |

Note: There are two methods of putting the internal oscillator cell in POWERDOWN MODE. Whenever the CLKSEL Pin is asserted high (External clock selected) the oscillator cell is automatically put in powerdown mode, or whenever the POWERDN Pin is asserted high.

Table 1. Selection of Internal Clock Rate from Crystal Oscillator

| Selected Clock Rate (bps) | A2 | A1 | A0 | Crystal Freq. Division |
|---------------------------|----|----|----|------------------------|
| 115200 | 0 | 0 | 0 | Divided by 2 |
| 57600 | 0 | 0 | 1 | Divided by 4 |
| 19200 | 0 | 1 | 0 | Divided by 12 |
| 9600 | 0 | 1 | 1 | Divided by 24 |
| 38400 | 1 | 0 | 0 | Divided by 6 |
| 4800 | 1 | 0 | 1 | Divided by 48 |
| 2400 | 1 | 1 | 0 | Divided by 96 |
| TEST PURPOSE | 1 | 1 | 1 | No division |

Package Dimensions

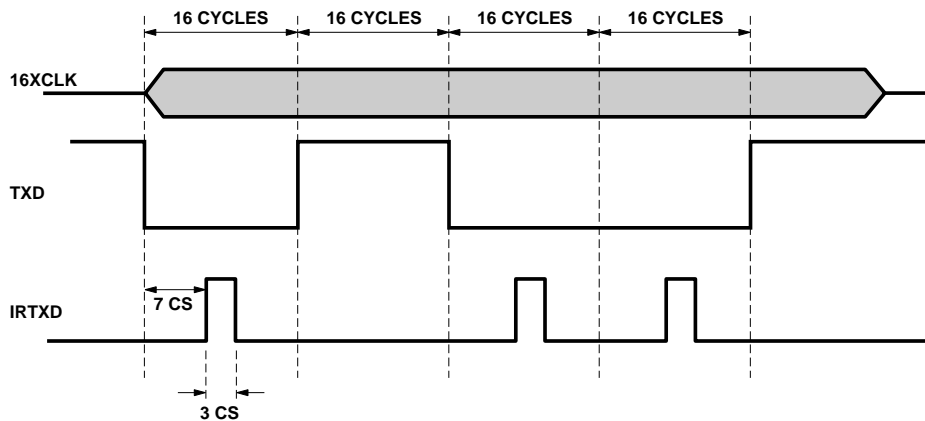


NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.060 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

Encoding Scheme

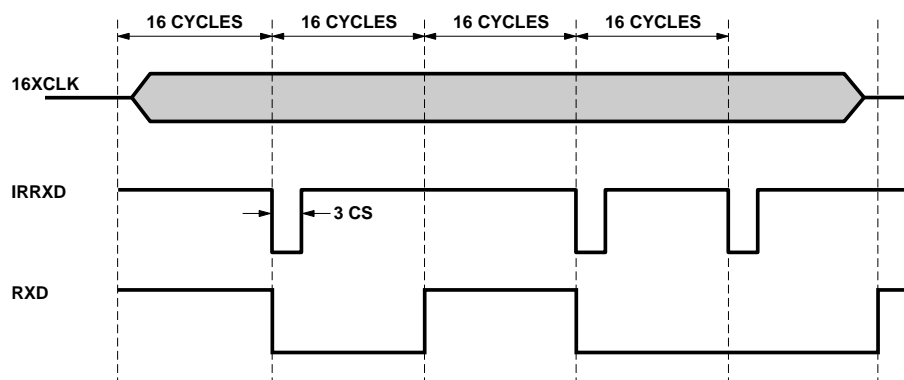


The encoding scheme relies on a clock being present, which is set to 16 times the data transmission baud rate (16XCLX). The encoder sends a pulse for every space or “0” that is sent on the TXD line. On a high to low transition of the TXD line, the generation of the

pulse is delayed for 7 clock cycles of the 16XCLK before the pulse is set high for 3 clock cycles (or $3/16$ th of a bit time) and then subsequently pulled low. This generates a $3/16$ th bit time pulse centered around the bit of information (“0”) that is being transmitted.

For consecutive spaces, pulses with a 1 bit time delay are generated in series. If a logic 1 (mark) is sent then the encoder does not generate a pulse.

Decoding Scheme



The IrDA-SIR (Serial InfraRed) decoding modulation method can be thought of as a pulse stretching scheme.

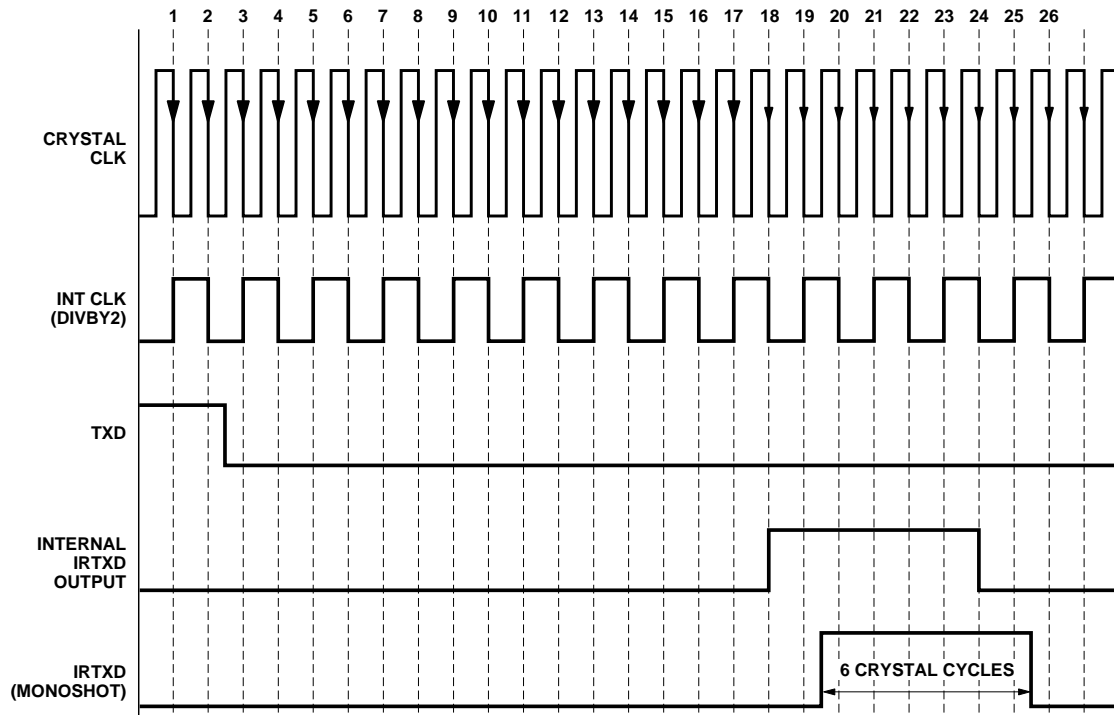
Every high to low transition of the IR_RXD line signifies the

arrival of a pulse. This pulse needs to be stretched to accommodate 1 bit time (or 16 16XCLK cycles). Every pulse that is received is translated into a “0” or space on the RXD line equal to 1 bit time.

Note 1: The stretched pulse must be at least $3/4$ of a bit time in duration to be correctly interpreted by a UART.

Note 2: It is recommended that TXD remains high when not transmitting. This ensures the LED is off and will not interfere with signal reception.

Monoshot Operation



The figure above illustrates the operation of the monoshot when the internal clock is set to divide by 2 mode, i.e., when $A2=0$, $A1=0$, and $A0=0$. A rising edge on the internal modulation state machine (IRTXD OUTPUT), will cause the output on the IRTXD to go up for 6 crystal clock cycles.

With a 3.6864 MHz clock, this corresponds to a pulse of $1.63 \mu\text{s}$. The duration of this pulse is independent of the code $A2$, $A1$, $A0$ and is always 6 clock cycles of the crystal, corresponding to the monoshot operation.

Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|-------------------------------------|-----------|------|----------------|-------|
| Storage Temperature | T_S | -65 | +150 | °C |
| Operating Temperature | T_A | -40 | +85 | °C |
| Output Current | I_O | -100 | 100 | mA |
| Power Dissipation ^[1] | P_{MAX} | | 0.46 | W |
| Input/Output Voltage ^[2] | V_I/V_O | -0.5 | $V_{CC} + 0.5$ | V |
| Power Supply Voltage | V_{CC} | -0.5 | 7.0 | V |
| Electrostatic Protection | V_{ESD} | | 4000 | V |

Notes:

1. Maximum power dissipation is given for $R_{th} = 140$ C/W (SO 16 Plastic).
2. All pins are protected from damage to static discharge by internal diode clamps to V_{CC} and GND.

Switching Specifications

($V_{CC} = 2.7$ to 5.5 V, $T_A = -20$ to $+85$ °C)

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|------------|-----------|------------|------------|-------|--|
| Propagation Delay Time ^[1] | t_{pd} | | | 80 | ns | |
| Output Rise Time ^[2] | t_{rise} | 3.7 10 | 7.25 16 | 11.6 24 | ns | $V_{CC} = 5.5$ V, $CL = 50$ pF $V_{CC} = 2.7$ V, $CL = 50$ pF |
| Output Fall Time ^[3] | t_{fall} | 4.4 11 | 8.35 16 | 11.2 26 | ns | $V_{CC} = 5.5$ V, $CL = 50$ pF $V_{CC} = 2.7$ V, $CL = 50$ pF |
| Output Capacitance on Output Pads Used for Simulation | C_{OUT} | | | 50 | pF | |

Notes:

1. Propagation Delay Time in the output buffer is the time taken from the input passing $V_{CC}/2$ to the time of the output reaching $V_{CC}/2$ with 50 pF as the output load.
2. The Output Rise Time is the time taken for the outputs (RCV, IR_TXD) to rise from 10% of the original value to 90% of the final value.
3. The Output Fall Time is the time taken for the outputs (RCV, IR_TXD) to fall from 90% of the original value to 10% of the final value.

Recommended Operating Conditions

($V_{CC} = 2.7$ to 5.5 V, $T_A = -20$ to $+85^\circ\text{C}$)

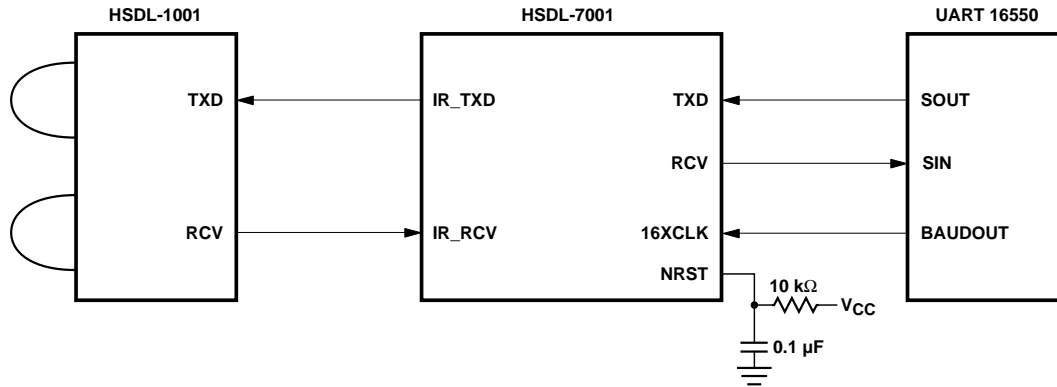
| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|--|----------------|--------------|--------------|--------------|--------------------------------|--------------------------------------|
| Supply Voltage | V_{CC} | 2.7 | 5 | 5.5 | V | |
| Input Voltage | V_I | 0.0 | | V_{CC} | V | |
| Ambient Temperature | T_A | -20 | | +85 | $^\circ\text{C}$ | |
| High Level Input Voltage | V_{IH} | 0.7 V_{CC} | | V_{CC} | V | |
| Low Level Input Voltage | V_{IL} | 0 | | 0.3 V_{CC} | V | |
| Output High Voltage | V_{OH} | 2.2 | | | V | $V_{CC} = 2.7$ V $i_{oh} = 2$ mA |
| Output Low Voltage | V_{OL} | | | 0.5 | V | $V_{CC} = 2.7$ V $i_{ol} = 2$ mA |
| Output High Voltage | V_{OH} | 4.5 | | | V | $V_{CC} = 5.5$ V $i_{oh} = 2$ mA |
| Output Low Voltage | V_{OL} | | | 0.5 | V | $V_{CC} = 5.5$ V $i_{ol} = 2$ mA |
| Static Power Dissipation | P_{STAT} | | 0.44 0.11 | 0.61 0.15 | mW mW | $V_{CC} = 5.5$ V $V_{CC} = 2.7$ V |
| Dynamic Power Dissipation | P_{DYN} | | 11 5.4 | 16.5 8.1 | mW mW | $V_{CC} = 5.5$ V $V_{CC} = 2.7$ V |
| Static Current Consumption | I_{STAT} | | 80 40 | 110 54 | μA μA | $V_{CC} = 5.5$ V $V_{CC} = 2.7$ V |
| Dynamic Current Consumption | I_{DYN} | | 2 2 | 3 3 | mA mA | $V_{CC} = 5.5$ V $V_{CC} = 2.7$ V |
| Max Clk Frequency (16XCLK) ^[1] | f_{16XCLK} | | | 2 | MHz | |
| Minimum Pulse Width (IR_TXD) ^[2] | t_{mpw} | 1630 | | | ns | |
| Pulse Width on Monoshot (IR_TXD and IR_RCV) | t_{mpw} | 1630 | 1710 | 1730 | ns | |
| Value of Pulldown Resistor Used on POWERDOWN & PULSEMOD Input Pins | R_{DWN} | 114 | 152 | 256 | K Ω | |
| Trigger Low Level Input Voltage (For /NRST Input Pin) | V_{IL_TRIG} | 0.7 1.9 | 0.8 1.95 | 0.9 2.00 | V | $V_{CC} = 2.7$ V $V_{CC} = 5.5$ V |
| Trigger High Level Input Voltage (For /NRST Input Pin) | V_{IH_TRIG} | 1.7 3.25 | 1.85 3.4 | 1.9 3.60 | V | $V_{CC} = 2.7$ V $V_{CC} = 5.5$ V |

Notes:

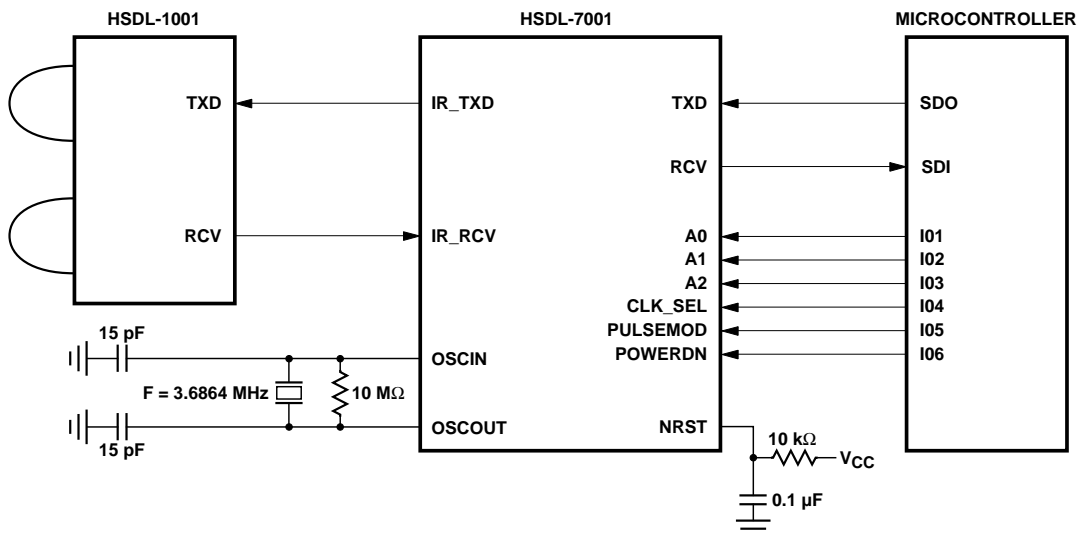
1. IrDA Parameters. The Max Clk Frequency represents the maximum clock frequency to drive the HSDL-7001's internal state machine. Under normal circumstances, the clock input should not exceed $16 * 115.2$ Kbps or 1.8432 MHz. This product can operate at higher clock rates, but the above is the recommended rate.
2. The Minimum Pulse Width (t_{mpw}) represents the minimum pulse width of the encoded IR_TXD pulse (and the IR_RCV pulse). As per the IrDA specifications, the minimum pulse width of the IR_TXD and IR_RCV pulses should be $3 * (1/1.8432 \text{ MHz})$ or 1.63 μs .

Application Circuits

HSDL-7001 Connection to UART



HSDL-7001 Connected to Microcontroller



NOTE: POWERDN CAN BE USED AS A BASIC CHIP SELECT.
THE HSDL-7001 WILL NOT BE ABLE TO RECEIVE OR TRANSMIT DATA WHILE POWERDN IS ASSERTED.

www.hp.com/go/ir

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

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Far East/Australasia: Call your local HP sales office.

Japan: (81 3) 3335-8152

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Data subject to change.

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Obsoletes 5965-5150E (11/96)

5968-7456E (8/99)