CCD Signal Processor with Vertical Driver and *Precision Timing* ™ Generator

AD9925

FEATURES

Integrated 10-channel V-driver
Register-compatible with the AD9991 and AD9995
3-field (6-phase) vertical clock support
2 additional vertical outputs for advanced CCDs
Complete on-chip timing generator
***Precision Timing* core with <600 ps resolution**
Correlated double sampler (CDS)
6 dB to 42 dB 10-bit variable gain amplifier (VGA)
12-bit 36 MHz ADC
Black level clamp with variable level control
On-chip 3 V horizontal and RG drivers
2-phase and 4-phase H-clock modes
Electronic and mechanical shutter support
On-chip driver for external crystal
On-chip sync generator with external sync input
8 mm × 8 mm CSPBGA package with 0.65 mm pitch

APPLICATIONS

Digital still cameras
Digital video camcorders
CCD camera modules

GENERAL DESCRIPTION

The AD9925 is a complete 36 MHz front end solution for digital still camera and other CCD imaging applications. Based on the AD9995 product, the AD9925 includes the analog front end and a fully programmable timing generator (AFETG), combined with a 10-channel vertical driver (V-driver). A *Precision Timing* core allows adjustment of high speed clocks with approximately 600 ps resolution at 36 MHz operation.

The on-chip V-driver supports up to 10 channels for use with 3-field (6-phase) CCDs. Two additional vertical outputs can be used with CCDs that contain advanced video readout modes. Voltage levels of up to +15 V and −8 V are supported.

The analog front end includes black level clamping, CDS, VGA, and a 12-bit ADC. The timing generator and V-driver provide all the necessary CCD clocks: RG, H-clocks, vertical clocks, sensor gate pulses, substrate clock, and substrate bias control. The internal registers are programmed using a 3-wire serial interface.

Packaged in an 8 mm × 8 mm CSPBGA, the AD9925 is specified over an operating temperature range of −25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

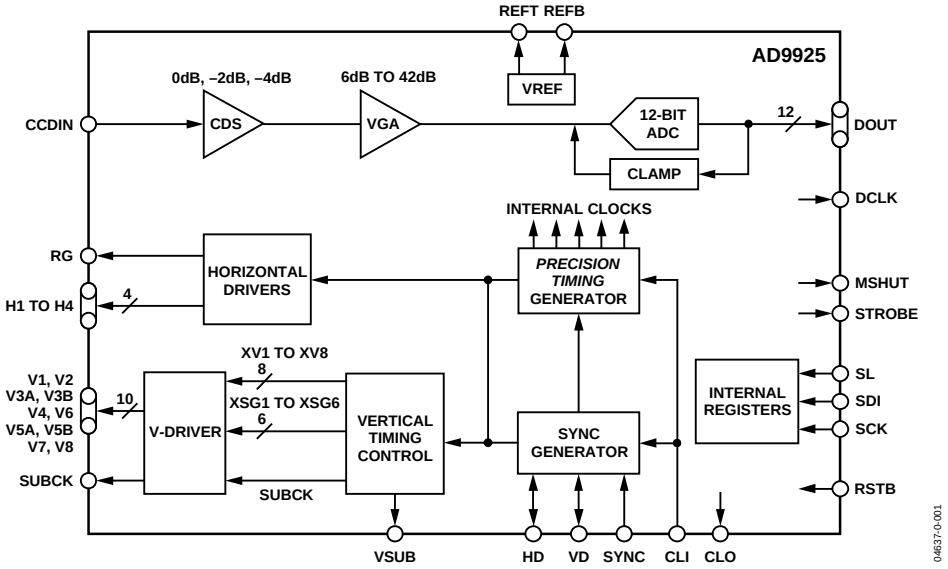

Figure 1.

Rev. A

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4/04—Revision 0: Initial Version

SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	–25		+85	°C
Storage	–65		+150	°C
POWER SUPPLY VOLTAGES				
AVDD (AFE Analog Supply)	2.7	3.0	3.6	V
TCVDD (Timing Core Analog Supply)	2.7	3.0	3.6	V
RGVDD (RG Driver)	2.7	3.0	3.6	V
HVDD (H1 to H4 Drivers)	2.7	3.0	3.6	V
DRVDD (Data Output Drivers)	2.7	3.0	3.6	V
DVDD (Digital)	2.7	3.0	3.6	V
V-DRIVER SUPPLY VOLTAGES				
VDVDD (V-Driver Input Logic Supply)	2.7	3.0	3.6	V
VH1, VH2 (V-Driver High Supply for 3-Level Outputs)	10.5	15.0	16.0	V
VM1, VM2 (V-Driver Mid Supply for 3-Level and 2-Level Outputs)	–1.0	0.0	+3.0	V
VL1, VL2 (V-Driver Low Supply for 3-Level and 2-Level Outputs)	–10.0	–7.5	–6.0	V
POWER DISSIPATION—AFETG Section Only (see Figure 9 for Power Curves)				
36 MHz, 3.0 V Supply, 100 pF Load on Each H1 to H4 Output, 20 pF RG Load		370		mW
Standby 1 Mode		10		mW
Standby 2 Mode		10		mW
Standby 3 Mode		1		mW
Power from HVDD Only[1]		130		mW
Power from RGVDD Only		10		mW
Power from AVDD Only		105		mW
Power from TCVDD Only		42		mW
Power from DVDD Only		57		mW
Power from DRVDD Only		26		mW
POWER DISSIPATION—V-Driver Section Only (VDVDD, VH, VL)				
Normal Operation (VH = 15.0 V, VL = –7.5 V)[2]		60		mW
Standby 1 Mode[2]		70		mW
Standby 2 Mode[2]		70		mW
Standby 3 Mode[2]		110		mW
MAXIMUM CLOCK RATE (CLI)	36			MHz

[1] The total power dissipated by the HVDD supply may be approximated using the equation *Total HVDD Power* = [C_{LOAD} × *HVDD* × *Pixel Frequency*] × *HVDD*. Reducing the H-loading and/or using a lower HVDD supply will reduce the power dissipation. C_{LOAD} is the total capacitance seen by all H-outputs.

[2] The power dissipated by the V-driver circuitry depends on the logic states of the inputs as well as actual CCD operation; default dc values are used for each measurement, in each mode of operation. Load conditions are described in the Vertical Driver Specifications section.

DIGITAL SPECIFICATIONS

RGVDD = HVDD = DVDD = DRVDD = 2.7 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS (Powered by DVDD, DRVDD)					
High Level Output Voltage at I_{OH} = 2 mA	V_{OH}	VDD – 0.5			V
Low Level Output Voltage at I_{OL} = 2 mA	V_{OL}			0.5	V
RG and H-DRIVER OUTPUTS (Powered by HVDD, RGVDD)					
High Level Output Voltage at Maximum Current		VDD – 0.5			V
Low Level Output Voltage at Maximum Current				0.5	V
Maximum Output Current (Programmable)		30			mA
Maximum Load Capacitance (for Each Output)		100			pF

VERTICAL DRIVER SPECIFICATIONS

VDVDD = 3.3 V, VH = 15 V, VM = 0 V, VL = −7.5 V, C_L shown in load model, 25°C.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
3-LEVEL OUTPUTS (V1, V2, V3A, V3B, V5A, V5B)					
(Simplified Load Conditions, 6000 pF to Ground)					
Delay Time, VL to VM and VM to VH	t_{PLM}, t_{PMH}			100	ns
Delay Time, VM to VL and VH to VM	t_{PML}, t_{PHM}			200	ns
Rise Time, VL to VM and VM to VH	t_{RLM}, t_{RMH}			500	ns
Fall Time, VM to VL and VH to VM	t_{FML}, t_{FHM}			500	ns
Output Currents					
At −7.25 V			10.0		mA
At −0.25 V			−5.0		mA
At +0.25 V			5.0		mA
At +14.75 V			−7.2		mA
2-LEVEL OUTPUTS (V4, V6, V7, V8)					
(Simplified Load Conditions, 6000 pF to Ground)					
Delay Time, VL to VM	t_{PLM}			100	ns
Delay Time, VM to VL	t_{PML}			200	ns
Rise Time, VL to VM	t_{RLM}			500	ns
Fall Time, VM to VL	t_{FML}			500	ns
Output Currents					
At −7.25 V			10.0		mA
At −0.25 V			−5.0		mA
SUBCK OUTPUT					
(Simplified Load Conditions, 1000 pF to Ground)					
Delay Time, VL to VH	t_{PLH}			100	ns
Delay Time, VH to VL	t_{PHL}			200	ns
Rise Time, VL to VH	t_{RLH}			200	ns
Fall Time, VH to VL	t_{FHL}			200	ns
Output Currents					
At −7.25 V			5.4		mA
At +14.75 V			−4.0		mA
SERIAL VERTICAL CLOCK RESISTANCE			30		Ω
GND VERTICAL CLOCK RESISTANCE			10		Ω

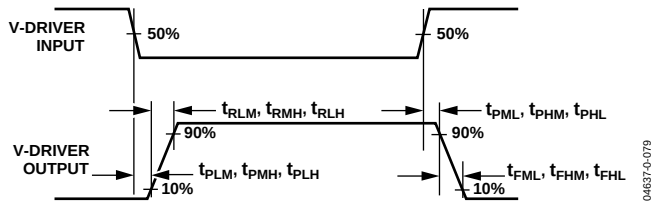


Figure 2. Definition of V-Driver Timing Specifications

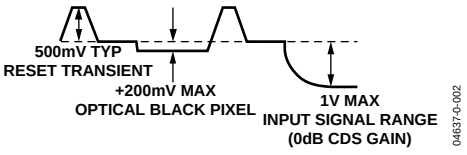
ANALOG SPECIFICATIONS

AVDD1 = 3.0 V, f_{CLI} = 36 MHz, typical timing specifications, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CDS					Input Characteristics Definition.[1]
Allowable CCD Reset Transient		500		mV	
Maximum Input Range before Saturation					
0 dB CDS Gain (Default Setting)		1.0		V p-p	
−2 dB CDS Gain		1.25		V p-p	
−4 dB CDS Gain		1.6		V p-p	
Maximum CCD Black Pixel Amplitude		+200/−100		mV	Positive Offset Definition[1]
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Minimum Gain (VGA Code 0)		6		dB	
Maximum Gain (VGA Code 1023)		42		dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		256		Steps	
Clamp Level					Measured at ADC Output.
Minimum Clamp Level (Code 0)		0		LSB	
Maximum Clamp Level (Code 255)		255		LSB	
ANALOG-TO-DIGITAL CONVERTER (ADC)					
Resolution	12			Bits	
Differential Nonlinearity (DNL)	−1.0	±0.5	+1.0	LSB	
No Missing Codes		Guaranteed			
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		2.0		V	
Reference Bottom Voltage (REFB)		1.0		V	
SYSTEM PERFORMANCE					Includes Entire Signal Chain.
Gain Accuracy					
Low Gain (VGA Code 0)	5.0	5.5	6.0	dB	Gain = (0.0351 × Code) + 5.5 dB.
Maximum Gain (VGA Code 1023)	40.5	41.5	42.5	dB	
Peak Nonlinearity, 500 mV Input Signal		0.1		%	12 dB Gain Applied.
Total Output Noise		0.8		LSB rms	AC Grounded Input, 6 dB Gain Applied.
Power Supply Rejection (PSR)		50		dB	Measured with Step Change on Supply.

[1] Input signal characteristics are defined as



TIMING SPECIFICATIONS

C_L = 20 pF, AVDD = DVDD = DRVDD = 3.0 V, f_{CLI} = 36 MHz, unless otherwise noted.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
MASTER CLOCK, CLI (Figure 17)					
CLI Clock Period	t_{CONV}	27.8			ns
CLI High/Low Pulse Width		11.2	13.9	16.6	ns
Delay from CLI Rising Edge to Internal Pixel Position 0	t_{CLIDLY}		6		ns
AFE CLPOB PULSE WIDTH[1, 2] (Figure 23 and Figure 29)		2	20		Pixels
AFE SAMPLE LOCATION[1] (Figure 20)					
SHP Sample Edge to SHD Sample Edge	t_{S1}	12.5	13.9		ns
DATA OUTPUTS (Figure 21 and Figure 22)					
Output Delay from DCLK Rising Edge, Default Value[1]	t_{OD}		8		ns
Inhibited Area for DOUTPHASE Edge Location[1]	$t_{DOUTINH}$	SHDLOC		SHDLOC + 11	
Pipeline Delay from SHP/SHD Sampling to DOUT		11			Cycles
SERIAL INTERFACE (Figure 74 and Figure 75)					
Maximum SCK Frequency	f_{SCLK}	36			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns
SCK Falling Edge to SDATA Valid Read	t_{DV}	10			ns

[1] Parameter is register-programmable.
[2] Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	With Respect To	Min	Max	Unit
VDVDD	VDVSS	VDVSS – 0.3	VDVSS + 4	V
VL	VDVSS	VDVSS – 10	VDVSS + 0.3	V
VH1, VH2	VDVSS	VL – 0.3	VL + 27	V
VM1, VM2	VDVSS	VL – 0.3	VL + 27	V
AVDD	AVSS	–0.3	+3.9	V
TCVDD	TCVSS	–0.3	+3.9	V
HVDD	HVSS	–0.3	+3.9	V
RGVDD	RGVSS	–0.3	+3.9	V
DVDD	DVSS	–0.3	+3.9	V
DRVDD	DRVSS	–0.3	+3.9	V
RG Output	RGVSS	–0.3	RGVDD + 0.3	V
H1 to H4 Output	HVSS	–0.3	HVDD + 0.3	V
Digital Outputs	DVSS	–0.3	DVDD + 0.3	V
Digital Inputs	DVSS	–0.3	DVDD + 0.3	V
SCK, SL, SDATA	DVSS	–0.3	DVDD + 0.3	V
REFT/REFB, CCDIN	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Lead Temperature, 10 s			350	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS

Thermal Resistance

CSPBGA Package: θJA = 40.3°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

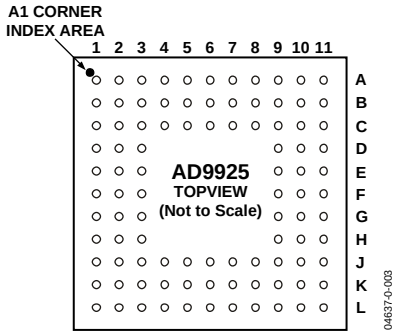


Figure 3. 96-Lead CSPBGA Package Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description[2]
E1, F2, F3	HVSS	P	H1 to H4, HL Driver Ground
G2, G3	HVSS	P	H1 to H4, HL Driver Ground
F1	H1	DO	CCD Horizontal Clock 1
G1	H2	DO	CCD Horizontal Clock 2
H1, H2, H3	HVDD	P	H1 to H4, HL Driver Supply
J2, J3	HVDD	P	H1 to H4, HL Driver Supply
J1	H3	DO	CCD Horizontal Clock 3
K1	H4	DO	CCD Horizontal Clock 4
K2, L2	RGVSS	P	RG Driver Ground
L3	RG	DO	CCD Reset Gate Clock
L4	RGVDD	P	RG Driver Supply
K3, K4	TCVDD	P	Analog Supply for Timing Core
J4	CLO	DO	Clock Output for Crystal
J5	SYNC	DI	External System Sync Input
K5, L5	TCVSS	P	Analog Ground for Timing Core
J6	CLI	DI	Reference Clock Input
K6, L7	AVSS	P	Analog Ground for AFE
L6	CCDIN	AI	CCD Signal Input
K7	AVDD	P	Analog Supply for AFE
L8	REFT	AO	Voltage Reference Top Bypass
L9	REFB	AO	Voltage Reference Bottom Bypass
J7	MSHUT	DO	Mechanical Shutter Pulse
J8	SUBCK	DO	CCD Substrate Clock (E Shutter)
K8	VL	P	V-Driver Low Supply
K9	VH2	P	V-Driver High Supply 2
L10	RSTB	DI	Reset Bar, Active Low Pulse
K11	SL	DI	3-Wire Serial Load Pulse
J11	SCK	DI	3-Wire Serial Clock
J10	SDI	DI	3-Wire Serial Data Input
J9	V8	VO2	CCD Vertical Transfer Clock
K10	V7	VO2	CCD Vertical Transfer Clock
H9	STROBE	DO	Strobe Pulse
H11	VM2	P	V-Driver Mid Supply 2
H10	V6	VO2	CCD Vertical Transfer Clock
G10	V4	VO2	CCD Vertical Transfer Clock
G11	V2	VO2	CCD Vertical Transfer Clock
G9	VD	DIO	Vertical Sync Pulse (Input in Slave Mode, Output in Master Mode)

Pin No.	Mnemonic	Type[1]	Description[2]
F9	HD	DIO	Horizontal Sync Pulse (Input in Slave Mode, Output in Master Mode)
F10	DVSS	P	Digital Ground
F11	DVDD	P	Digital Logic Power Supply
E9	V5B	VO3	CCD Vertical Transfer Clock
D9	V5A	VO3	CCD Vertical Transfer Clock
E10	DCLK	DO	Data Clock Output
D11	D0	DO	Data Output (LSB)
C10	D1	DO	Data Output
C11	D2	DO	Data Output
B10	D3	DO	Data Output
B11	D4	DO	Data Output
A10	D5	DO	Data Output
A9	D6	DO	Data Output
C9	V3B	VO3	CCD Vertical Transfer Clock
B9	V3A	VO3	CCD Vertical Transfer Clock
B8	V1	VO3	CCD Vertical Transfer Clock
A8	D7	DO	Data Output
B7	D8	DO	Data Output
A7	D9	DO	Data Output
B6	D10	DO	Data Output
A6	D11	DO	Data Output (MSB)
C8	VM1	P	V-Driver Mid Supply 1
C7	VH1	P	V-Driver High Supply 1
C6	VL	P	V-Driver Low Supply
C5	DRVDD	P	Data Output Driver Supply
B5	DRVSS	P	Data Output Driver Ground
A5	VSUB	DO	CCD Substrate Bias
A4	VDVDD	P	V-Driver Logic Supply
B4	VDVSS	P	V-Driver Logic Ground
A1, A2, A3	NC		Not Internally Connected
B1, B2, B3	NC		Not Internally Connected
C1, C2, C3	NC		Not Internally Connected
C4, D1, D2	NC		Not Internally Connected
D3, E2, E3	NC		Not Internally Connected
D10, E11	NC		Not Internally Connected
L1, L11, A11	NC		Not Internally Connected

[1] AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; DIO = Digital Input/Output; P = Power; VO2 = V-Driver Output 2-Level; VO3 = V-Driver Output 3-Level.

[2] See Figure 73 for circuit configuration.

TERMINOLOGY

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus, every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating conditions.

Peak Nonlinearity

Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9925 from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a Level 1 and is 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.

Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship 1 LSB = ADC Full Scale/2^n codes, where *n* is the bit resolution of the ADC. For the AD9925, 1 LSB is 0.488 mV.

Power Supply Rejection (PSR)

The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

EQUIVALENT CIRCUITS

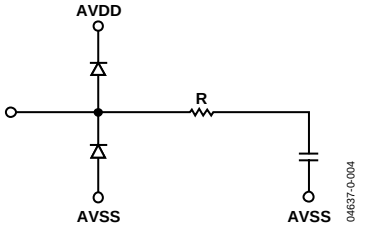


Figure 4. CCDIN

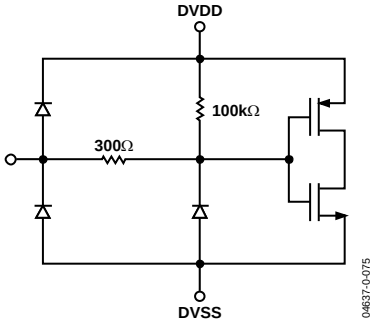


Figure 7. SL and RSTB Inputs

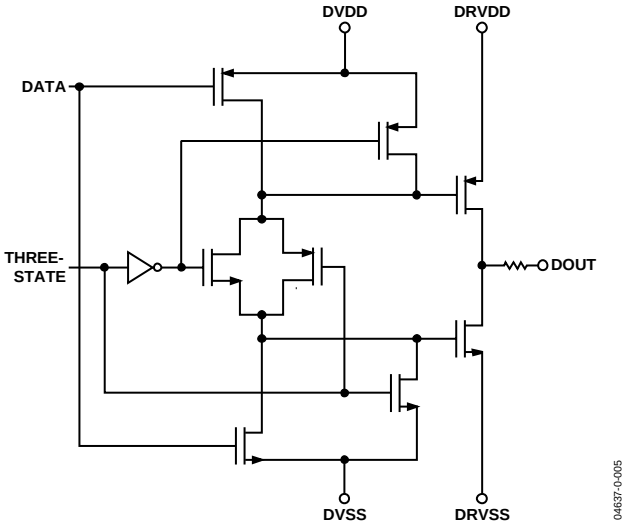


Figure 5. Digital Data Outputs

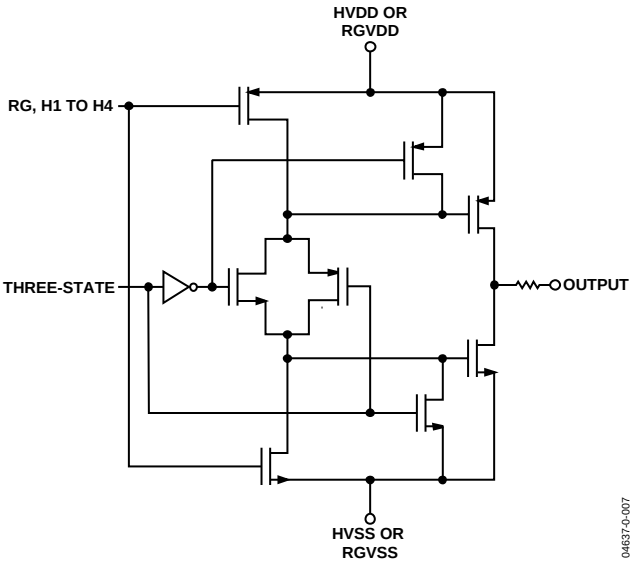


Figure 8. H1 to H4, RG Drivers

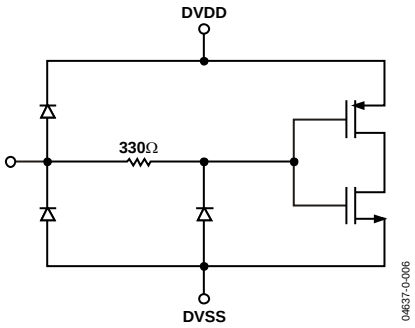


Figure 6. Digital Inputs

TYPICAL PERFORMANCE CHARACTERISTICS

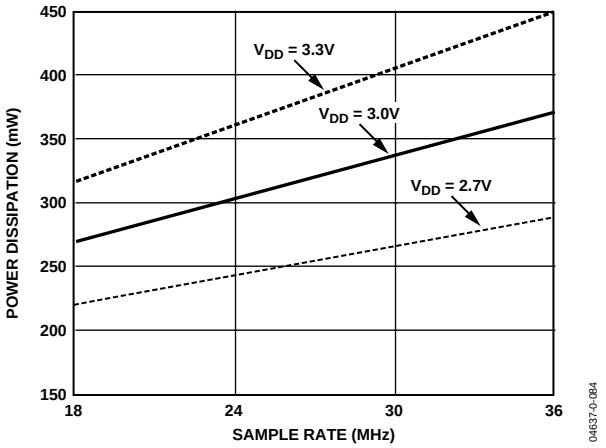


Figure 9. Power vs. Sample Rate

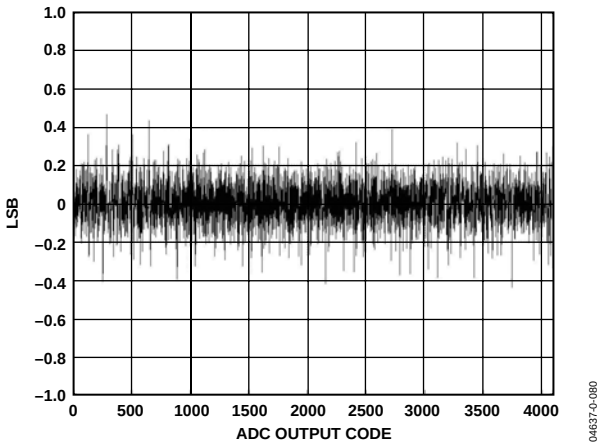


Figure 10. Typical DNL Performance

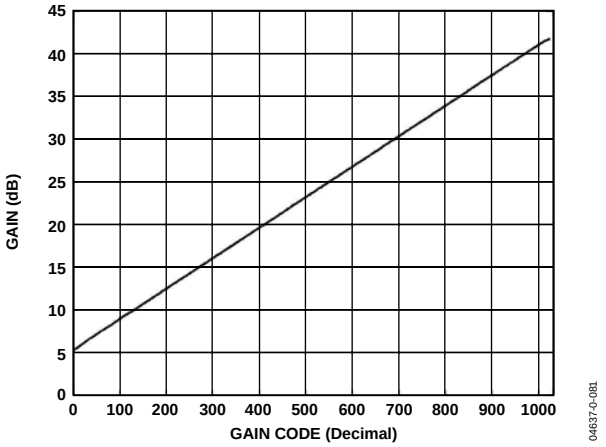


Figure 11. Typical VGA Gain Curve

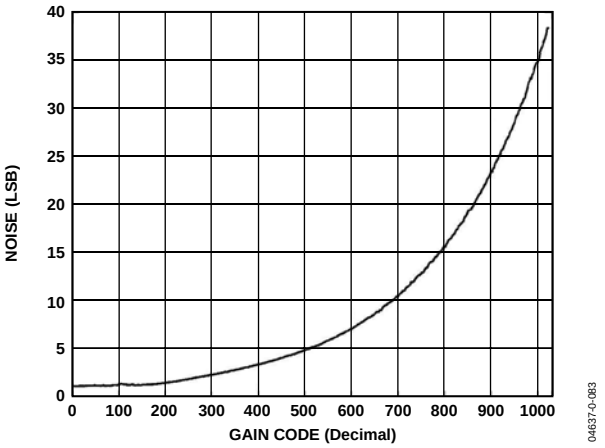


Figure 12. Total Output Noise vs. VGA Gain

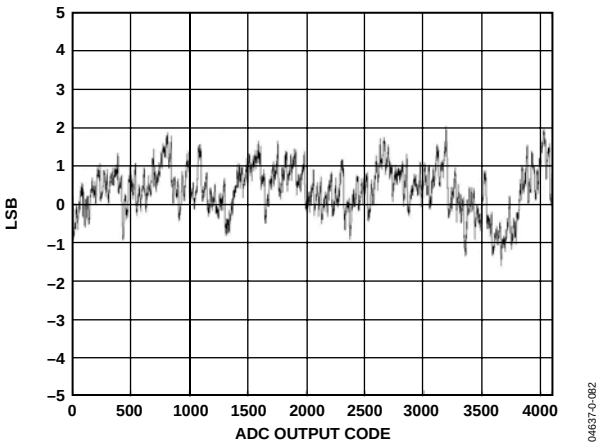


Figure 13. Typical INL Performance

SYSTEM OVERVIEW

Figure 14 shows the typical system block diagram for the AD9925 used in master mode. The CCD output is processed by the AD9925's AFE circuitry, which consists of a CDS, VGA, black level clamp, and ADC. The digitized pixel information is sent to the digital image processor chip, which performs the postprocessing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9925 from the system microprocessor through the 3-wire serial interface. From the system master clock, CLI, provided by the image processor or external crystal, the AD9925 generates the CCD's horizontal and vertical clocks and internal AFE clocks. External synchronization is provided by a SYNC pulse from the microprocessor, which will reset internal counters and resync the VD and HD outputs. The AD9925 also contains an optional reset pin, RSTB, which may be used to perform an asynchronous hardware reset function.

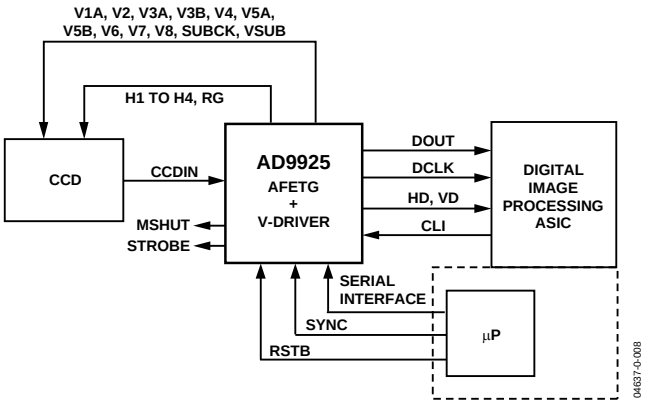


Figure 14. Typical System Block Diagram, Master Mode

Alternatively, the AD9925 may be operated in slave mode, in which the VD and HD are provided externally from the image processor. In this mode, all AD9925 timing will be synchronized with VD and HD.

The H-drivers for H1 to H4 and RG are included in the AD9925, allowing these clocks to be directly connected to the CCD. An H-drive voltage of up to 3.3 V is supported. A high voltage V-driver is also included for the vertical clocks, allowing direct connection to the CCD. The SUBCK and VSUB signals may require external transistors, depending on the CCD used.

The AD9925 also includes programmable MSHUT and STROBE outputs, which may be used to trigger mechanical shutter and strobe (flash) circuitry.

Figure 15 and Figure 16 show the maximum horizontal and vertical counter dimensions for the AD9925. All internal horizontal and vertical clocking is controlled by these counters to specify line and pixel locations. Maximum HD length is 8192 pixels per line, and maximum VD length is 4096 lines per field.

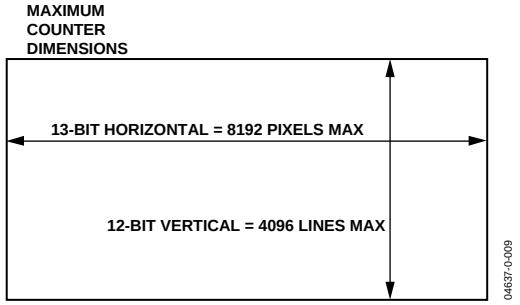


Figure 15. Vertical and Horizontal Counters

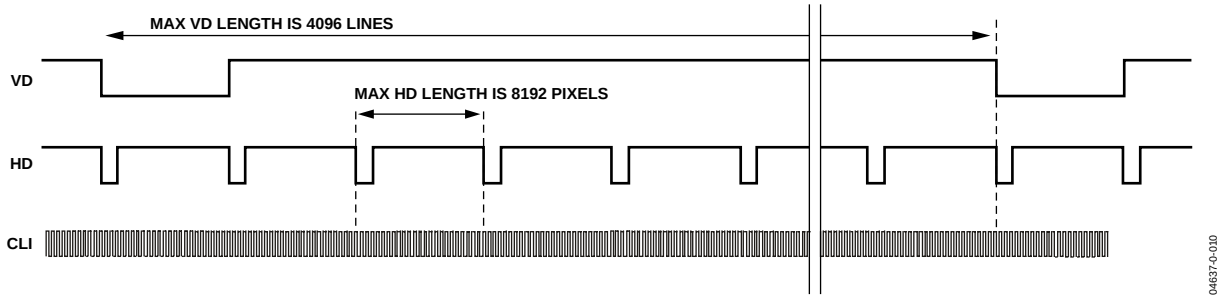


Figure 16. Maximum VD/HD Dimensions

PRECISION TIMING HIGH SPEED TIMING GENERATION

The AD9925 generates high speed timing signals using the flexible *Precision Timing* core. This core is the foundation that generates the timing used for both the CCD and the AFE: the reset gate (RG), horizontal drivers H1 to H4, and the SHP/SHD sample clocks. The unique architecture provides precise control over the horizontal CCD readout and the AFE correlated double sampling, allowing the system designer to optimize image quality.

The high speed timing of the AD9925 operates the same in either master or slave mode configuration. For more information on synchronization and pipeline delays, see the Power-Up and Synchronization section.

Timing Resolution

The *Precision Timing* core uses a 13 master clock input (CLI) as a reference. This clock should be the same as the CCD pixel clock frequency. Figure 17 illustrates how the internal timing core divides the master clock period into 48 steps or edge positions. Using a 20 MHz CLI frequency, the edge resolution of the *Precision Timing* core is 1 ns. If a 1× system clock is not available, it is also possible to use a 2× reference clock by programming the CLIDIVIDE register (Addr x30). The AD9925 will then internally divide the CLI frequency by two.

The AD9925 also includes a master clock output, CLO, which is the inverse of CLI. This output can be used as a crystal driver. A crystal can be placed between the CLI and CLO pins to generate the master clock for the AD9925. For more information on using a crystal, see Figure 72.

High Speed Clock Programmability

Figure 18 shows how the high speed clocks RG, H1 to H4, SHP, and SHD are generated. The RG pulse has programmable rising and falling edges and may be inverted using the polarity control. The horizontal clocks, H1 and H3, have programmable rising and falling edges and polarity control. The H2 and H4 clocks are always inverses of H1 and H3, respectively. Table 8 summarizes the high speed timing registers and their parameters. Figure 19 shows the typical 2-phase H-clock arrangement in which H3 and H4 are programmed for the same edge location as H1 and H2.

The edge location registers are 6 bits wide, but there are only 48 valid edge locations available. Therefore, the register values are mapped into four quadrants, with each quadrant containing 12 edge locations. Table 9 shows the correct register values for the corresponding edge locations.

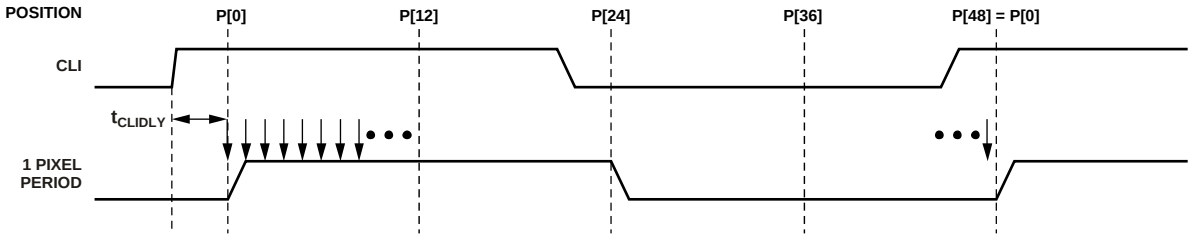


Figure 17. High Speed Clock Resolution from CLI Master Clock Input

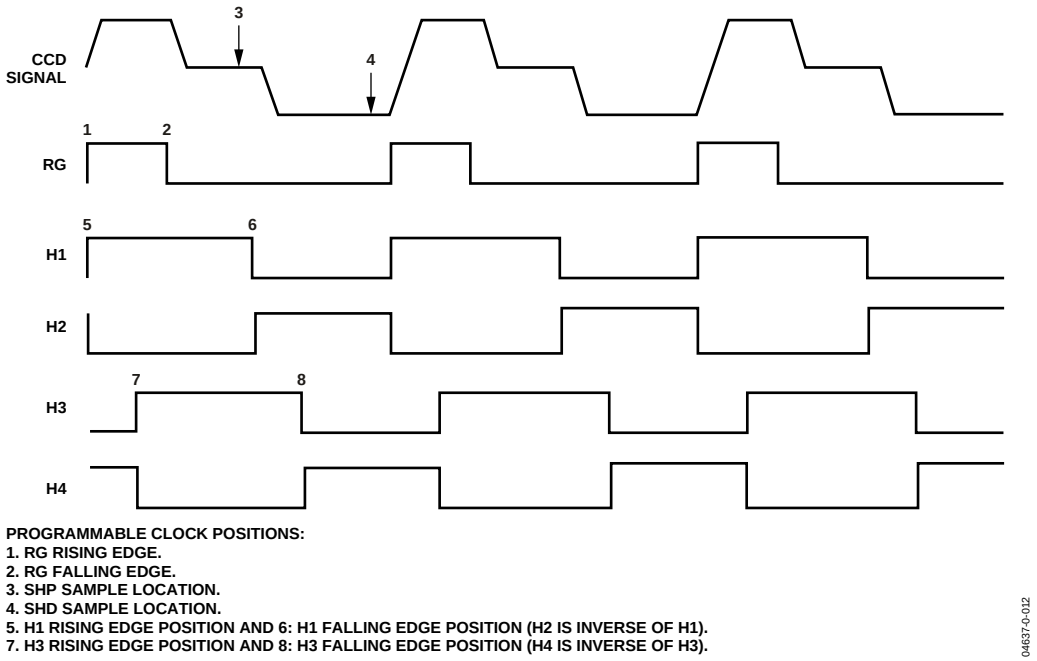


Figure 18. High Speed Clock Programmable Locations

Figure 20 shows the default timing locations for all of the high speed clock signals.

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9925 features on-chip output drivers for the RG and H1 to H4 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver and RG current can be adjusted for optimum rise/fall time with a particular load by using the DRVCONTROL register (Addr x35). The 3-bit drive setting for each output is adjustable in 4.1 mA increments, with the minimum setting of 0 equal to OFF or three-state and the maximum setting of 7 equal to 30.1 mA.

As shown in Figure 18, Figure 19, and Figure 20, the H2 and H4 outputs are inverses of H1 and H3, respectively. The H1/H2 crossover voltage is approximately 50% of the output swing. The crossover voltage is not programmable.

Digital Data Outputs

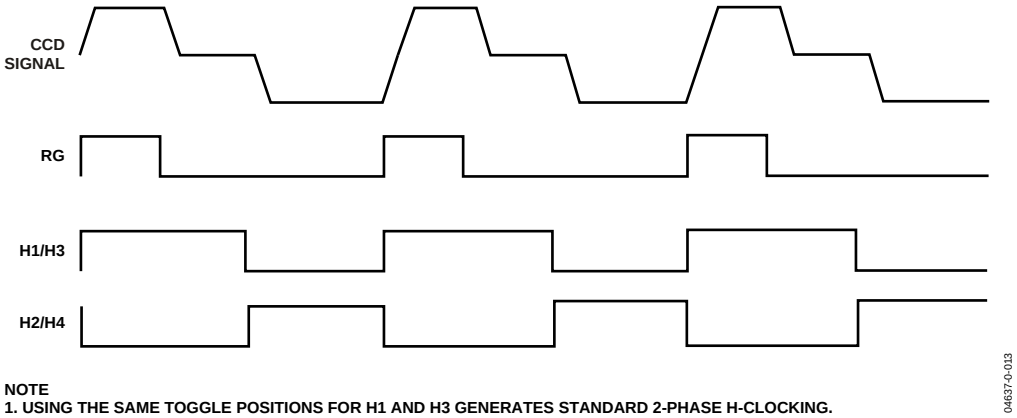
The AD9925 data output and DCLK phase are programmable using the DOUTPHASE register (Addr x37, Bits [5:0]). Any edge from 0 to 47 may be programmed, as shown in Figure 21. Normally, the DOUT and DCLK signals will track in phase, based on the DOUTPHASE register contents. The DCLK output phase can also be held fixed with respect to the data outputs by changing the DCLKMODE register high (Addr x37, Bit [6]). In this mode, the DCLK output will remain at a fixed phase equal to CLO (the inverse of CLI), while the data output phase is still programmable.

There is a fixed output delay from the DCLK rising edge to the DOUT transition, called t_{OD}. This delay can be programmed to four values between 0 ns and 12 ns by using the DOUTDELAY register (Addr x37, Bits [8:7]). The default value is 8 ns.

The pipeline delay through the AD9925 is shown in Figure 22. After the CCD input is sampled by SHD, there is an 11 cycle delay until the data is available.

Table 8. Timing Core Register Parameters for H1, H3, RG, SHP/SHD

Parameter	Length	Range	Description
Polarity	1 b	High/Low	Polarity Control for H1, H3, and RG (0 = No Inversion, 1 = Inversion)
Positive Edge	6 b	0 to 47 Edge Location	Positive Edge Location for H1, H3, and RG
Negative Edge	6 b	0 to 47 Edge Location	Negative Edge Location for H1, H3, and RG
Sampling Location	6 b	0 to 47 Edge Location	Sampling Location for Internal SHP and SHD Signals
Drive Strength	3 b	0 to 47 Current Steps	Drive Current for H1 to H4 and RG Outputs (4.1 mA per Step)

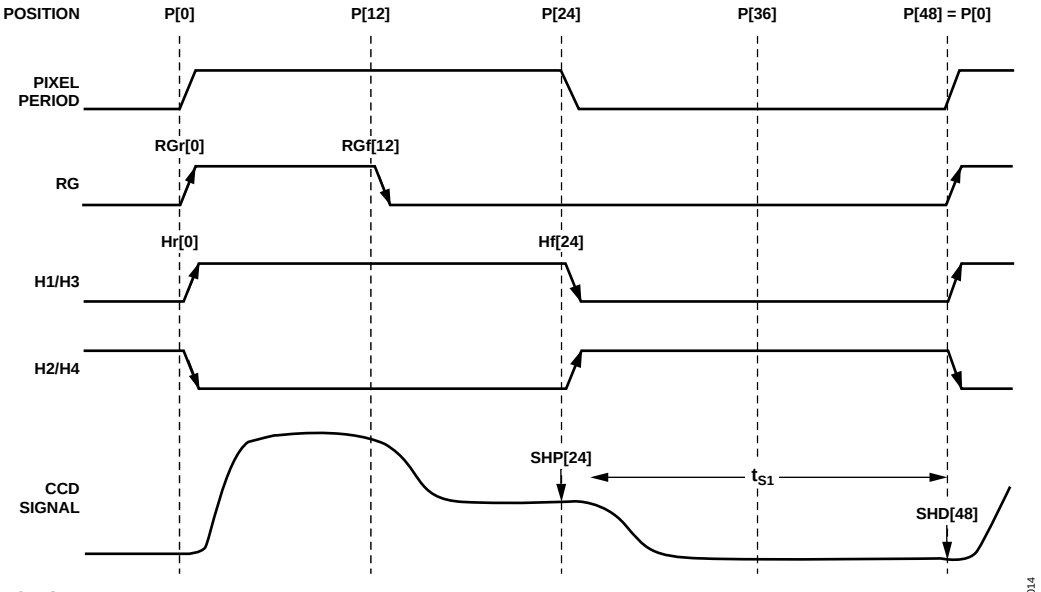


NOTE
1. USING THE SAME TOGGLE POSITIONS FOR H1 AND H3 GENERATES STANDARD 2-PHASE H-CLOCKING.

Figure 19. 2-Phase H-Clock Operation

Table 9. *Precision Timing* Edge Locations

Quadrant	Edge Location (Dec)	Register Value (Dec)	Register Value (Bin)
I	0 to 11	0 to 11	000000 to 001011
II	12 to 23	16 to 27	010000 to 011011
III	24 to 35	32 to 43	100000 to 101011
IV	36 to 47	48 to 59	110000 to 111011



NOTES
1. ALL SIGNAL EDGES ARE FULLY PROGRAMMABLE TO ANY OF THE 48 POSITIONS WITHIN ONE PIXEL PERIOD.
2. DEFAULT POSITIONS FOR EACH SIGNAL ARE SHOWN.

Figure 20. High Speed Timing Default Locations

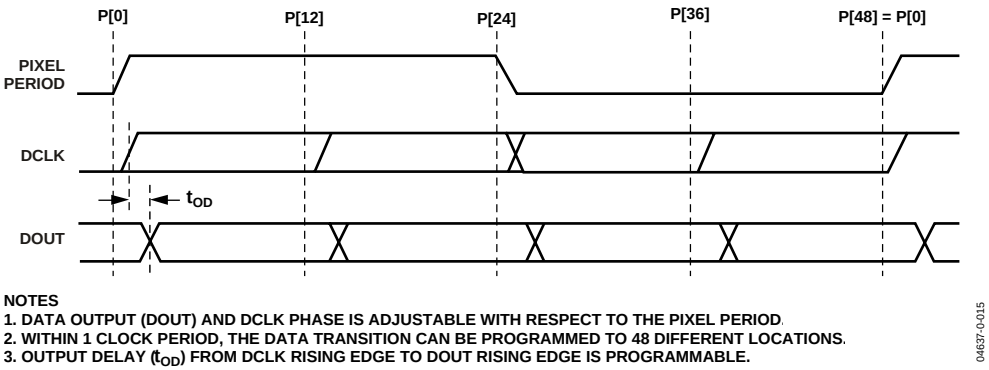


Figure 21. Digital Output Phase Adjustment

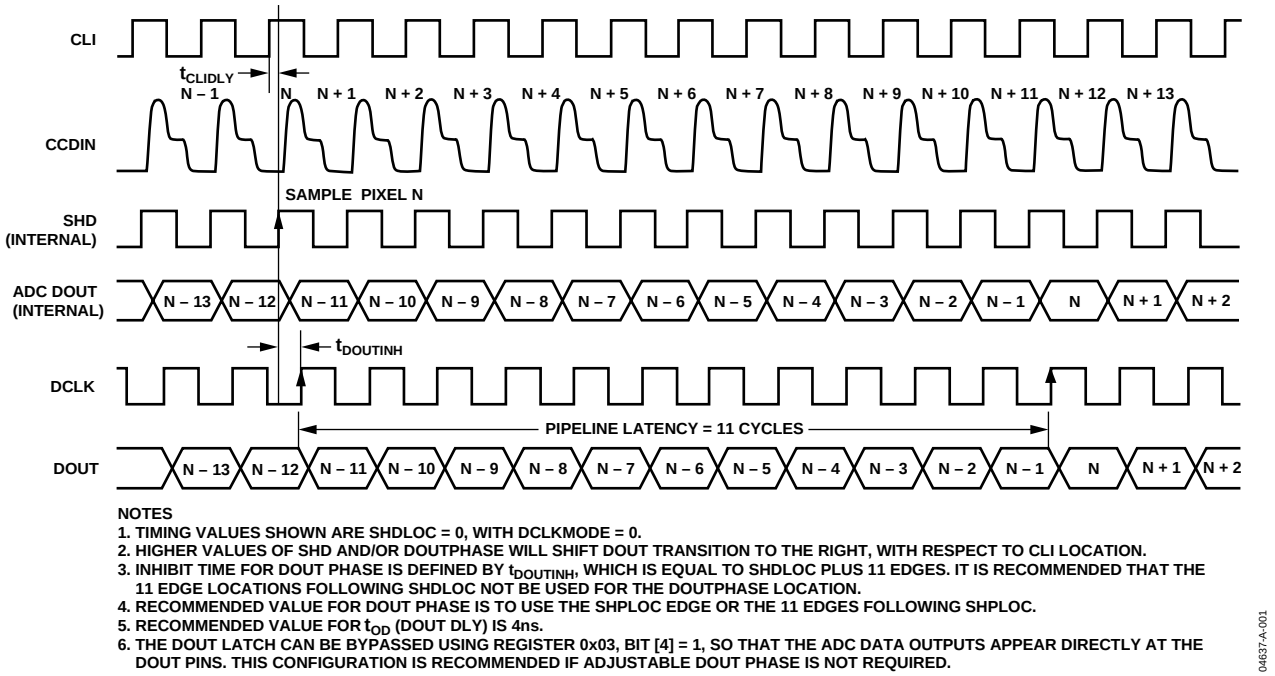


Figure 22. Digital Data Output Pipeline Delay

HORIZONTAL CLAMPING AND BLANKING

The AD9925's horizontal clamping and blanking pulses are fully programmable to suit a variety of applications. Individual control is provided for CLPOB, PBLK, and HBLK during the different regions of each field. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout, which accommodates the different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 23. These two signals are independently programmed using the registers in Table 10. SPOL is the start polarity for the signal, and TOG1 and TOG2 are the first and second toggle positions of the pulse. Both signals are active low and should be programmed accordingly.

A separate pattern for CLPOB and PBLK may be programmed for every 10 vertical sequences. As described in the Vertical Timing Generation section, up to 10 separate vertical sequences can be created, each containing a unique pulse pattern for CLPOB and PBLK. Figure 37 shows how the sequence change positions divide the readout field into different regions. A different vertical sequence can be assigned to each region, allowing the CLPOB and PBLK signals to be changed accordingly with each change in the vertical timing.

CLPOB Masking Area

Additionally, the AD9925 allows the CLPOB signal to be disabled during certain lines in the field without changing any of the existing CLPOB pattern settings. There are two ways to use CLPOB masking. First, the six CLPOBMASK registers can be used

to specify six individual lines within the field. These lines will not contain an active CLPOB pulse. CLPMASKTYPE is set low for this mode of operation.

Second, the CLPMASK registers can be used to specify blocks of adjacent lines. The CLPMASK start and end line values are programmed to specify the starting and ending lines in the field, where the CLPOB patterns will be ignored. There are three sets of start and end values, allowing up to three CLPOB masking areas to be created. CLPMASKTYPE is set high for this mode of operation.

The CLPOB masking registers are not specific to a certain vertical sequence; they are always active for any existing field of timing. To disable the CLPOB masking feature, these registers should be set to the maximum value of 0xFFF (default value).

Individual HBLK Patterns

The HBLK programmable timing shown in Figure 24 is similar to CLPOB and PBLK, but there is no start polarity control. Only the toggle positions are used to designate the start and the stop positions of the blanking period. Additionally, there is a polarity control HBLKMASK that designates the polarity of the horizontal clock signals H1 to H4 during the blanking period. Setting HBLKMASK high will set H1 = H3 = Low and H2 = H4 = High during the blanking, as shown in Figure 25. As with the CLPOB and PBLK signals, HBLK registers are available in each vertical sequence, which allow different blanking signals to be used with different vertical timing sequences.

One additional feature is the ability to enable the H3/H4 signals to remain active during HBLK. To do this, set register Bit D6 in Addr 0xE7 equal to 1. This feature is useful if the H3 output is used to drive the HL (last horizontal gate) input of the CCD.

Table 10. CLPOB and PBLK Pattern Registers

Register	Length	Range	Description
SPOL	1 b	High/Low	Starting Polarity of CLPOB/PBLK for Vertical Sequence 0 to 9.
TOG1	12 b	0 to 4095 Pixel Location	First Toggle Position within Line for Vertical Sequence 0 to 9.
TOG2	12 b	0 to 4095 Pixel Location	Second Toggle Position within Line for Vertical Sequence 0 to 9.
CLPOBMASK	12 b	0 to 4095 Line Location	CLPOBMASK0 through CLPOBMASK5 specify six individual lines in the field for the CLPOB pulse to be temporarily disabled. These registers can also be used to specify three ranges of adjacent lines, rather than six individual lines.
CLPMASKTYPE	1 b	High/Low	When set low (default), the CLPOBMASK registers select individual lines in the field to disable the CLPOB pulse. When set high, the range masking is enabled, allowing up to three blocks of adjacent lines to have the CLPOB signal masked. CLPOBMASK0 and CLPOBMASK1 are the start/end of the first block of lines, CLPOBMASK2 and CLPOBMASK3 are the start/end of the second block, and CLPOBMASK4 and CLPOBMASK5 are the start/end of the third block.

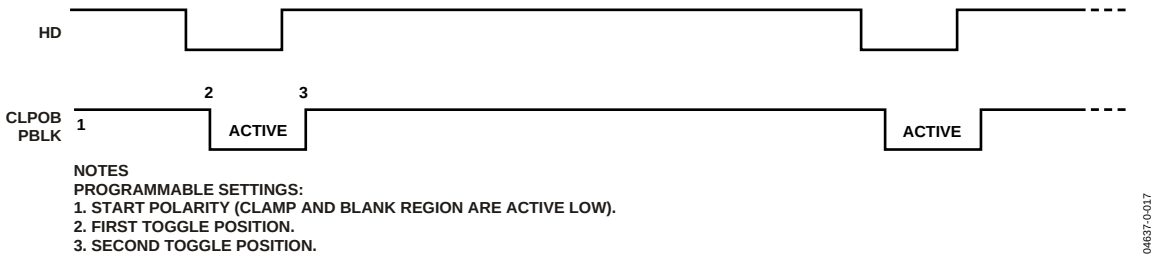


Figure 23. Clamp and Preblank Pulse Placement

Table 11. HBLK Pattern Registers

Register	Length	Range	Description
HBLKMASK	1 b	High/Low	Masking Polarity for H1/H3 (0 = H1/H3 Low, 1 = H1/H3 High).
H3HBLKOFF	1 b	High/Low	Addr 0xE7, Bit [6]. Set = 1 to keep H3/H4 active during HBLK pulse. Normal set to 0.
HBLKALT	2 b	0 to 3 Alternation Mode	Enables Odd/Even Alternation of HBLK Toggle Positions. 0 = Disable Alternation. 1 = TOG1 to TOG2 Odd, TOG3 to TOG6 Even. 2 = 3 = TOG1to TOG2 Even, TOG3 to TOG6 Odd.
HBLKTOG1	12 b	0 to 4095 Pixel Location	First Toggle Position within Line for Each Vertical Sequence 0 to 9.
HBLKTOG2	12 b	0 to 4095 Pixel Location	Second Toggle Position within Line for Each Vertical Sequence 0 to 9.
HBLKTOG3	12 b	0 to 4095 Pixel Location	Third Toggle Position within Line for Each Vertical Sequence 0 to 9.
HBLKTOG4	12 b	0 to 4095 Pixel Location	Fourth Toggle Position within Line for Each Vertical Sequence 0 to 9.
HBLKTOG5	12 b	0 to 4095 Pixel Location	Fifth Toggle Position within Line for Each Vertical Sequence 0 to 9.
HBLKTOG6	12 b	0 to 4095 Pixel Location	Sixth Toggle Position within Line for Each Vertical Sequence 0 to 9.

Generating Special HBLK Patterns

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions may be used to generate special HBLK patterns, as shown in Figure 26. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns can be created.

Generating HBLK Line Alternation

One further feature of the AD9925 is the ability to alternate different HBLK toggle positions on odd and even lines. This may be used in conjunction with vertical pattern odd/even alternation or on its own. When a 1 is written to the HBLKALT register, TOG1 and TOG2 are used on odd lines, while TOG3 to TOG6 are used on even lines. Writing a 2 to the HBLKALT register gives the opposite result: TOG1 and TOG2 are used on even lines, while TOG3 to TOG6 are used on odd lines. See the Vertical Timing Generation section for more information.

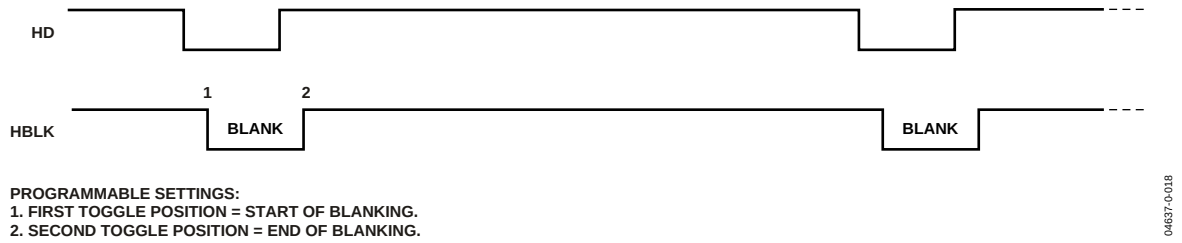


Figure 24. Horizontal Blanking (HBLK) Pulse Placement

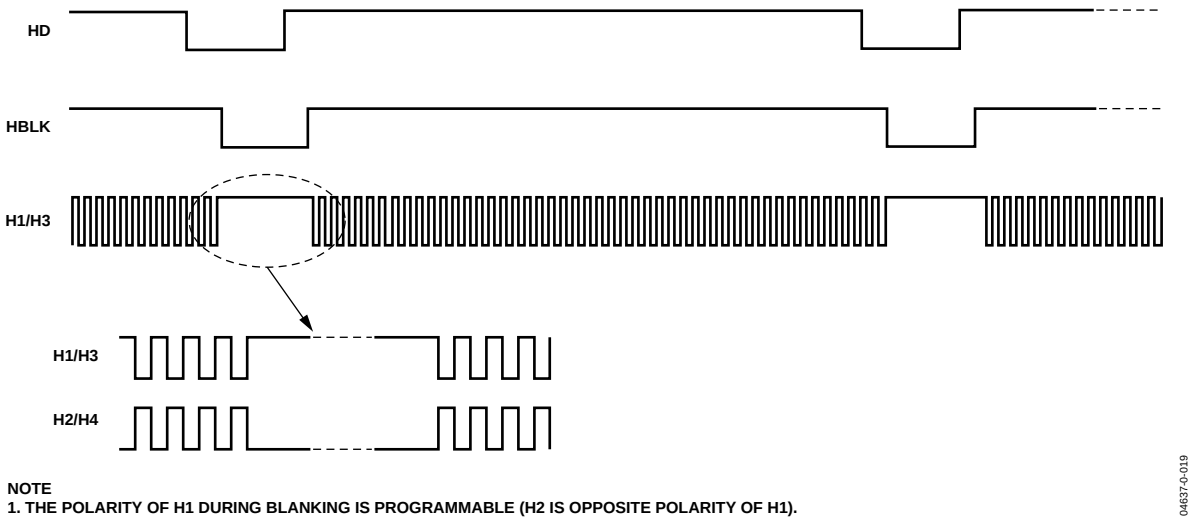


Figure 25. HBLK Masking Control

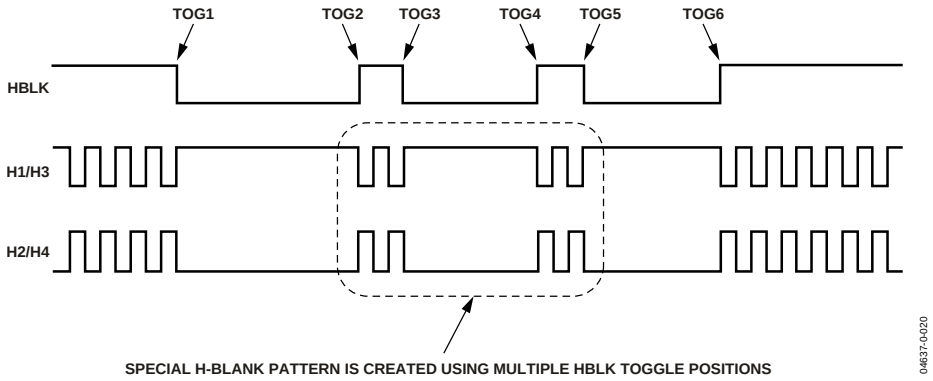


Figure 26. Generating Special HBLK Patterns

Increasing H-Clock Width during HBLK

The AD9925 will also allow the H1 to H4 pulse width to be increased during the HBLK interval. The H-clock pulse width can increase by reducing the H-clock frequency (see Figure 27). The HBLKWIDTH register, at Bank 1 Address 0x38, is a 3-bit register that allows the H-clock frequency to be reduced by 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, or 1/14. The reduced frequency will only occur for H1 to H4 pulses that are located within the HBLK area.

Table 12. HBLK Width Register

Register	Length	Range	Description
HBLKWIDTH	3 b	1 to 1/14	Controls H1 to H4 width during HBLK as a fraction of pixel rate 0: same frequency as pixel rate 1: 1/2 pixel frequency, i.e., doubles the H1 to H4 pulse width 2: 1/4 pixel frequency 3: 1/6 pixel frequency 4: 1/8 pixel frequency 5: 1/10 pixel frequency 6: 1/12 pixel frequency 7: 1/14 pixel frequency

HORIZONTAL TIMING SEQUENCE EXAMPLE

Figure 28 shows an example CCD layout. The horizontal register contains 28 dummy pixels, which will occur on each line clocked from the CCD. In the vertical direction, there are 10 optical black (OB) lines at the front of the readout and 2 at the back of the readout. The horizontal direction has 4 OB pixels in the front and 48 in the back.

Figure 29 shows the basic sequence layout to be used during the effective pixel readout. The 48 OB pixels at the end of each line are used for the CLPOB signals. PBLK is optional and is often used to blank the digital outputs during the noneffective CCD pixels. HBLK is used during the vertical shift interval. The HBLK, CLPOB, and PBLK parameters are programmed in the vertical sequence registers.

More elaborate clamping schemes may be used, such as adding in a separate sequence to clamp during the entire shield OB lines. This requires configuring a separate vertical sequence for reading out the OB lines.

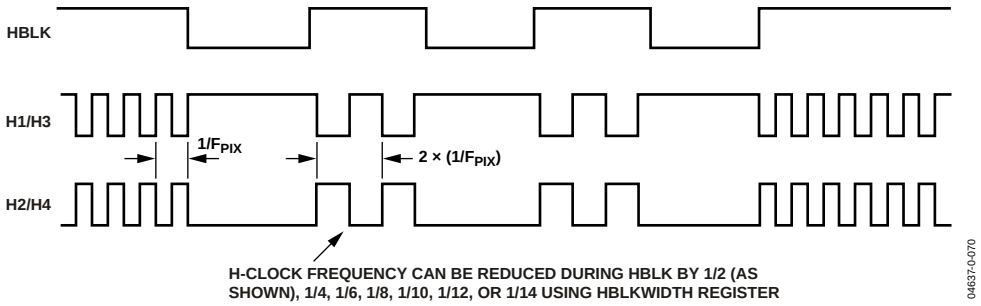


Figure 27. Generating Wide H-Clock Pulses during HBLK Interval

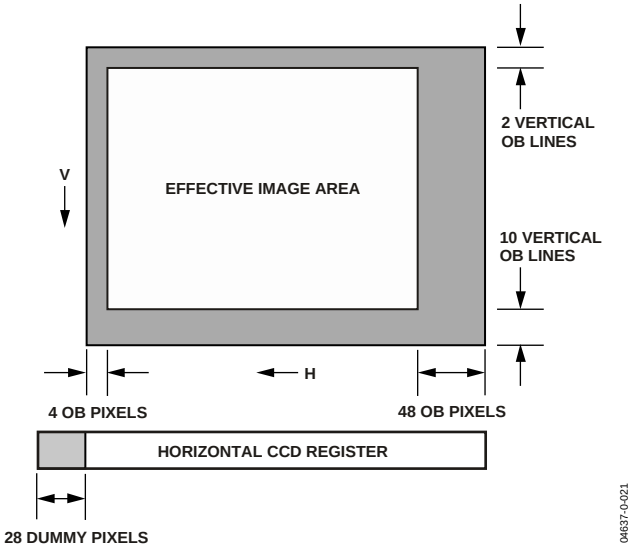


Figure 28. Example CCD Configuration

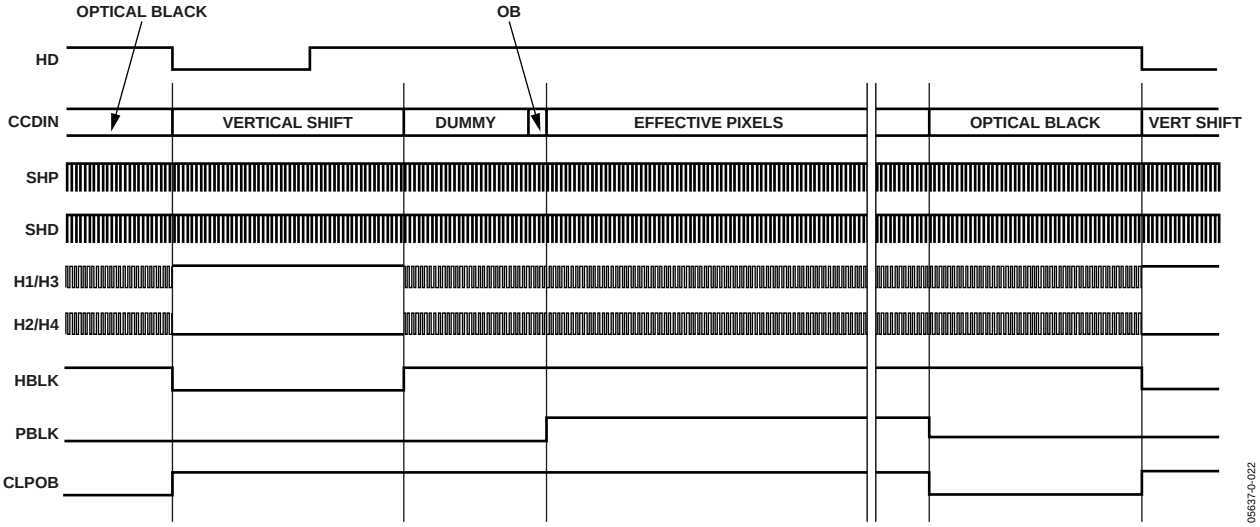


Figure 29. Horizontal Sequence Example

VERTICAL TIMING GENERATION

The AD9925 provides a very flexible solution for generating vertical CCD timing and can support multiple CCDs and different system architectures. The vertical transfer clocks XV1 to XV8 are used to shift each line of pixels into the horizontal output register of the CCD. The AD9925 allows these outputs to be individually programmed into various readout configurations, using a 4-step process.

Figure 30 shows an overview of how the vertical timing is generated in four steps. First, the individual pulse patterns for XV1 to XV8 are created by using the vertical pattern group registers. Second, the vertical pattern groups are used to build the sequences, where additional information is added. Third, the readout for an entire field is constructed by dividing the field into different regions and then assigning a sequence to each region. Each field can contain up to seven different regions to accommodate the different steps of the readout, such as high speed line shifts and unique vertical line transfers. Up to six different fields may be created. Finally, the MODE register allows the different fields to be combined into any order for various readout configurations.

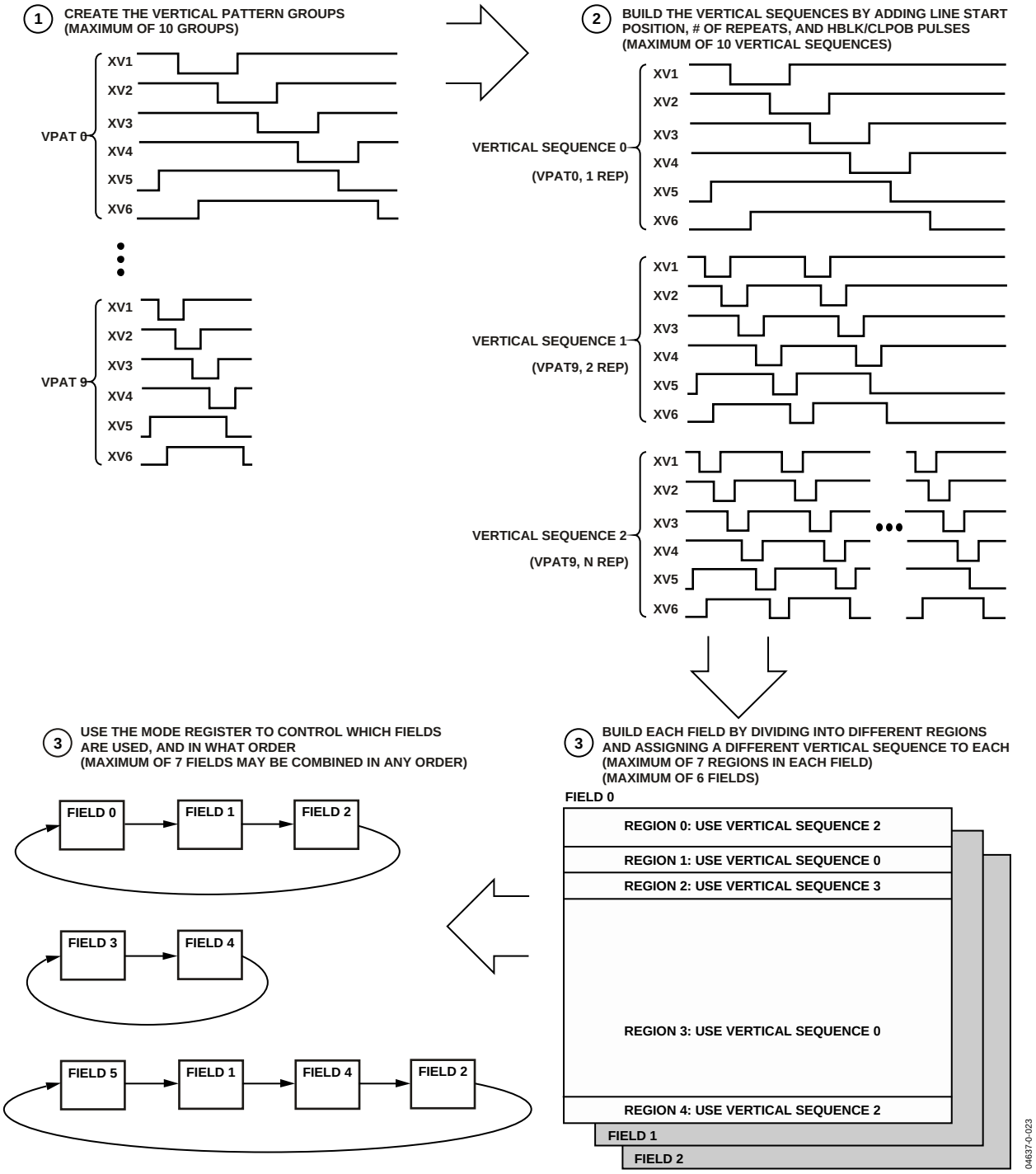


Figure 30. Summary of Vertical Timing Generation

Vertical Pattern Groups (VPAT)

The vertical pattern groups define the individual pulse patterns for each XV1 to XV6 output signal. Table 13 summarizes the registers available for generating each of the 10 vertical pattern groups. The start polarity (VPOL) determines the starting polarity of the vertical sequence and can be programmed high or low for each XV1 to XV6 output. The first, second, and third toggle positions (XVTOG1, XVTOG2, and XVTOG3) are the pixel locations within the line where the pulse transitions. A fourth toggle position (XVTOG4) is also available for vertical pattern groups 8 and 9. All toggle positions are 12-bit values, allowing their placement anywhere in the horizontal line. A separate register, VPATSTART, specifies the start position of the vertical pattern groups within the line (see the Vertical Sequences (VSEQ) section). The VPATLEN register designates the total length of the vertical pattern group, which determines the number of pixels between each of the pattern repetitions when repetitions are used (see the Vertical Sequences (VSEQ) section).

Additional VPAT groups are provided in Register Bank 3 for the XV7 and XV8 outputs. This allows the AD9925 to remain backward-compatible with the AD9995 register settings while still providing additional flexibility with XV7 and XV8 for new CCDs.

Table 13. Vertical Pattern Group Registers

Register	Length	Range	Description
XVPOL	1 b	High/Low	Starting Polarity of Each XV Output
XVTOG1	12 b	0 to 4096 Pixel Location	First Toggle Position within Line for Each XV Output
XVTOG2	12 b	0 to 4096 Pixel Location	Second Toggle Position within Line for Each XV Output
XVTOG3	12 b	0 to 4096 Pixel Location	Third Toggle Position within Line for Each XV Output
XVTOG4	12 b	0 to 4096 Pixel Location	Fourth Toggle Position, Only Available in Vertical Pattern Groups 8 and 9 and Also in XV7 and XV8 Vertical Pattern Groups
VPATLEN	12 b	0 to 4096 Pixels	Total Length of Each Vertical Pattern Group
FREEZE1	12 b	0 to 4096 Pixel Location	Holds the XV Outputs at Their Current Levels (Static DC)
RESUME1	12 b	0 to 4096 Pixel Location	Resumes Operation of the XV Outputs to Finish Their Pattern
FREEZE2	12 b	0 to 4096 Pixel Location	Holds the XV Outputs at Their Current Levels (Static DC)
RESUME2	12 b	0 to 4096 Pixel Location	Resumes Operation of the XV Outputs to Finish Their Pattern

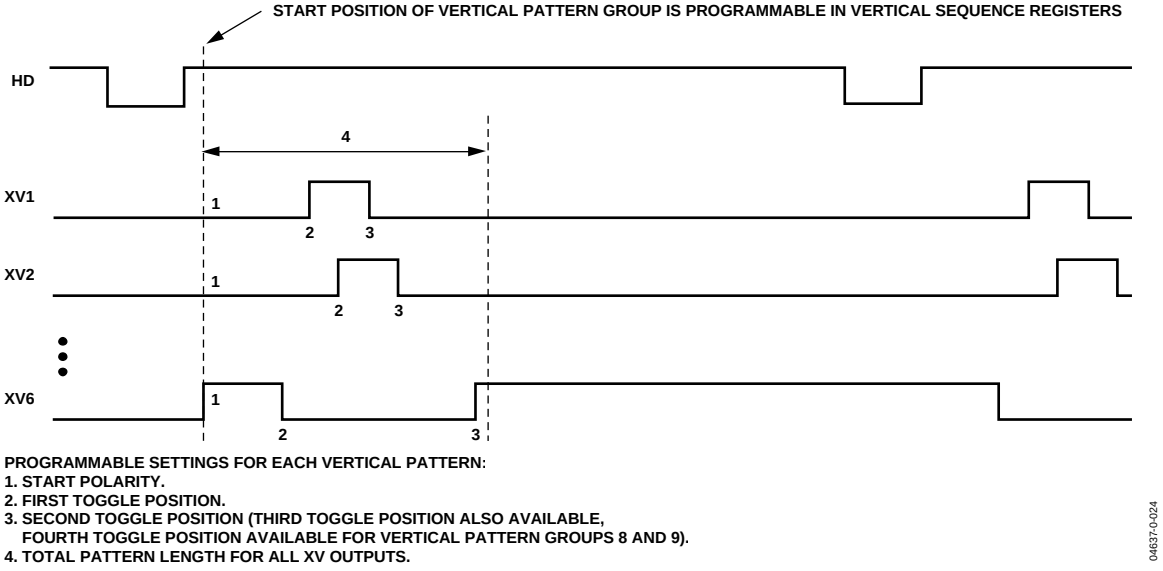


Figure 31. Vertical Pattern Group Programmability

Masking Using FREEZE/RESUME Registers

As shown in Figure 33, the FREEZE/RESUME registers are used to temporarily mask the XV outputs. The pixel locations to begin the masking (FREEZE) and end the masking (RESUME) create an area in which the vertical toggle positions are ignored. At the pixel location specified in the FREEZE register, the XV outputs will be held static at their current dc state, high or low. The XV outputs are held until the pixel location specified by the RESUME register is reached, at which point the signals will continue with any remaining toggle positions. Two sets of FREEZE/RESUME registers are provided, allowing the vertical outputs to be interrupted twice in the same line. The FREEZE and RESUME positions are programmed in the vertical pattern group registers, but are enabled separately using the VMASK registers. The VMASK registers are described in the Vertical Sequences (VSEQ) section.

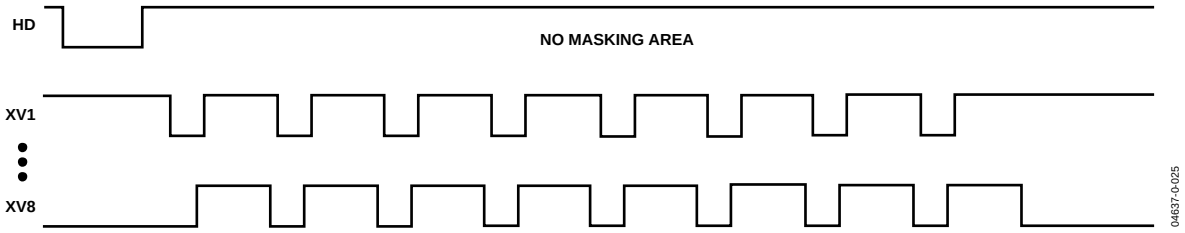


Figure 32. No Vertical Masking

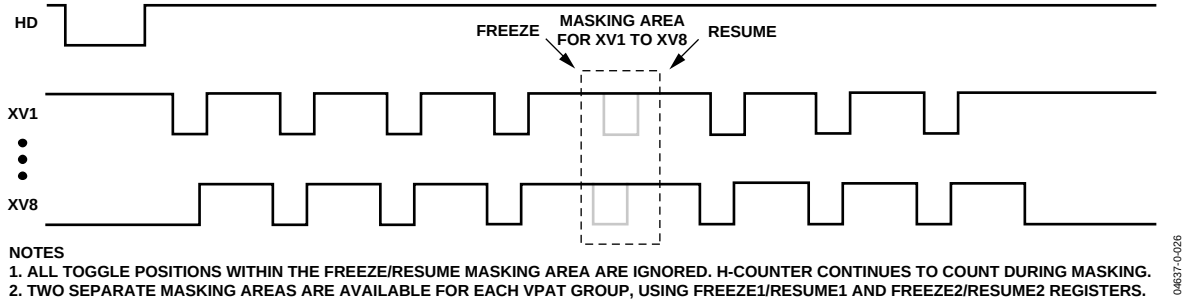


Figure 33. Vertical Masking Using the FREEZE/RESUME Registers

Hold Area Using FREEZE/RESUME Registers

The FREEZE/RESUME registers can also be used to create a hold area, in which the XV outputs are temporarily held and then later continued starting at the point where they were held. As shown in Figure 34 and Figure 35, this is different than the VMASK, because the XV outputs continue from where they stopped rather than continuing from where they would have been. The hold area temporarily stops the pixel counter for the XV outputs, while the v-masking allows the counter to continue during the masking area.

XV7 and XV8 may or may not use the hold area, as shown in Figure 34 and Figure 35. The hold operation is controlled in the Bank 3 vertical sequence registers, described in the Vertical Sequences (VSEQ) section.

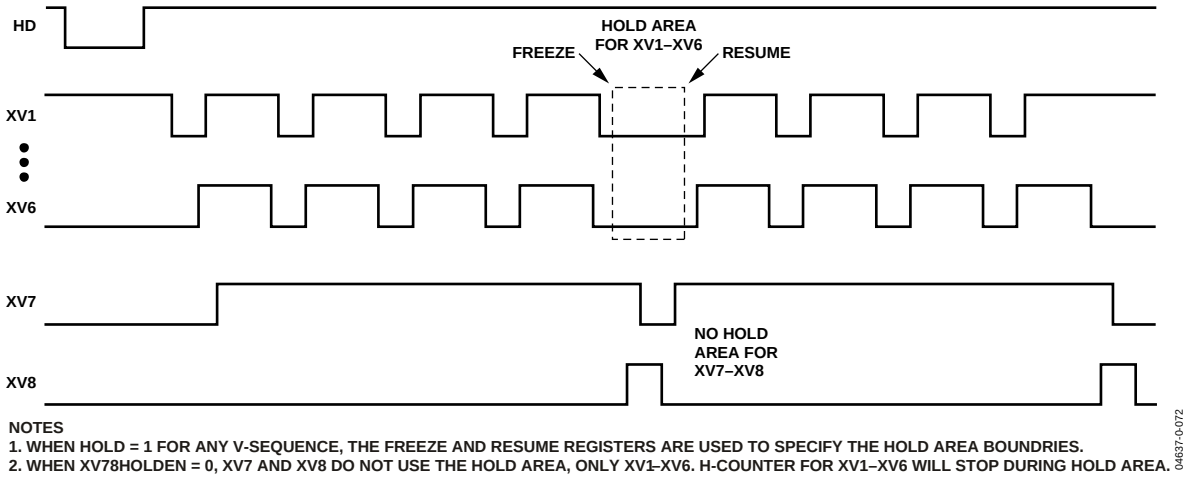


Figure 34. Vertical Hold Area Using the FREEZE/RESUME Registers

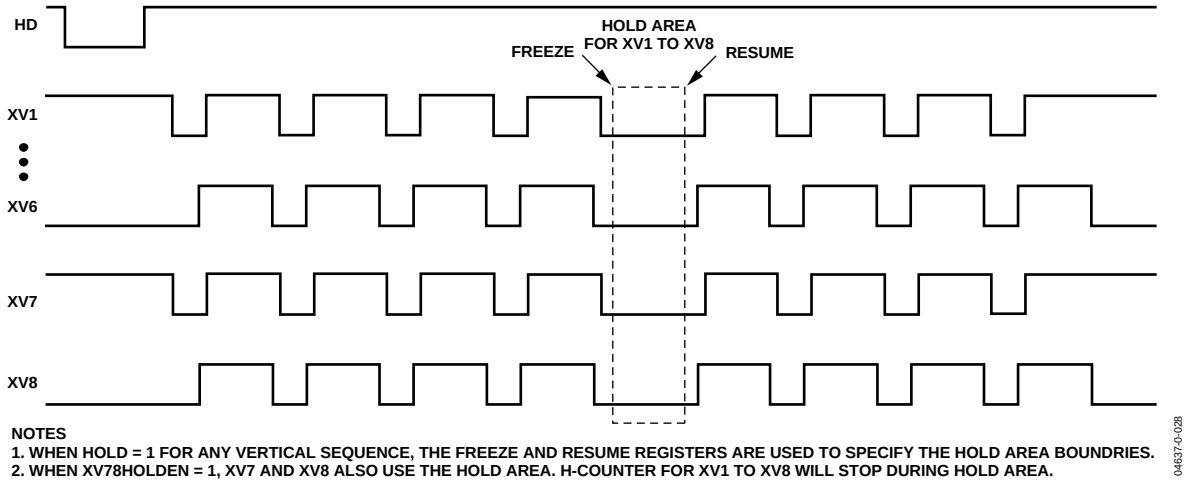


Figure 35. Apply Hold Area to XV7 and XV8

Vertical Sequences (VSEQ)

The vertical sequences are created by selecting one of the 10 vertical pattern groups and adding repeats, the start position, and horizontal clamping and blanking information. Up to 10 vertical sequences may be programmed, each using the registers shown in Table 14. Figure 36 shows how the different registers are used to generate each vertical sequence.

The VPATSEL register selects which vertical pattern group will be used in a given vertical sequence. The basic vertical pattern group can have repetitions added for high speed line shifts or line binning by using the VPATREPO and VPATREPE registers. Generally, the same number of repetitions is programmed into both registers, but if a different number of repetitions is required on odd and even lines, separate values may be used for each register (see the Generating Line Alternation for Vertical Sequence and HBLK section). The VPATSTART register specifies the pixel location where the vertical pattern group will start.

The VMASK register is used in conjunction with the FREEZE/RESUME registers to enable optional masking of the vertical outputs. Either or both of the FREEZE1/RESUME1 and FREEZE2/RESUME2 registers can be enabled using the VMASK register.

The line length (in pixels) is programmable using the HDLEN registers. Each vertical sequence can have a different line length to accommodate the various image readout techniques. The maximum number of pixels per line is 8192. Note that the 13th bit (MSB) of the line length is located in a separate register. Also note that the last line of the field is separately programmable using the HDLAST register, located in the field register section.

Additional vertical sequences are provided in Register Bank 3 for the XV7 and XV8 outputs. This allows the AD9925 to remain backward-compatible with the AD9995 register settings while still providing additional flexibility with XV7 and XV8 for new CCDs.

As described in the Hold Area Using FREEZE/RESUME Registers section, the hold registers in Bank 3 are used to specify a hold area instead of vertical masking. The FREEZE/RESUME registers are used to define the hold area. The XV78HOLDEN registers are used to specify whether XV7 and XV8 will use the hold area or not.

Table 14. Vertical Sequence Registers (See Table 10 and Table 11 for the HBLK, CLPOB, and PBLK registers)

Register	Length	Range	Description
VPATSEL	4 b	0 to 9 Vertical Pattern Group No.	Selected Vertical Pattern Group for Each Vertical Sequence.
VMASK	2 b	0 to 3 Mask Mode	Enables the Masking of V1 to V6 Outputs at the Locations Specified by the FREEZE/RESUME Registers. 0 = No Mask. 1 = Enable Freeze1/Resume1. 2 = Enable Freeze2/Resume2. 3 = Enable Both 1 and 2.
VPATREPO	12 b	0 to 4095 Number of Repeats	Number of Repetitions for the Vertical Pattern Group for Odd Lines. If no odd/even alternation is required, set equal to VPATREPE.
VPATREPE	12 b	0 to 4095 Number of Repeats	Number of Repetitions for the Vertical Pattern Group for Even Lines. If no odd/even alternation is required, set equal to VPATREPO.
VPATSTART	12 b	0 to 4095 Pixel Location	Start Position for the Selected Vertical Pattern Group.
HDLEN	13 b	0 to 8191 Number of Pixels	HD Line Length for Lines in Each Vertical Sequence. Note that 13th bit (MSB) of the line length is located in a separate register to maintain compatibility with AD9995.
HOLD[1]	1 b	High/Low	Enable Hold Area Instead of Vertical Masking, Using FREEZE/RESUME Registers.
XV78HOLDEN[1]	1 b	High/Low	Enable XV7 and XV8 to Use Hold Area. 0 = Disable. 1 = Enable.

[1]Located in Bank 3, vertical sequence registers for XV7 and XV8.

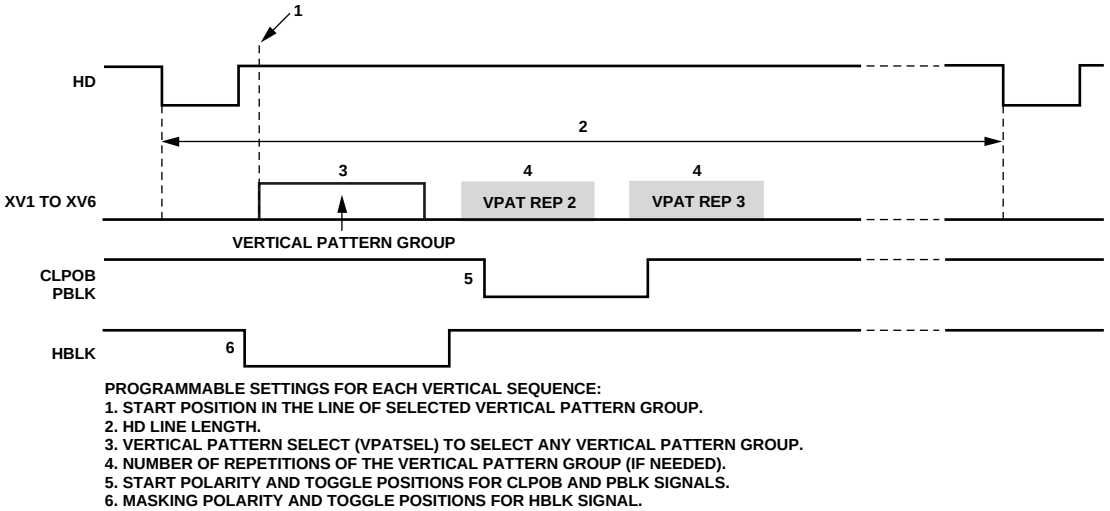


Figure 36. Vertical Sequence Programmability

Complete Field: Combining Vertical Sequences

After the vertical sequences have been created, they are combined to create different readout fields. A field consists of up to seven different regions, and within each region, a different vertical sequence can be selected. Figure 37 shows how the sequence change positions (SCP) designate the line boundary for each region, and how the VSEQSEL registers select which vertical sequence is used during each region. Registers to control the XSG outputs are also included in the field registers.

Table 15 summarizes the registers used to create the different fields. Up to six different fields can be preprogrammed using the field registers.

The VEQSEL registers, one for each region, select which of the 10 vertical sequences will be active during each region. The SWEEP registers are used to enable the sweep mode during any region. The MULTI registers are used to enable the multiplier mode during any region. The SCP registers create the line boundaries for each region. The VDLEN register specifies the total number of lines in the field. The total number of pixels per line (HDLEN) is specified in the vertical sequence registers, but the HDLAST register specifies the number of pixels in the last line of the field. Note that the 13th bit (MSB) of the last line length is located in a separate register. During the sensor gate (SG) line, the VPATSECOND register is used to add a second vertical pattern group to the XV outputs.

The SGMASK register is used to enable or disable each individual VSG output. There is a single bit for each XSG output, setting the bit high will mask the output and setting it low will enable the output. The SGPAT register assigns one of the four different SG patterns to each VSG output. The individual SG patterns are created separately using the SG pattern registers. The SGLINE1 register specifies which line in the field will contain the XSG outputs. The optional SGLINE2 register allows the same SG pulses to be repeated on a different line.

Table 15. Field Registers

Register	Length	Range	Description
VSEQSEL	4 b	0 to 9 V Sequence Number	Selected Vertical Sequence for Each Region in the Field.
SWEEP	1 b	High/Low	Enables Sweep Mode for Each Region, When Set High.
MULTI	1 b	High/Low	Enables Multiplier Mode for Each Region, When Set High.
SCP	12 b	0 to 4095 Line Number	Sequence Change Position for Each Region.
VDLEN	12 b	0 to 4095 Number of Lines	Total Number of Lines in Each Field.
HDLAST	13 b	0 to 8191 Number of Pixels	Length in Pixels of the Last HD Line in Each Field. The13th bit (MSB) is located in a separate register to maintain compatibility with the AD9995.
VPATSECOND	4 b	0 to 9 Vertical Pattern Group Number	Selected Vertical Pattern Group for Second Pattern Applied During SG Line.
SGMASK	6 b	High/Low, Each XSG	Set High to Mask Each Individual XSG Output. XSG1 [0], XSG2 [1], XSG3 [2], XSG4 [3], XSG5 [4], XSG6 [5].
SGPATSEL	12 b	0 to 3 Pattern Number, Each XSG	Selects the SG Pattern Number for Each XSG Output. XSG1 [1:0], XSG2 [3:2], XSG3 [5:4], XSG4 [7:6], XSG5 [9:8], XSG6 [11:10].
SGLINE1	12 b	0 to 4095 Line Number	Selects the Line in the Field Where the SG Signals Are Active.
SGLINE2	12 b	0 to 4095 Line Number	Selects a Second Line in the Field to Repeat the SG Signals.

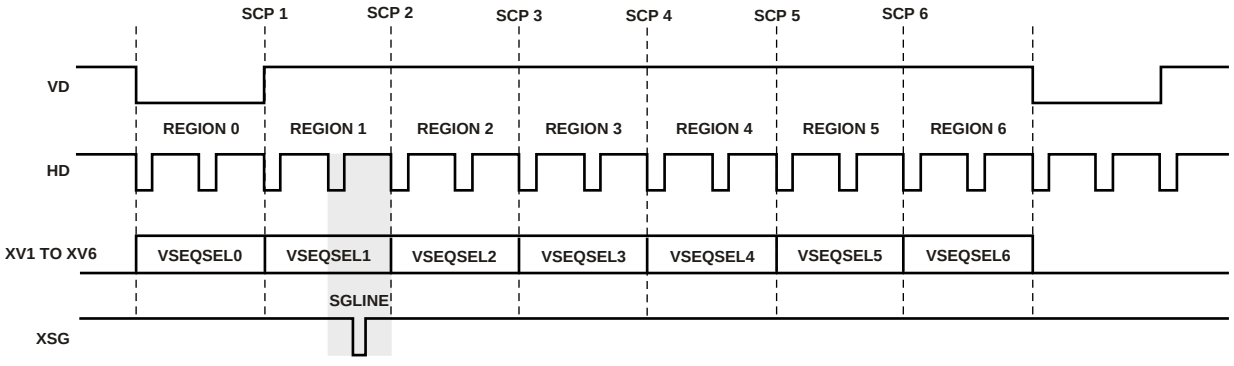


Figure 37. Complete Field Is Divided into Regions

Generating Line Alternation for Vertical Sequence and HBLK

During low resolution readout, some CCDs require a different number of vertical clocks on alternate lines. The AD9925 can support this by using the VPATREPO and VPATREPE registers. This allows a different number of VPAT repetitions to be programmed on odd and even lines. Note that only the number of repeats can be different in odd and even lines, but the VPAT group remains the same.

Additionally, the HBLK signal can also be alternated for odd and even lines. When the HBLKALT register is set high, the HBLK TOG1 and HBLK TOG2 positions will be used on odd lines, and the HBLK TOG3 to HBLK TOG6 positions will be used on even lines. This allows the HBLK interval to be adjusted on odd and even lines if needed.

Figure 38 shows an example of a VPAT repetition alternation and a HBLK alternation used together. It is also possible to use the VPAT and HBLK alternation separately.

Second Vertical Pattern Group during VSG Active Line

Most CCDs require additional vertical timing during the sensor gate (SG) line. The AD9925 supports the option to output a second vertical pattern group for XV1 to XV8 during the line when the sensor gates XSG1 to XSG6 are active. Figure 39 shows a typical SG line that includes two separate sets of vertical pattern group for XV1 to XV6. The vertical pattern group at the start of the SG line is selected in the same manner as the other regions, using the appropriate VSEQSEL register. The second vertical pattern group, unique to the SG line, is selected using the VPATSECOND register, located with the field registers. The start position of the second VPAT group uses the VPATLEN register from the selected VPAT registers. Because the VPATLEN register is used as the start position and not as the VPAT length, it is not possible to program multiple repetitions for the second VPAT group.

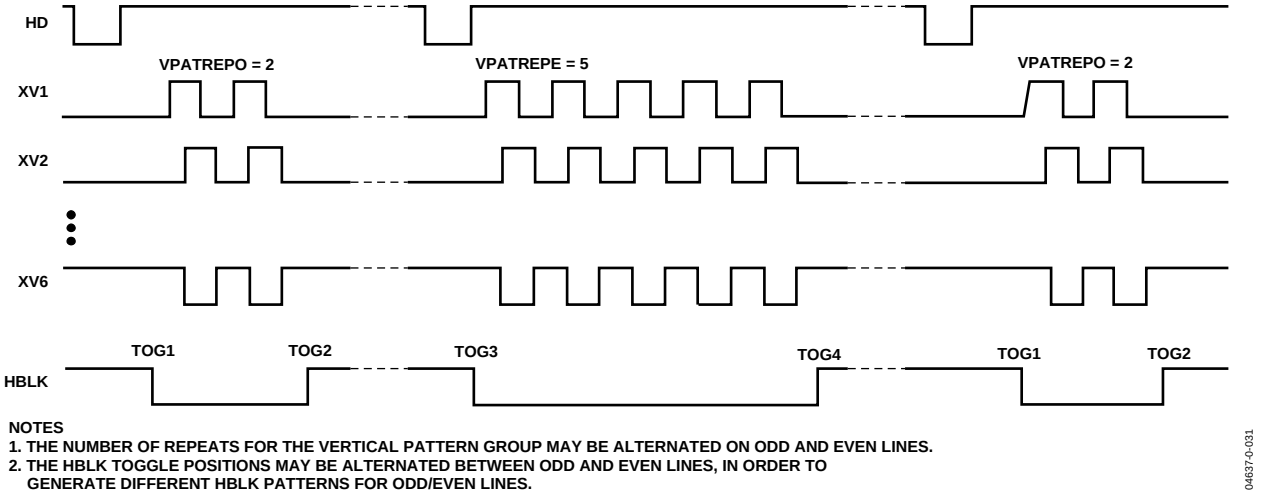


Figure 38. Odd/Even Line Alteration of VPAT Repetitions and HBLK Toggle Positions

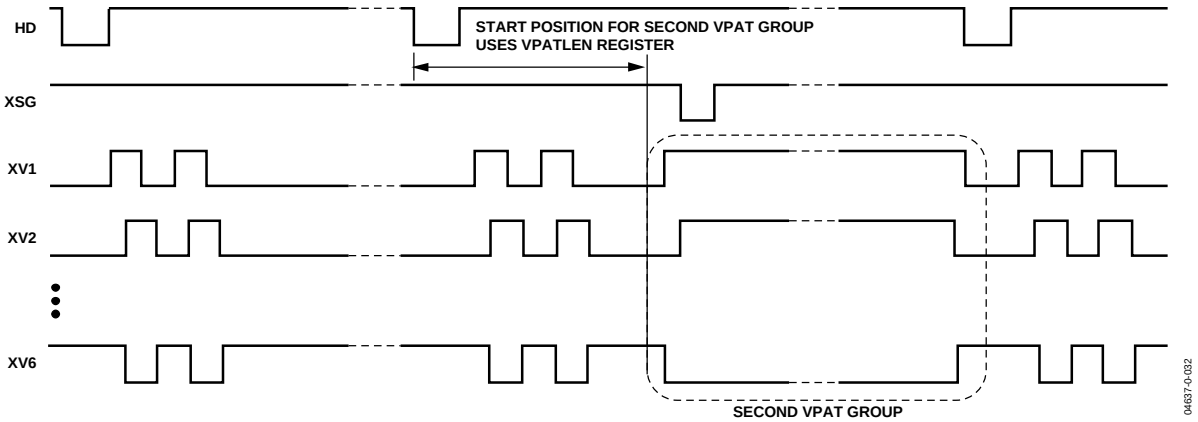


Figure 39. Example of Second VPAT Group during Sensor Gate Line

Sweep Mode Operation

The AD9925 contains an additional mode of vertical timing operation called sweep mode. This mode is used to generate a large number of repetitive pulses that span across multiple HD lines. One example of where this mode is needed is at the start of the CCD readout operation. At the end of the image exposure, but before the image is transferred by the sensor gate pulses, the vertical interline CCD registers should be free of all charge. This can be accomplished by quickly shifting out any charge using a long series of pulses from the XV outputs. Depending on the vertical resolution of the CCD, up to two or three thousand clock cycles will be needed to shift the charge out of each vertical CCD line. This operation will span across multiple HD line lengths. Normally, the AD9925 vertical timing must be contained within one HD line length, but when sweep mode is enabled, the HD boundaries will be ignored until the region is finished. To enable sweep mode within any region, program the appropriate SWEEP register to high.

Figure 40 shows an example of the sweep mode operation. The number of vertical pulses needed depends on the vertical resolution of the CCD. The XV output signals are generated using the vertical pattern registers (shown in Table 15). A single pulse is created using the polarity and toggle position registers. The number of repetitions is then programmed to match the number of vertical shifts required by the CCD. Repetitions are programmed in the vertical sequence registers using the VPATREP registers. This produces a pulse train of the appropriate length. Normally, the pulse train is truncated at the end of the HD line length, but with sweep mode enabled for this region, the HD boundaries are ignored. In Figure 40, the sweep region occupies 23 HD lines. After the sweep mode region is completed in the next region, normal sequence operation will resume. When using sweep mode, be sure to set the region boundaries to the appropriate lines (using the sequence change positions) to prevent the sweep operation from overlapping the next vertical sequence.

Multiplier Mode

To generate very wide vertical timing pulses, a vertical region may be configured into a multiplier region. This mode uses the vertical pattern registers in a slightly different manner. Multiplier mode can be used to support unusual CCD timing requirements, such as vertical pulses that are wider than a single HD line length.

The start polarity and toggle positions are still used in the same manner as the standard VPAT group programming, but the VPATLEN is used differently. Instead of using the pixel counter (HD counter) to specify the toggle position locations (VTOG1, 2, 3) of the VPAT group, the VPATLEN is multiplied with the VTOG position to allow very long pulses to be generated. To calculate the exact toggle position, counted in pixels after the start position, use the following equation:

$$Multiplier\ Mode\ Toggle\ Position = VTOG \times VPATLEN$$

Because the *VTOG* register is multiplied by *VPATLEN*, the resolution of the toggle position placement is reduced. If *VPATLEN* = 4, then the toggle position accuracy will be reduced to a 4-pixel step size, instead of a single pixel step size. Table 16 summarizes how the VPAT group registers are used in multiplier mode operation. In multiplier mode, the VPATREPO and VPATREPE registers should always be programmed to the same value as the highest toggle position.

The example shown in Figure 41 illustrates this operation. The first toggle position is two, and the second toggle position is nine. In nonmultiplier mode, this would cause the vertical sequence to toggle at pixel 2 and then pixel 9 within a single HD line. However, now toggle positions are multiplied by the VTPLEN = 4, so the first toggle occurs at pixel count = 8, and the second toggle occurs at pixel count = 36. Sweep mode has also been enabled to allow the toggle positions to cross the HD line boundaries.

Table 16. Multiplier MODE Register Parameters

Register	Length	Range	Description
MULTI	1 b	High/Low	High Enables Multiplier Mode.
XVPOL	1 b	High/Low	Starting Polarity of XV Signal in Each VPAT Group.
XVTOG1	12 b	0 to 4095 Pixel Location	First Toggle Position for XV Signal in Each VPAT Group.
XVTOG2	12 b	0 to 4095 Pixel Location	Second Toggle Position for XV Signal in Each VPAT Group.
XVTOG3	12 b	0 to 4095 Pixel Location	Third Toggle Position for XV Signal in Each VPAT Group.
VPATLEN	10 b	0 to 1023 Pixels	Used as Multiplier Factor for Toggle Position Counter.
VPATREP	12 b	0 to 4095	VPATREPE/VPATREPO Should Be Set to the Same Value as TOG2 or TOG3.

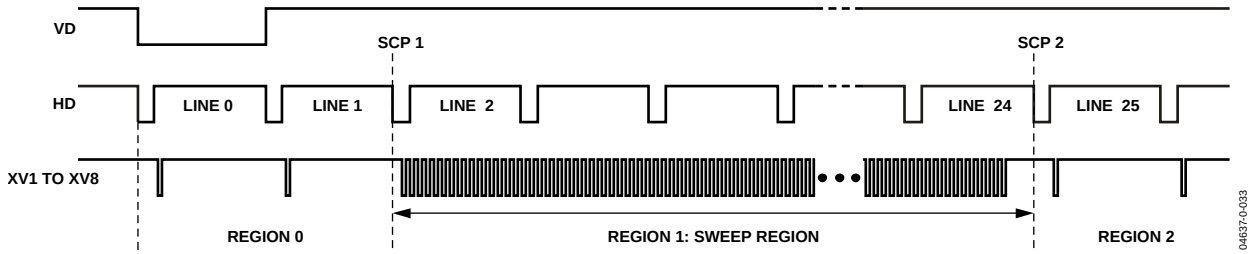


Figure 40. Example of Sweep Region for High Speed Vertical Shift

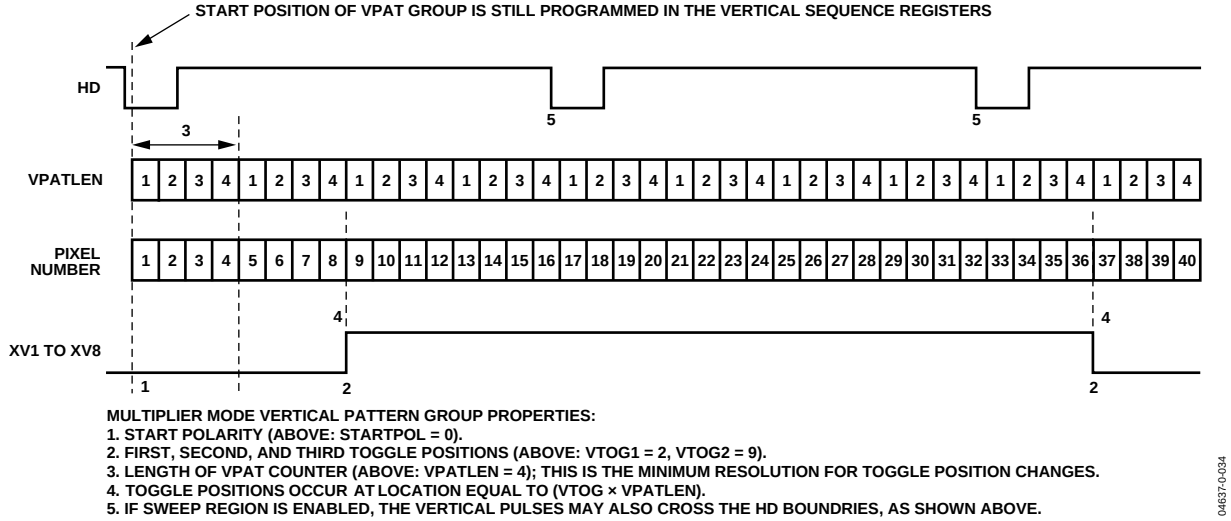


Figure 41. Example of Multiplier Region for Wide Vertical Pulse Timing

Vertical Sensor Gate (Shift Gate) Patterns

In an interline CCD, the sensor gates (SG) are used to transfer the pixel charges from the light-sensitive image area into the light-shielded vertical registers. From the light-shielded vertical registers, the image is then clocked out line-by-line, using the vertical transfer pulses in conjunction with the high speed horizontal clocks.

Table 17 contains the summary of the SG pattern registers. The AD9925 has six SG outputs, XSG1 to XSG6. Each of the outputs can be assigned to one of four programmed patterns by using the SGPATSEL registers. Each pattern is generated in a similar manner as the vertical pattern groups, with a programmable start polarity (SGPOL), first toggle position (SGTOG1), and second toggle position (SGTOG2). The active line where the SG pulses occur is programmable using the SGLINE1 and SGLINE2 registers. Additionally, any of the XSG1 to XSG6 outputs may be individually disabled by using the SGMASK register. The individual masking allows all of the SG patterns to be preprogrammed, and the appropriate pulses for the different fields can be separately enabled. For maximum flexibility, the SGPATSEL, SGMASK, and SGLINE registers are separately programmable for each field. See the Complete Field: Combining Vertical Sequences section for more details.

Additionally, there is a register in Bank 1 (Addr 0x55) that overrides the SG masking in the field registers (Bank 2). The SGMASK_OVR register allows sensor gate masking to be changed without modifying the field register values. Setting the SGMASKOVR_EN bit high enables the SGMASK override function. The SGMASK_OVR register is SCK updated, so the new SG masking values will update immediately.

Table 17. SG Pattern Registers (Also See Field Registers in Table 15)

Register	Length	Range	Description
SGPOL	1 b	High/Low	Sensor Gate Starting Polarity for SG Pattern 0 to 3
SGTOG1	12 b	0 to 4095 Pixel Location	First Toggle Position for SG Pattern 0 to 3
SGTOG2	12 b	0 to 4095 Pixel Location	Second Toggle Position for SG Pattern 0 to 3
SGMASK_OVR	6 b	Six Individual Bits	SG Masking, Overrides the Values in the Field Registers
SGMASKOVR_EN	1 b	Disable/Enable	1: Enables SGMASK Fast Update

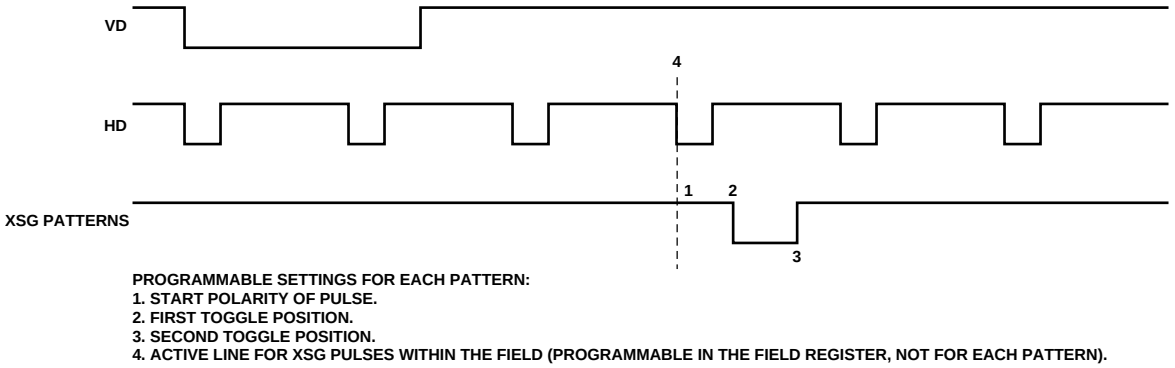


Figure 42. Vertical Sensor Gate Pulse Placement

MODE Register

The MODE register is a single register that selects the field timing of the AD9925. Typically, all the field, vertical sequence, and vertical pattern group information is programmed into the AD9925 at startup. During operation, the MODE register allows the user to select any combination of field timing to meet the current requirements of the system. The advantage of using the MODE register in conjunction with preprogrammed timing is that it greatly reduces the system programming requirements during camera operation. Only a few register writes are required when the camera operating mode is changed, rather than having to write in all the vertical timing information with each camera mode change.

A basic still camera application might require five different fields of vertical timing: one for draft mode operation, one for autofocusing, and three for still image readout. All of the register timing information for the five fields would be loaded at startup. Then, during camera operation, the MODE register would select which field timing would be active depending on how the camera was being used. Table 18 shows how the MODE register data bits are used. The three MSBs, D23 to D21, are used to specify how many total fields will be used. Any value from 1 to 7 can be selected using these three bits. The remaining register bits are divided into 3-bit sections to select which of the six fields are used and in which order. Up to seven fields may be used in a single MODE write. The AD9925 will start with the field timing specified by the first field bits, and on the next VD it will switch to the timing specified by the second field bits, and so on.

After completing the total number of fields specified in Bits D23 to D21, the AD9925 will repeat by starting at the first field again. This will continue until a new write to the MODE register occurs. Figure 43 shows examples of the MODE register settings for different field configurations.

Table 18. MODE Register Data Bit Breakdown (D23 = MSB)

D23 D22 D21	D20 D19 D18	D17 D16 D15	D14 D13 D12	D11 D10 D9	D8 D7 D6	D5 D4 D3	D2 D1 D0
Total Number of Fields to Use	**Seventh Field**	**Sixth Field**	**Fifth Field**	**Fourth Field**	**Third Field**	**Second Field**	**First Field**
1 = First Field Only	0 = Field 0	0 = Field 0	0 = Field 0	0 = Field 0	0 = Field 0	0 = Field 0	0 = Field 0
7 = All 7 Fields	5 = Field 5	5 = Field 5	5 = Field 5	5 = Field 5	5 = Field 5	5 = Field 5	5 = Field 5
0 = Invalid	6, 7 = Invalid	6, 7 = Invalid	6, 7 = Invalid	6, 7 = Invalid	6, 7 = Invalid	6, 7 = Invalid	6, 7 = Invalid

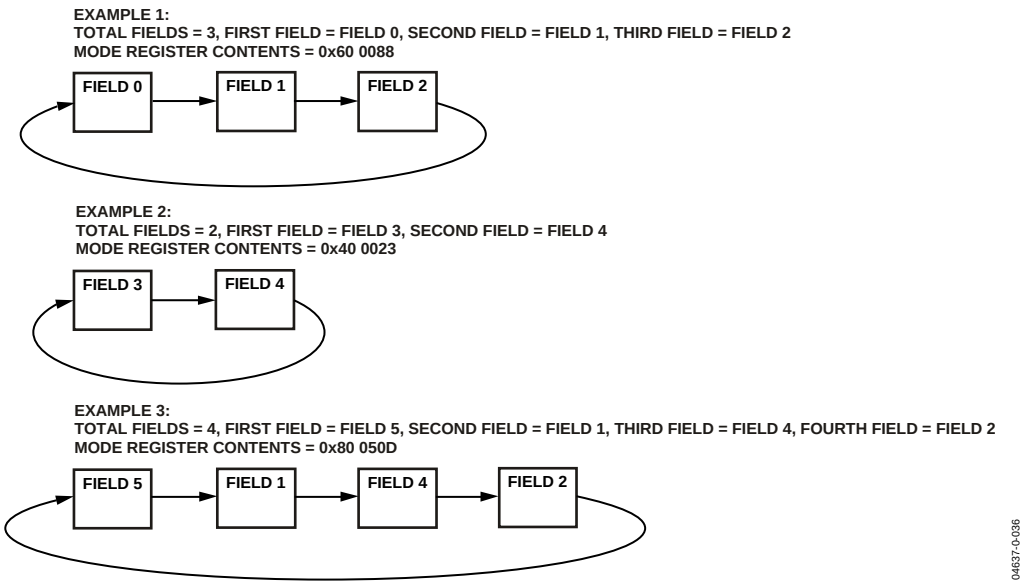


Figure 43. Using the MODE Register to Select Field Timing

VERTICAL TIMING EXAMPLE

To better understand how the AD9925 vertical timing generation is used, consider CCD timing chart in Figure 44. This particular example illustrates a CCD using a general 3-field readout technique. As described in the previous field section, each readout field should be divided into separate regions to perform each step of the readout. The sequence change positions (SCP) determine the line boundaries for each region, and then the VSEQSEL registers assign a particular vertical sequence to each region. The vertical sequences contain the specific timing information required in each region: XV1 to XV6 pulses (using VPAT groups), HBLK/CLPOB timing, and XSG patterns for the SG active lines.

This particular timing example requires four regions for each of the three fields, labeled Region 0, Region 1, Region 2, and Region 3. Because the AD9925 allows up to six individual fields to be programmed, the Field 0, Field 1, and Field 2 registers can be used to meet the requirements of this timing example. The four regions for each field are very similar in this example, but the individual registers for each field allow flexibility to accommodate other timing charts.

Region 0 is a high speed vertical shift region. Sweep mode may be used to generate this timing operation, with the desired number of high speed vertical pulses needed to clear any charge from the CCD's vertical registers. Region 1 consists of only two lines and, like Region 3, uses standard single line vertical shift timing. Region 2 is the sensor gate line, where the VSG pulses transfer the image into the vertical CCD registers. This region may require the use of the second vertical pattern group for the SG active line.

In summary, four regions are required in each of the three fields. The timing for Region 1 and Region 3 is essentially the same, reducing the complexity of the register programming. However, other registers will need to be used during the actual readout operation, such as the MODE register, shutter control registers (TRIGGER, SUBCK, VSUB, MSHUT, and STROBE), and the AFE gain register. These registers will be explained in other examples.

Important Note about Signal Polarities

When programming the AD9925 to generate the XV1 to XV8, XSG1 to XSG6, and SUBCK signals, it is important to note that the vertical driver circuit will invert these signals. Carefully check the required timing signals needed at the output of the vertical driver circuit and adjust the polarities of the XV signals accordingly.

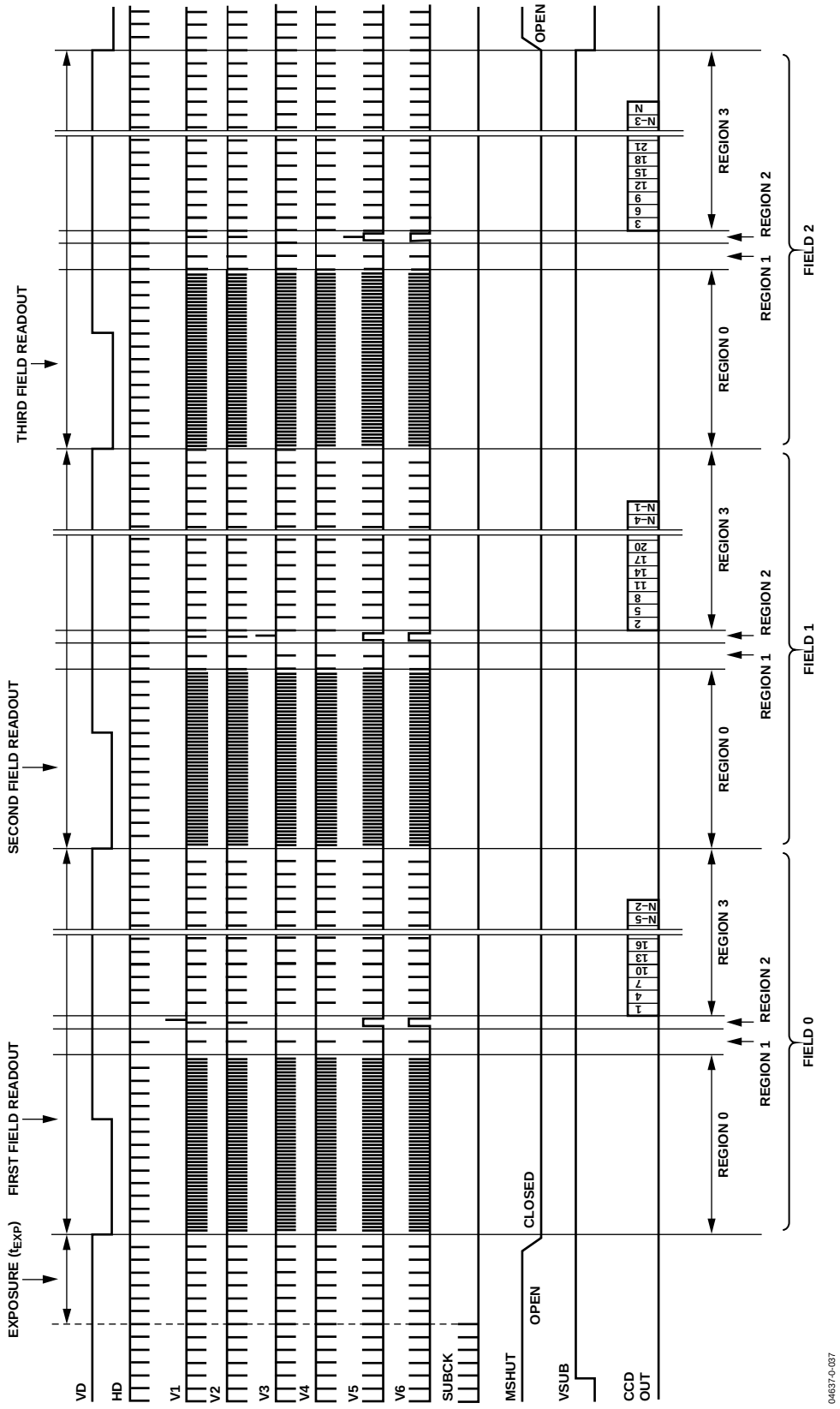


Figure 44. CCD Timing Example—Dividing Each Field into Regions

SHUTTER TIMING CONTROL

The CCD image exposure time is controlled by the substrate clock signal (SUBCK), which pulses the CCD substrate to clear out accumulated charge. The AD9925 supports three types of electronic shuttering: normal, high precision, and low speed. Along with the SUBCK pulse placement, the AD9925 can accommodate different readout configurations to further suppress the SUBCK pulses during multiple field readouts. The AD9925 also provides programmable outputs to control an external mechanical shutter (MSHUT), a strobe/flash (STROBE), and the CCD bias select signal (VSUB).

Normal Shutter Operation

By default, the AD9925 always operates in the normal shutter configuration, in which the SUBCK signal pulses in every VD field (see Figure 45). The SUBCK pulse occurs once per line, and the total number of repetitions within the field will determine the length of the exposure time. The SUBCK pulse polarity and toggle positions within a line are programmable using the SUBCKPOL and SUBCK1TOG registers (see Table 19). The number of SUBCK pulses per field is programmed in the SUBCKNUM register (Addr 0x63).

As shown in Figure 45, the SUBCK pulses will always begin in the line following the SG active line, which is specified in the SGACTLINE registers for each field. The SUBCKPOL, SUBCK1TOG, SUBCK2TOG, SUBCKNUM, and SUBCKSUPPRESS registers are updated at the start of the line after the sensor gate line, as described in the Updating New Register Values section.

High Precision Shutter Operation

High precision shuttering is used in the same manner as normal shuttering, but it uses an additional register to control the last SUBCK pulse. In this mode, the SUBCK still pulses once per line, but the last SUBCK in the field will have an additional SUBCK pulse, the location of which is determined by the SUBCK2TOG register, as shown in Figure 46. Finer resolution of the exposure time is possible using this mode. Leaving the SUBCK2TOG register set to its maximum value (0xFF FFFF) will disable the last SUBCK pulse (default setting).

Low Speed Shutter Operation

Normal and high precision shutter operations are used when the exposure time is less than one field long. For exposure times longer than one field interval, low speed shutter operation is used. The AD9925 uses a separate exposure counter to achieve long exposure times. The number of fields for the low speed shutter operation is specified in the EXPOSURE register (Addr 0x62). As shown in Figure 47, this shutter mode will suppress the SUBCK and VSG outputs for up to 4095 fields (VD periods). The VD and HD outputs may be suppressed during the exposure period by programming the VDHDOFF register to 1.

To generate a low speed shutter operation, it is necessary to trigger the start of the long exposure by writing to the TRIGGER Register Bit D3. When this bit is set high, at the next VD edge, the AD9925 will begin an exposure operation. If a value greater than 0 is specified in the EXPOSURE register, AD9925 will suppress the SUBCK output on subsequent fields.

If the exposure is generated using the TRIGGER register and the EXPOSURE register is set to 0, then the behavior of the SUBCK will not be any different than that of normal shutter or high precision shutter operations, in which the TRIGGER register is not used.

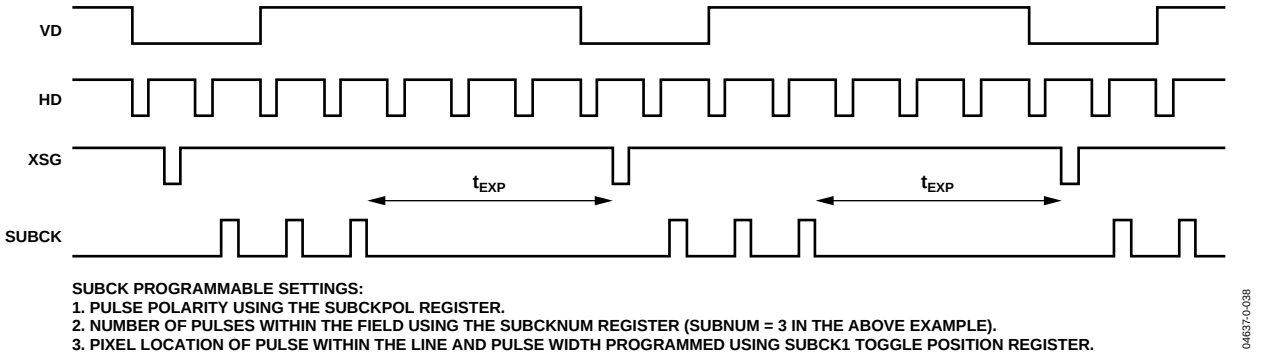


Figure 45. Normal Shutter Mode

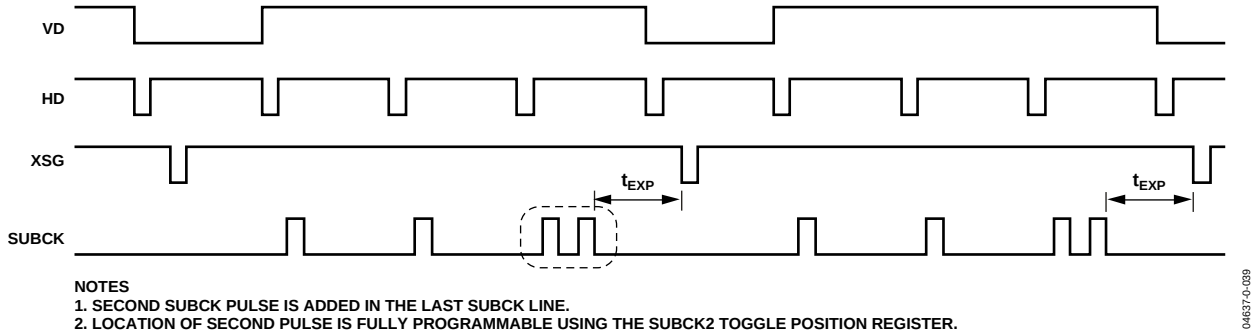


Figure 46. High Precision Shutter Mode

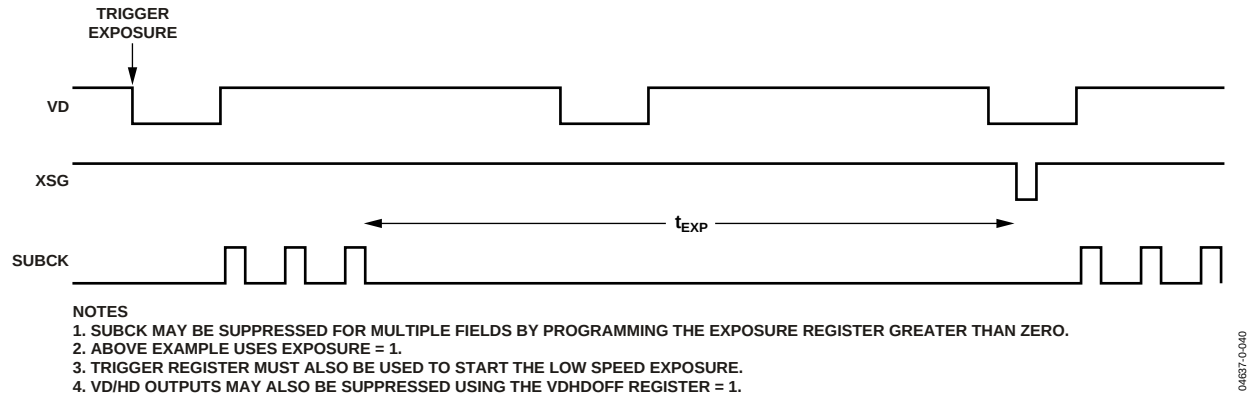


Figure 47. Low Speed Shutter Mode Using EXPOSURE Register

Table 19. Shutter MODE Register Parameters

Register	Length	Range	Description
TRIGGER	5 b	On/Off for Five Signals	Trigger for VSUB [0], MSHUT [1], STROBE [2], Exposure [3], and Readout Start [4]
READOUT	3 b	0 to 7 Number of Fields	Number of Fields to Suppress SUBCK after Exposure
EXPOSURE	12 b	0 to 4095 Number of Fields	Number of Fields to Suppress to SUBCK and VSG during Exposure Time (Low Speed Shutter)
VDHDOFF	1 b	On/Off	Disable VD/HD Output during Exposure (1 = On, 0 = Off)
SUBCKPOL[1]	1 b	High/Low	SUBCK Start Polarity for SUBCK1 and SUBCK2
SUBCK1TOG[1]	24 b	0 to 4095 Pixel Locations	Toggle Positions for First SUBCK Pulse (Normal Shutter)
SUBCK2TOG[1]	24 b	0 to 4095 Pixel Locations	Toggle Positions for Second SUBCK Pulse in Last Line (High Precision)
SUBCKNUM[1]	12 b	1 to 4095 Number of Pulses	Total Number of SUBCKs per Field, at 1 Pulse per Line
SUBCKSUPPRESS[1]	12 b	0 to 4095 Number of Pulses	Number of Lines to Further Suppress SUBCK after the VSG Line

[1] Register is not VD updated, but is updated at the start of the line after the sensor gate line.

SUBCK Suppression

Normally, the SUBCKs will begin to pulse on the line following the sensor gate line (VSG). With some CCDs, the SUBCK pulse needs to be suppressed for one or more lines following the VSG line. The SUBCKSUPPRESS register allows for the suppression of the SUBCK pulses for lines following the VSG line.

Readout after Exposure

After the exposure, the readout of the CCD data occurs, beginning with the sensor gate (VSG) operation. By default, the AD9925 is generating the VSG pulses in every field. In the case where only a single exposure and a single readout frame is needed, such as the CCD's preview mode, the VSG and SUBCK pulses can operate in every field.

However, in many cases, during readout, the SUBCK output needs to be further suppressed until the readout is completed. The READOUT register specifies the number of additional fields after the exposure to continue the suppression of SUBCK. READOUT can be programmed for zero to seven additional fields and should be preprogrammed at startup, not at the same time as the exposure write. A typical interlaced CCD frame readout mode will generally require two additional fields of SUBCK suppression (READOUT = 2). A 3-field, 6-phase CCD will require three additional fields of SUBCK suppression after the readout begins (READOUT = 3).

If the SUBCK output is required to start back up during the last field of readout, simply program the READOUT register to one less than the total number of CCD readout fields.

Like the exposure operation, the readout operation must be triggered using the TRIGGER register.

Using the TRIGGER Register

As described above, by default, the AD9925 will output the SUBCK and VSG signals on every field. This works well for continuous single-field exposure and readout operations, such as the CCD's live preview mode. However, if the CCD requires a longer exposure time, or if multiple readout fields are needed, the TRIGGER register needs to initiate specific exposure and readout sequences.

Typically, the exposure and readout bits in the TRIGGER register are used together. This will initiate a complete exposure-plus readout operation. Once the exposure has been completed, the readout will automatically occur. The values in the EXPOSURE and READOUT registers will determine the length of each operation.

It is possible to independently trigger the readout operation without triggering the exposure operation. This will cause the readout to occur at the next VD, and the SUBCK output will be suppressed according to the value of the READOUT register.

The TRIGGER register is also used to control the STROBE, MSHUT, and VSUB signal transitions. Each of these signals is individually controlled, although they will be dependent on the triggering of the exposure and readout operation.

See Figure 49 for a complete example of triggering the exposure and readout operations.

VSUB Control

The CCD readout bias (VSUB) can be programmed to accommodate different CCDs. Figure 48 shows two different modes that are available. In Mode 0, VSUB goes active during the field of the last SUBCK when the exposure begins. The on position (rising edge in Figure 48) is programmable to any line within the field. VSUB will remain active until the end of the image readout. In Mode 1, the VSUB is not activated until the start of the readout.

An additional function called VSUB keep-on is also available. When this bit is set high, the VSUB output will remain on (active) even after the readout has finished. To disable the VSUB, set this bit back to low.

MSHUT and STROBE Control

MSHUT and STROBE operation is shown in Figure 49, Figure 50, and Figure 51. Table 20 shows the registers parameters for controlling the MSHUT and STROBE outputs. The MSHUT output is switched on with the MSHUTON registers, and it will remain on until the location specified in the MSHUTOFF is reached. The location of MSHUTOFF is fully programmable to anywhere within the exposure period, using the FD (field), LN (line), and PX (pixel) registers. The STROBE pulse is defined by the on and off positions. STROBON_FD is the field in which the STROBE is turned on, measured from the field containing the last SUBCK before exposure begins. The STROBON_ LN PX register gives the line and pixel positions with respect to STROBON_FD. The STROBE off position is programmable to any field, line, and pixel location with respect to the field of the last SUBCK.

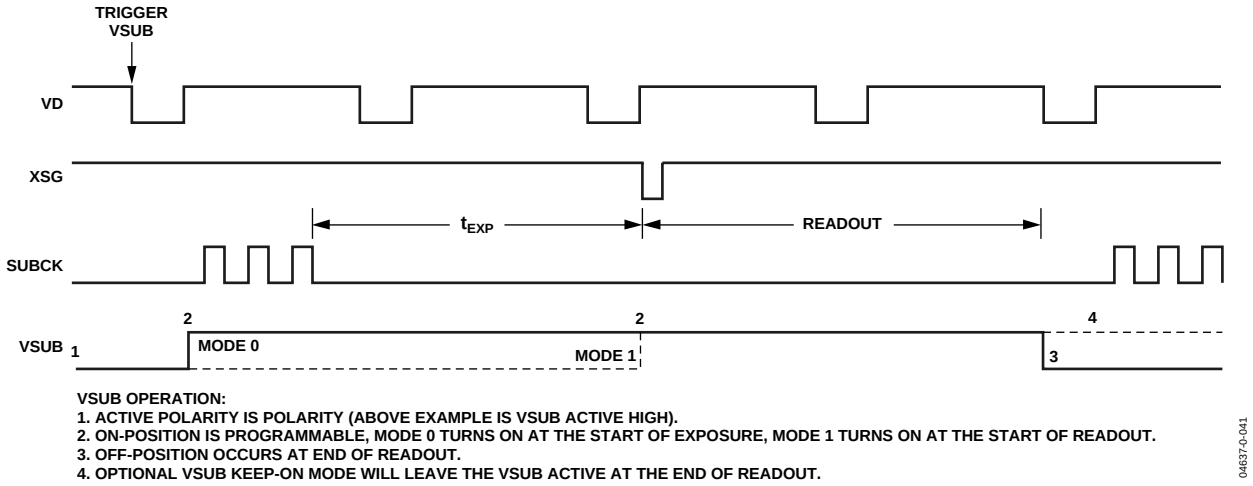


Figure 48. VSUB Programmability

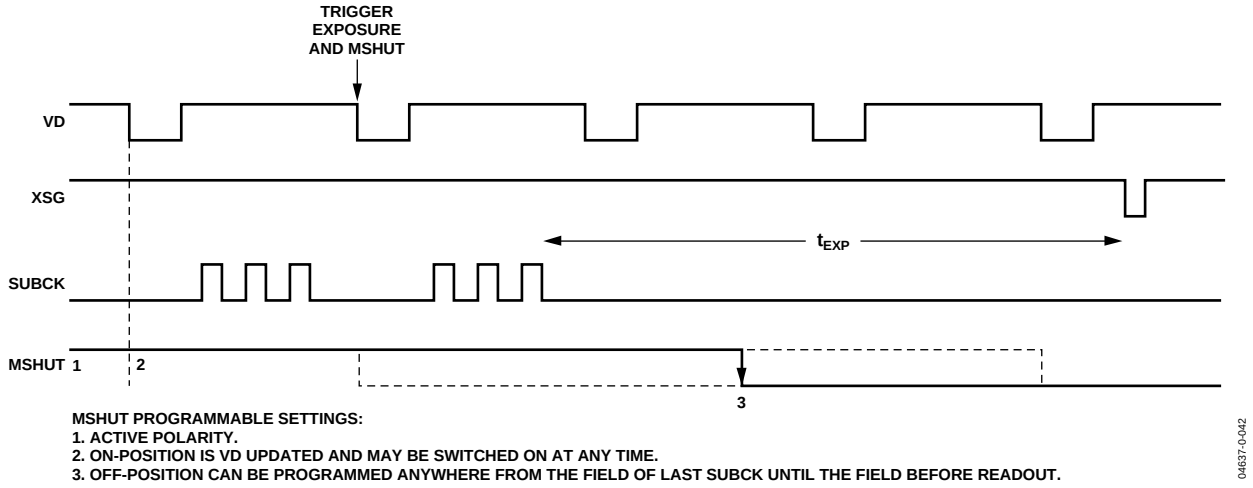


Figure 49. MSHUT Output Programmability

TRIGGER Register Limitations

Although the TRIGGER register can be used to perform a complete exposure and readout operation, there are limitations on its use.

Once an exposure-plus readout operation has been triggered, another exposure/readout operation cannot be triggered right away. There must be at least one idle field (VD intervals) before the next exposure/readout can be triggered. The same limitation applies to the triggering of the MSHUT signal. There must be at least one idle field after the completion of the MSHUT OFF operation before another MSHUT OFF operation can be programmed.

The VSUB trigger requires two idle fields between exposure/readout operations in order to ensure proper VSUB on/off triggering. If the VSUB signal is not required to be turned on and off in between each successive exposure/readout operation, then this limitation can be ignored. Using the VSUB keep-on mode is useful when successive exposure/readout operations are required.

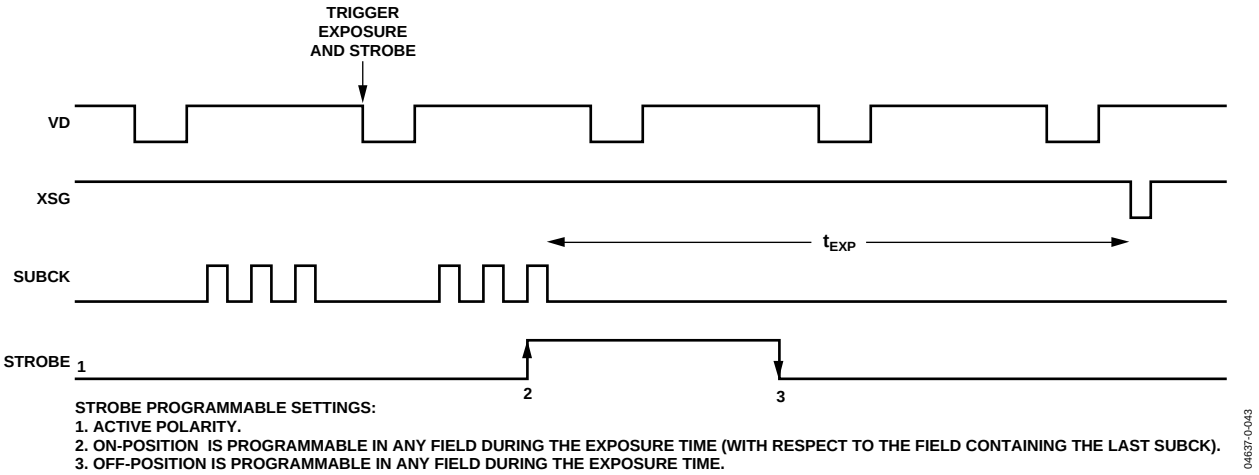


Figure 50. STROBE Output Programmability

Table 20. VSUB, MSHUT, and STROBE Register Parameters

Register	Length	Range	Description
VSUBMODE[0]	1 b	High/Low	VSUB Mode (0 = Mode 0, 1 = Mode 1) (See Figure 44).
VSUBMODE[1]	1 b	High/Low	VSUB Keep-On Mode. VSUB will stay active after readout when set high.
VSUBON[11:0]	12 b	0 to 4095 Line Location	VSUB On Position. Active starting in any line of field.
VSUBON[12]	1 b	High/Low	VSUB Active Polarity.
MSHUTPOL[0]	1 b	High/Low	MSHUT Active Polarity.
MSHUTPOL[1]	1 b	On/Off	MSHUT Manual Enable (1 = Active or Open).
MSHUTON	24 b	0 to 4095 Line/Pixel Location	MSHUT On Position Line [11:0] and Pixel [23:12] Location.
MSHUTOFF_FD	12 b	0 to 4095 Field Location	Field Location to Switch Off MSHUT (Inactive or Closed).
MSHUTOFF_LNPX	24 b	0 to 4095 Line/Pixel Location	Line/Pixel Position to Switch Off MSHUT (Inactive or Closed).
STROBPOL	1 b	High/Low	STROBE Active Polarity.
STROBON_FD	12 b	0 to 4095 Field Location	STROBE ON Field Location, with Respect to Last SUBCK Field.
STROBON_LNPX	24 b	0 to 4095 Line/Pixel Location	STROBE ON Line/Pixel Position.
STROBOFF_FD	12 b	0 to 4095 Field Location	STROBE OFF Field Location, with Respect to Last SUBCK Field.
STROBOFF_LNPX	24 b	0 to 4095 Line/Pixel Location	STROBE OFF Line/Pixel Position.

EXAMPLE OF EXPOSURE AND READOUT OF INTERLACED FRAME

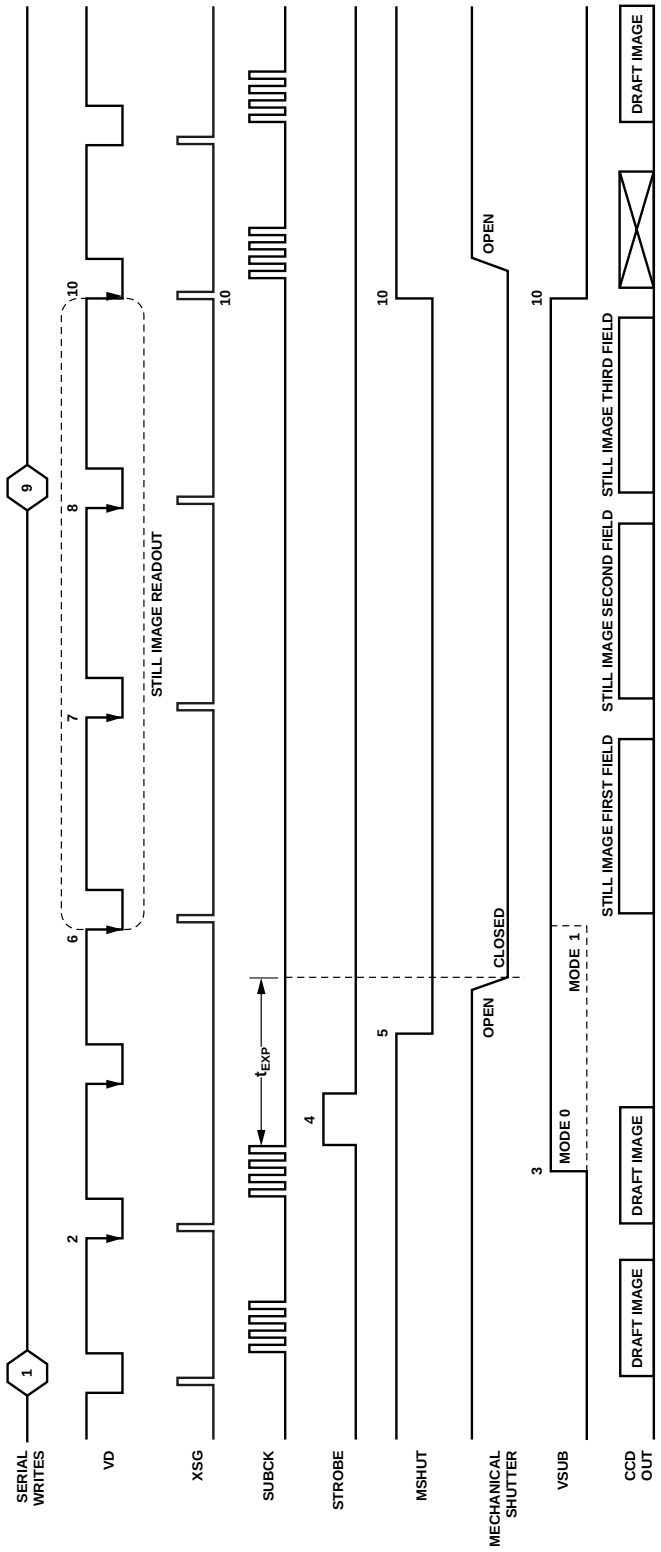


Figure 51. Example of Exposure and Still Image Readout Using Shutter Signals and MODE Register

Refer to Figure 51 for each step:

1. Write to the READOUT register (Addr x61) to specify the number of fields to further suppress SUBCK while the CCD data is readout. In this example, READOUT = 3.

   Write to the EXPOSURE register (Addr x62) to specify the number of fields to suppress SUBCK and VSG outputs during exposure. In this example, EXPOSURE = 1.

   Write to the TRIGGER register (Addr x60) to enable the STROBE, MSHUT, and VSUB signals and to start the exposure/readout operation. To trigger these events (as in Figure 56), set the register TRIGGER = 31. Readout will automatically occur after the exposure period is finished.

   Write to the MODE register (x1B) to configure the next five fields. The first two fields during exposure are the same as the current draft mode fields, and the following three fields are the still frame readout fields. The registers for the draft mode field and the three readout fields have already been programmed.

2. The VD/HD falling edge will update the serial writes from 1.

3. If VSUB mode = 0 (Addr x67), VSUB output will turn on at the line specified in the VSUBON register (Addr x68).

4. STROBE output turns on and off at the location specified in the STROBEON and STROBEOFF registers (Addr x6E to x71).

5. MSHUT output turns off at the location specified in the MSHUTOFF registers (Addr x6B and x6C).

6. The next VD falling edge will automatically start the first readout field.

7. The next VD falling edge will automatically start the second readout field.

8. The next VD falling edge will automatically start the third readout field.

9. Write to the MODE register to reconfigure the single draft mode field timing. Write to the MSHUTON register (Addr x6A) to open the mechanical shutter.

10. VD/HD falling edge will update the serial writes from 9.
    VSG outputs return to draft mode timing.
    SUBCK output resumes operation.
    MSHUT output returns to the on position (active or open).
    VSUB output returns to the off position (inactive).

FG_TRIG OPERATION

The AD9925 contains an additional signal that may be used in conjunction with shutter operation or general system operation. The FG_TRIG signal is an internally generated pulse that can be output on the VSUB or SYNC pins for system use or combined with the VSUB registers to create a four-toggle VSUB signal.

The FG_TRIG signal is generated using the start polarity and first and second toggle position registers, programmable with line and pixel resolution. The field placement of the FG_TRIG pulse is matched to the field count specified by the MODE register operation. The FG_TRIGEN register contains a 3-bit value to specify which field count will contain the FG_TRIG pulse. Figure 53 shows how the FG_TRIG pulse is generated using these registers.

After the FG_TRIG signal is specified, it is enabled using Bit 3 of the FG_TRIGEN register. By default, the FG_TRIG will be mapped to the SYNC output, as long as the SYNC pin is configured as an output (SYNCENABLE = 1). Alternatively, the FG_TRIG pulse may be mapped to the VSUB output by writing a 1 to the SHUT_EXTRA Register Bit 3.

One final application for the FG_TRIG signal is to combine it with the existing VSUB signal to generate additional toggle positions. By setting the SHUT_EXTRA Bit 8 to a 1, the VSUB toggles and FG_TRIG toggles are XOR'd together and sent to the VSUB output. Figure 52 and Figure 54 show this application in more detail.

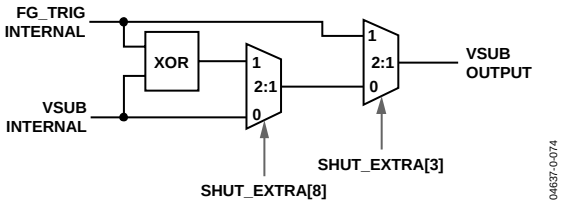


Figure 52. Combining the Internal FG_TRIG and Internal VSUB Signals

Table 21. FG_TRIG Operation Registers

Register	Address	Bit Width	Description
SYNCENABLE	0x12	[0]	1: Configures SYNC Pin as an Output. By default, the FG_TRIG signal outputs on the SYNC pin.
VSUBON	0x68	[12:0]	Controls VSUB On Position and Polarity. When SHUT_Extra [8] = 1, FG_TRIG toggles are combined with VSUB signal.
SHUT_EXTRA	0xE7	[8:0]	Selects Whether FG_TRIG Signal Is Used with VSUB. [2:0] Set to 0. [3] Set = 1 to send FG_TRIG signal to VSUB pin. [7:4] Set to 0. [8] Set = 1 to combine FG_TRIG and VSUB signals.
FG_TRIGEN	0xEB	[3:0]	FG_TRIG Enable. [2:0] Selects field count for pulse (based on mode field counter). [3] Set = 1 to enable FG_TRIG signal output.
FG_TRIGPOL	0xF2	[0]	FG_TRIG Start Polarity.
FG_TRIGLINE1	0xF3	[11:0]	FG_TRIG First Toggle Position, Line Location.
FG_TRIGPIX1	0xF4	[12:0]	FG_TRIG First Toggle Position, Pixel Location.
FG_TRIGLINE2	0xF5	[11:0]	FG_TRIG Second Toggle Position, Line Location.
FG_TRIGPIX2	0xF6	[12:0]	FG_TRIG Second Toggle Position, Pixel Location.

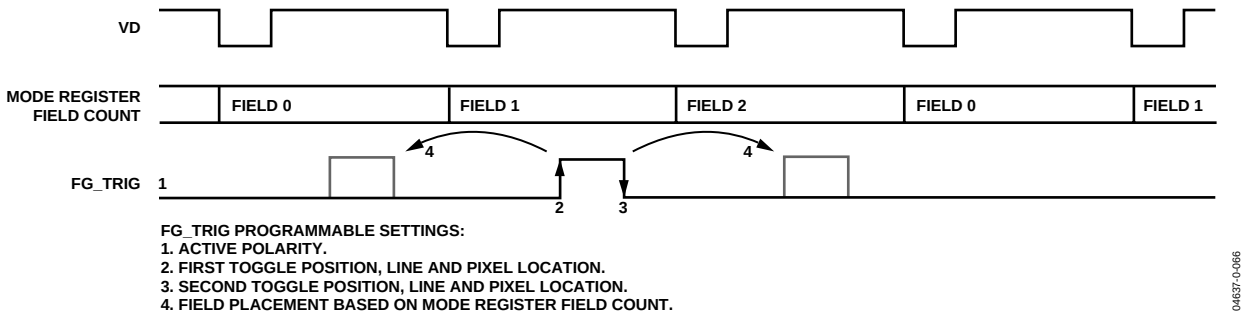


Figure 53. Generating the FG_TRIG Signal

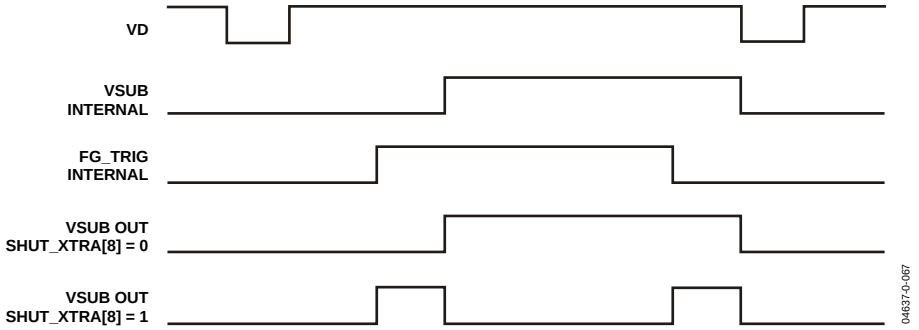


Figure 54. Combining FG_TRIG and VSUB to Create Four Toggle Positions for VSUB Output

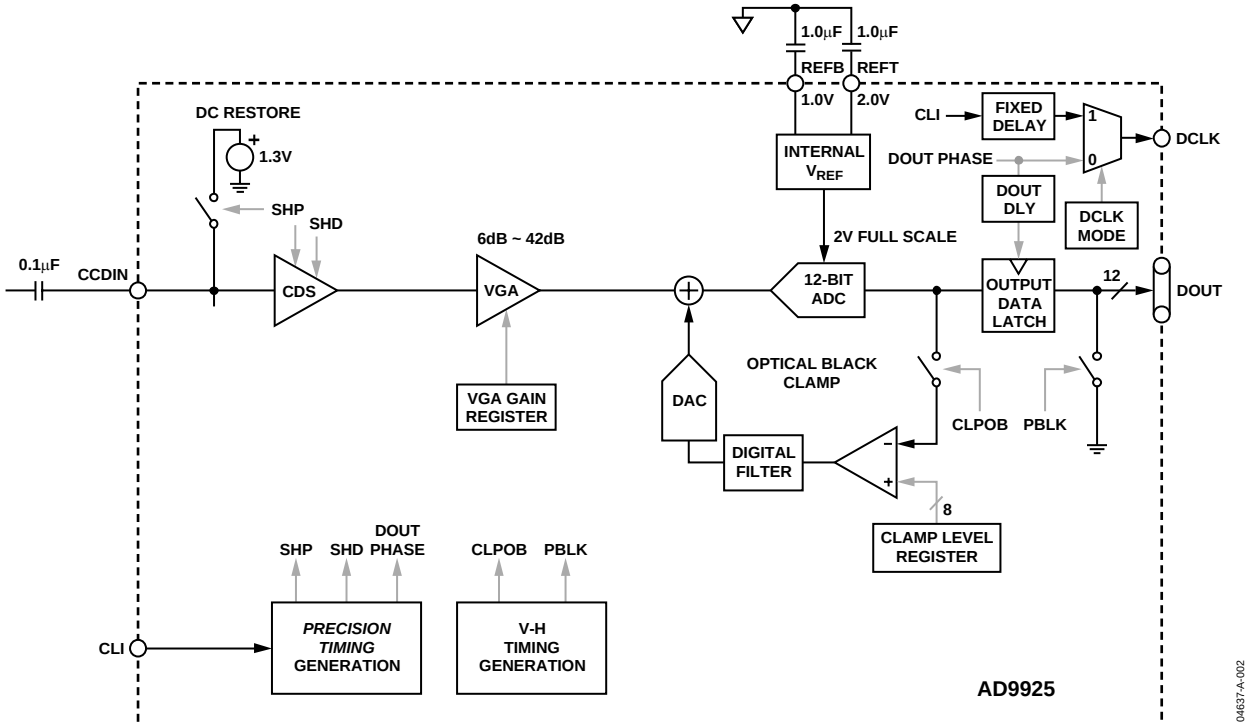


Figure 55. Analog Front End Functional Block Diagram

ANALOG FRONT END DESCRIPTION AND OPERATION

The AD9925 signal processing chain is shown in Figure 55. Each processing step is essential in achieving a high quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc-restore circuit is used with an external 0.1 µF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.3 V, which allows it to be compatible with the 3 V supply voltage of the AD9925.

Correlated Double Sampler

The CDS circuit samples each CCD pixel twice to extract the video information and reject the low frequency noise. The timing shown in Figure 19 illustrates how the two internally generated CDS clocks, SHP and SHD, are used to sample the reference level and data level of the CCD signal, respectively. The placement of the SHP and SHD sampling edges is determined by setting the SAMPCONTROL register located at Addr 0x36. Placement of these two clock signals is critical in achieving the best performance from the CCD.

Variable Gain Amplifier

The VGA stage provides a gain range of 6 dB to 42 dB, programmable with 10-bit resolution through the serial digital interface. The minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. When compared to 1 V full-scale systems, the equivalent gain range is 0 dB to 36 dB.

The VGA gain curve follows a linear-in-dB characteristic. The exact VGA gain can be calculated for any gain register value by using the equation

$$Gain\ (\text{dB}) = (0.0351 \times Code) + 6\ \text{dB}$$

where the *Code* range is 0 to 1023.

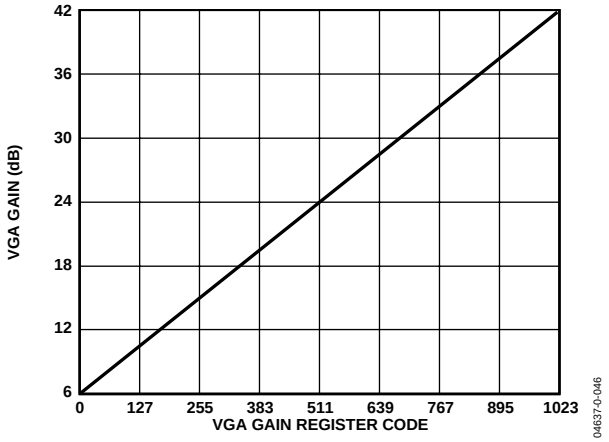


Figure 56. VGA Gain Curve

ADC

The AD9925 uses high performance ADC architecture, optimized for high speed and low power. Differential nonlinearity (DNL) performance is typically better than 0.5 LSB. The ADC uses a 2 V input range. See Figure 10, Figure 12, and Figure 13 for typical linearity and noise performance plots for the AD9925.

Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference, selected by the user in the clamp level register. The value can be programmed between 0 LSB and 255 LSB in 256 steps. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a DAC. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the postprocessing, the AD9925 optical black clamping may be disabled using Bit D2 in the OPRMODE register. When the loop is disabled, the clamp level register may still be used to provide programmable offset adjustment.

The CLPOB pulse should be placed during the CCD's optical black pixels. It is recommended that the CLPOB pulse duration be at least 20 pixels wide. Shorter pulse widths may be used, but the ability to track low frequency variations in the black level will be reduced. See the Horizontal Clamping and Blanking section for timing examples.

Digital Data Outputs

The AD9925 digital output data is latched using the DOUT PHASE register value, as shown in Figure 55. Output data timing is shown in Figure 21 and Figure 22. It is also possible to leave the output latches transparent, so that the data outputs are valid immediately from the ADC. Programming the AFE CONTROL Register Bit D4 to a 1 will set the output latches transparent. The data outputs can also be disabled (three stated) by setting the AFE CONTROL Register Bit D3 to a 1.

The switching of the data outputs can couple noise back to the analog signal path. To minimize any switching noise, it is recommended that the DOUT PHASE register be set to the same edge as the SHP sampling location, or up to 12 edges after the SHP sampling location. Other settings can produce good results, but experimentation is necessary. It is recommended that the DOUT PHASE location not occur between the SHD sampling location and 12 edges after the SHD location. For example, if SHDLOC = 0, then DOUT PHASE should be set to an edge location of 12 or greater. If adjustable phase is not required for the data outputs, the output latch can be left transparent using register 0x03, Bit [4].

The data output coding is normally straight binary, but the coding may be changed to gray coding by setting the AFE CONTROL Register Bit D5 to a 1.

VERTICAL DRIVER SIGNAL CONFIGURATION

As shown in Figure 57, XV1 to XV8, XSG1 to XSG6, and XSUBCK are outputs from the internal AD9925 timing generator, while V1 to V8 and SUBCK are the resulting outputs from the AD9925 vertical driver. The vertical driver performs the mixing of the XV and XSG pulses and amplifies them to the high voltages required for driving the CCD. Additionally, the vertical driver outputs are inverted from the internal XV, XSG, and SUBCK polarities configured by the AD9925 registers.

Table 22 to Table 32 describe the output polarities for these signals vs. their input levels. Refer to these tables when determining the register settings for the desired output levels. Figure 58 to Figure 64 show graphically the relationship between the polarities of the XV and XSG signals and the inverted vertical driver output signals.

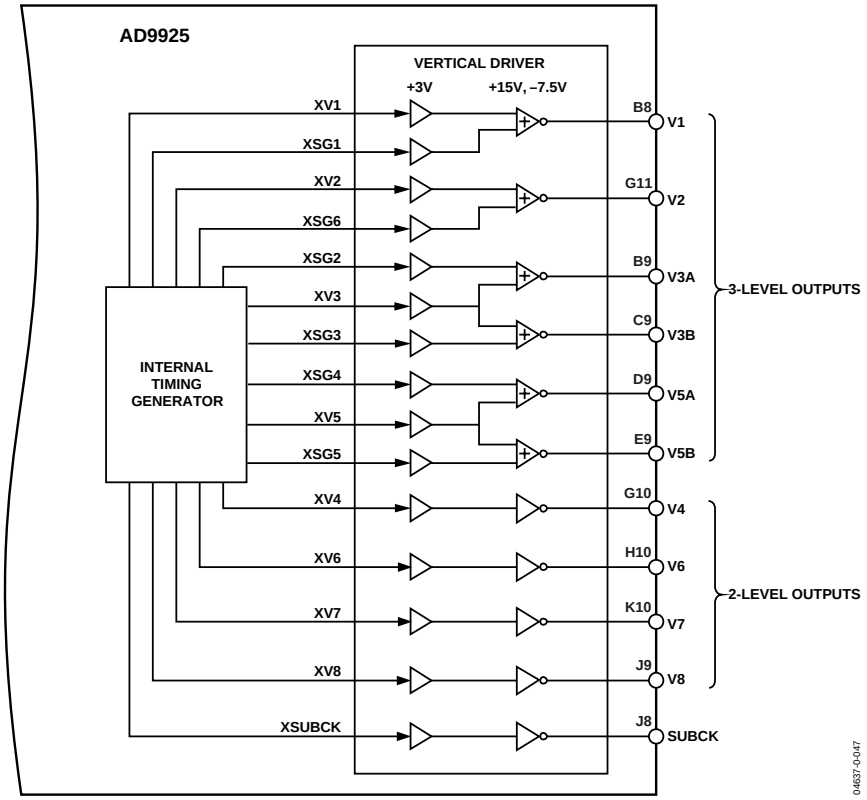


Figure 57. AD9925 Internal V-Driver Input Signals

Table 22. V1 Output Polarity

V-Driver Input		
XV1	XSG1	V1 Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 23. V2 Output Polarity

V-Driver Input		
XV2	XSG6	V2 Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 24. V3A Output Polarity

V-Driver Input		
XV3	XSG2	V3A Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 25. V3B Output Polarity

V-Driver Input		
XV3	XSG3	V3B Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 26. V4 Output Polarity

V-Driver Input	
XV4	V4 Output
L	VM
H	VL

Table 27. V5A Output Polarity

V-Driver Input		
XV5	XSG4	V5A Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 28. V5B Output Polarity

V-Driver Input		
XV5	XSG5	V5B Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 29. V6 Output Polarity

V-Driver Input	
XV6	V6 Output
L	VM
H	VL

Table 30. V7 Output Polarity

V-Driver Input	
XV7	V7 Output
L	VM
H	VL

Table 31. V8 Output Polarity

V-Driver Input	
XV8	V8 Output
L	VM
H	VL

Table 32. SUBCK Output Polarity

V-Driver Input	
XSUBCK	SUBCK Output
L	VH
H	VL

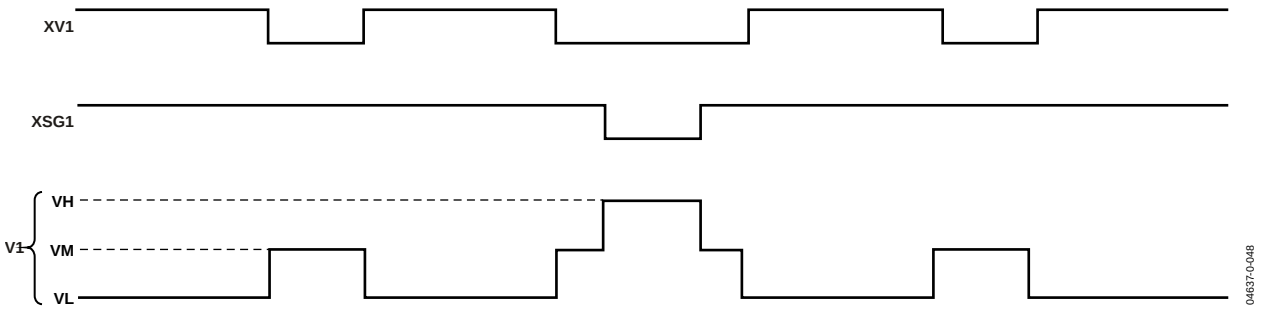


Figure 58. XV1, XSG1, and V1 Output Polarities

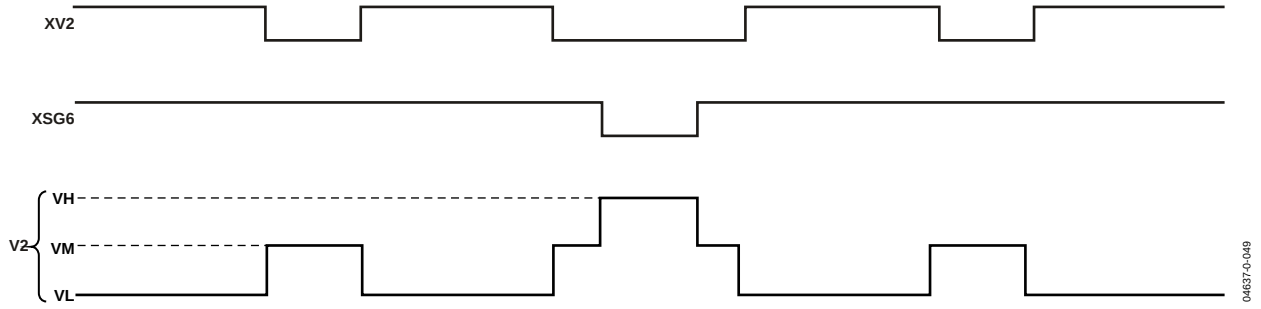


Figure 59. XV2, XSG6, and V2 Output Polarities

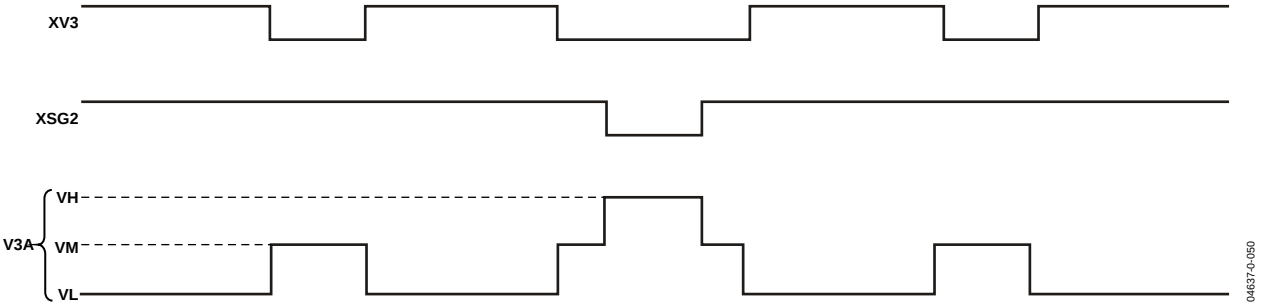


Figure 60. XV3, XSG2, and V3A Output Polarities

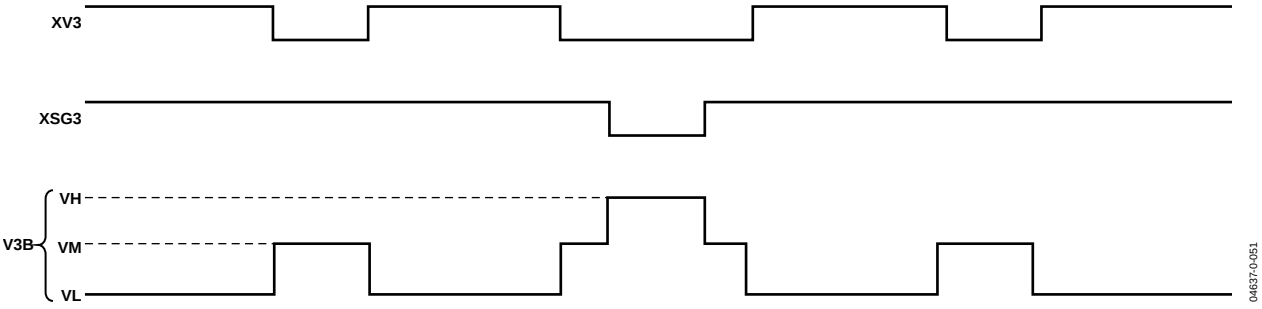


Figure 61. XV3, XSG3, and V3B Output Polarities

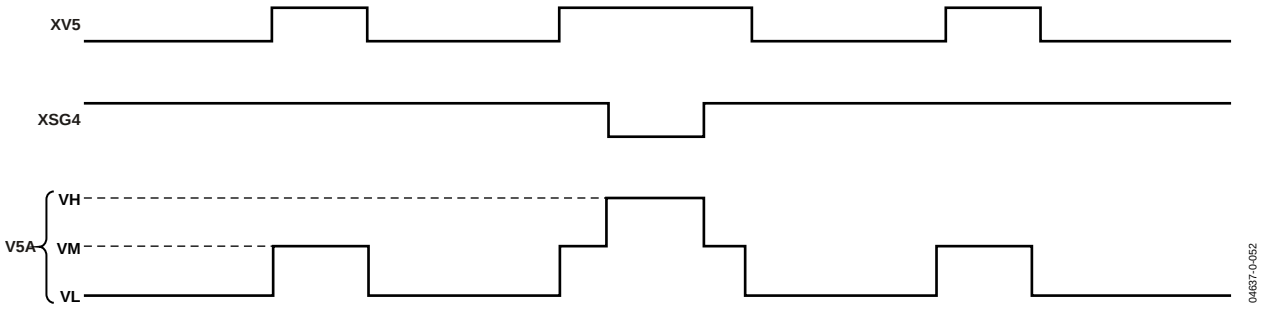


Figure 62. XV5, XSG4, and V5A Output Polarities

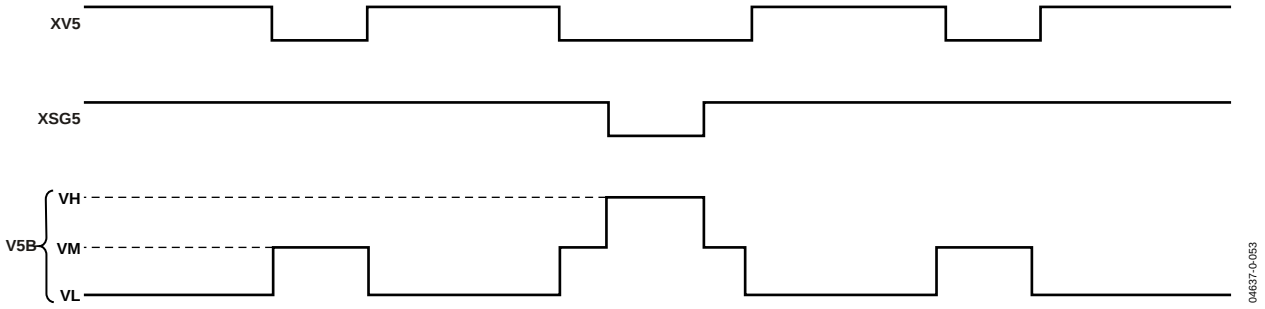


Figure 63. XV5, XSG5, and V5B Output Polarities

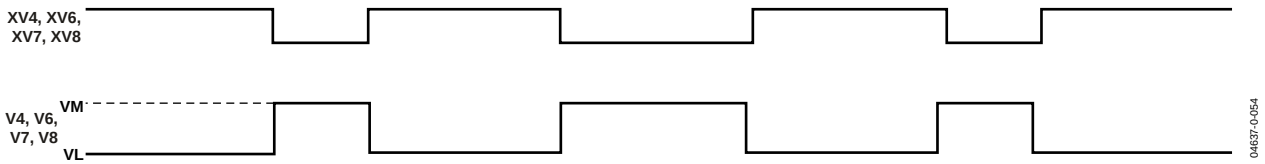


Figure 64. XV4, XV6, XV7, XV8 and V4, V6, V7, V8 Output Polarities

POWER-UP AND SYNCHRONIZATION

Vertical Driver Power Supply Sequencing

The recommended Power-Up and Power-Down sequences are shown in Figure 65 and Figure 66, respectively. As shown, the VM1 and VM2 voltage levels should never exceed the VH1 and VH2 voltage levels during power-up or power-down. Excessive current will result if this requirement is not met due to a PN junction diode turning on between the VM1/VM2 and VH supply pins.

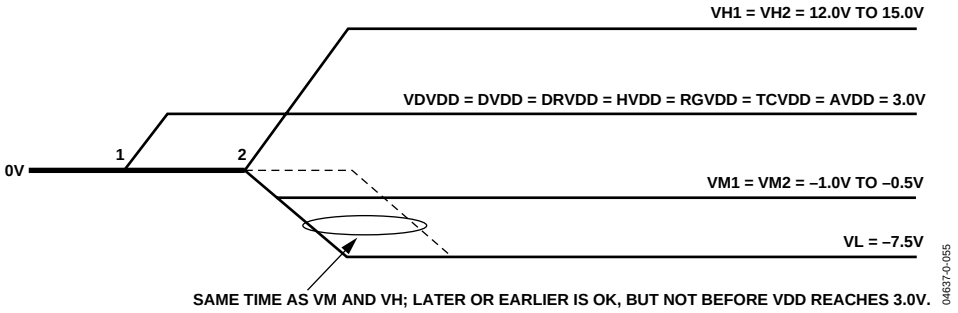


Figure 65. Power-Up Sequence

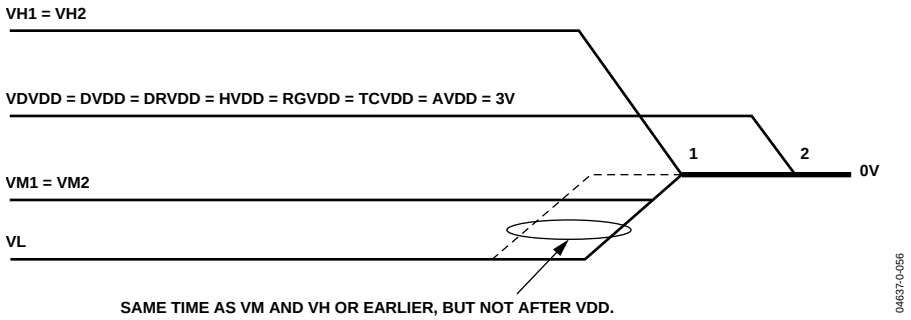


Figure 66. Power-Down Sequence

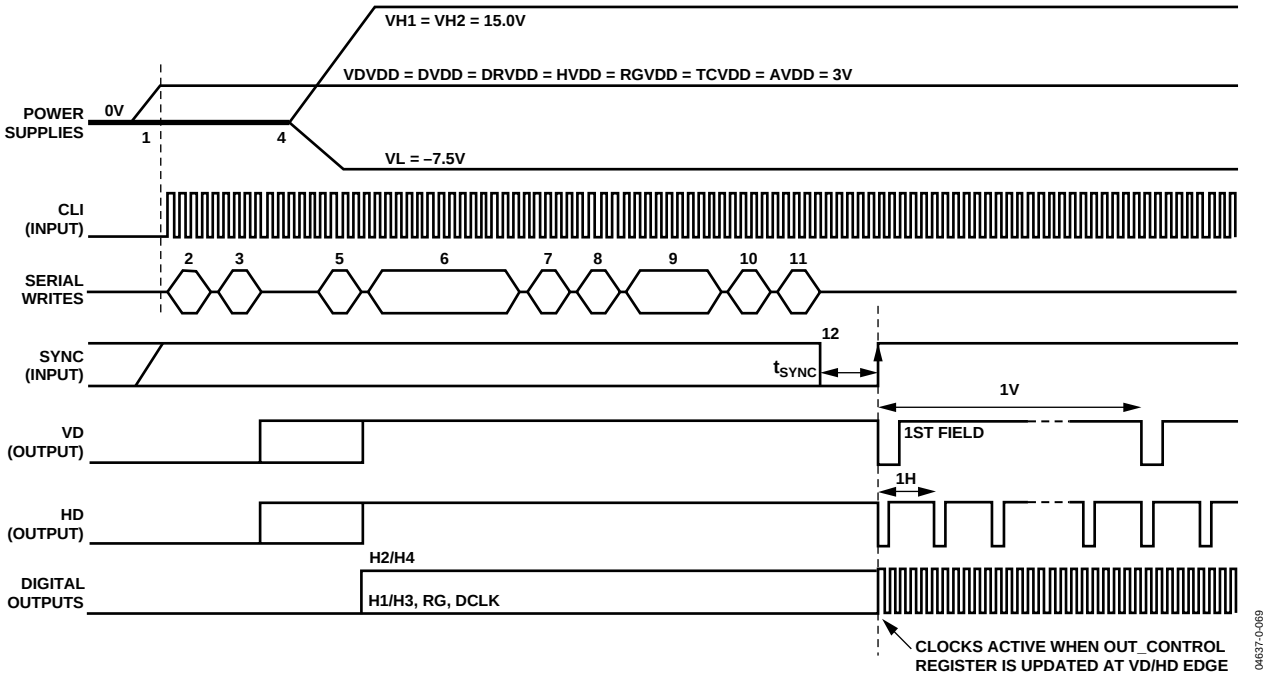


Figure 67. Recommended Power-Up Sequence and Synchronization, Master Mode

Recommended Power-Up Sequence for Master Mode

When the AD9925 is powered up, the following sequence is recommended (refer to Figure 67 for each step). Note that a SYNC signal is required for master mode operation. If an external SYNC pulse is not available, it is also possible to generate an internal SYNC pulse by writing to the SYNCPOL register, as described in the next section.

1. Turn on power supplies for the AD9925 and apply master clock CLI.
2. Reset the internal AD9925 registers by writing a 1 to the SW_RESET register (Addr 0x10 in Bank 1).
3. Write to the standby mode polarity registers 0x0A to 0x0D to set the proper polarities for the V-driver inputs, in order to avoid damage to the CCD. See Table 35 for settings.
4. The V-driver supplies, VH and VL, can then be powered up anytime after completing Step 3 to set the proper polarities.
5. By default, the AD9925 is in standby 3 mode. To place the part into normal power operation, write 0x004 to the AFE OPRMODE register (Addr 0x00 in Bank 1).
6. Write a 1 to the BANKSELECT register (Addr 0×7F)). This will select Register Bank 2. Load Bank 2 registers with the required VPAT group, vertical sequence, and field timing information.
7. Write a 0 to the BANKSELECT register to select Bank 1.
8. By default, the internal timing core is held in a reset state with TGCORE_RSTB register = 0. Write a 1 to the TGCORE_RSTB register (Addr 0x15 in Bank 1) to start the internal timing core operation. Note: If a 2x clock is used for the CLI input, the CLIDIVIDE register (Addr 0x30) should be set to 1 *before* resetting the timing core.
9. Load the required registers to configure the high speed timing, horizontal timing, and shutter timing information.
10. Configure the AD9925 for master mode timing by writing a 1 to the MASTER register (Addr 0x20 in Bank 1).
11. Write a 1 to the OUT_CONTROL register (Addr 0x11 in Bank 1).This will allow the outputs to become active after the next SYNC rising edge.
12. Generate a SYNC event: If SYNC is high at power-up, bring the SYNC input low for a minimum of 100 ns. Then bring SYNC back to high. This will cause the internal counters to reset and will start the VD/HD operation. The first VD/HD edge allows most Bank 1 register updates to occur, including OUT_CONTROL to enable all outputs.

Table 33. Power-Up Register Write Sequence

Address	Data	Description
0x10	0x01	Reset All Registers to Default Values
0x0A to 0x0D	TBD	Standby V-Driver Input Signal Polarities
0x00	0x04	Power-Up the AFE and CLO Oscillator
0x7F	0x01	Select Register Bank 2
0x00 to 0xFF	TBD	VPAT, Vertical Sequence, and Field Timing
0x7F	0x00	Select Register Bank 1
0x15	0x01	Reset Internal Timing Core
0x31 to 0x71	TBD	Horizontal and Shutter Timing
0x20	0x01	Configure for Master Mode
0x11	0x01	Enable All Outputs after SYNC
0x13	0x01	SYNCPOL (for Software SYNC Only)

Generating Software SYNC without External SYNC Signal

If an external SYNC pulse is not available, it is possible to generate an internal SYNC in the AD9925 by writing to the SYNCPOL register (Addr 0x13). If the software SYNC option is used, the SYNC input (Pin J5) should be tied to ground (VSS).

After power-up, follow the same procedure as before, for Steps 1 through 11. Then, for Step 12, instead of using the external SYNC pulse, write a 1 to the SYNCPOL register. This will generate the SYNC internally, and the timing operation will begin.

SYNC during Master Mode Operation

The SYNC input may be used any time during operation to resync the AD9925 counters with external timing, as shown in Figure 68. The operation of the digital outputs may be suspended during the SYNC operation by setting the SYNCSUSPEND register (Addr 0x14) to a 1.

Power-Up and Synchronization in Slave Mode

The power-up procedure for slave mode operation is the same as the procedure described for master mode operation, with two exceptions:

1. Eliminate Step 10. Do not write the part into master mode.
2. No SYNC pulse is required in slave mode. Substitute Step 12 with starting the external VD and HD signals. This will synchronize the part, allow the Bank 1 register updates, and start the timing operation.

When the AD9925 is used in slave mode, the VD and HD inputs are used to synchronize the internal counters. Following a falling edge of VD, there will be a latency of 23 master clock edges (CLI) after the falling edge of HD until the internal H-Counter is reset. The reset operation is shown in Figure 69.

Vertical Toggle Position Placement near Counter Reset

One additional consideration during the reset of the internal counters is the vertical toggle position placement. Before the internal counters are reset, there is an area of 18 pixels where no toggle positions should be programmed.

For master mode, the last 18 pixels before the HD falling edge should not be used for toggle position placement of the XV, XSG, SUBCK, HBLK, PBLK, or CLPOB pulses (see Figure 70).

Figure 71 shows the same example for slave mode. The same restriction applies: the last 18 pixels before the counters are reset and cannot be used. However, in slave mode, the counter reset is delayed with respect to VD/HD placement; therefore, the inhibited area is different than it is in master mode.

Additional Considerations for Toggle Positions

In addition to avoiding toggle position placement near the counter-reset location, there are a couple of other recommendations.

Pixel location 0 should not be used for any of the toggle positions for the XSG and SUBCK pulses.

Also, the propagation delay of the V-driver circuit should be considered when programming the toggle positions for the XV, XSG, and SUBCK pulses. The delay of the V-driver circuit is specified in Table 3 and is a maximum of 200 ns.

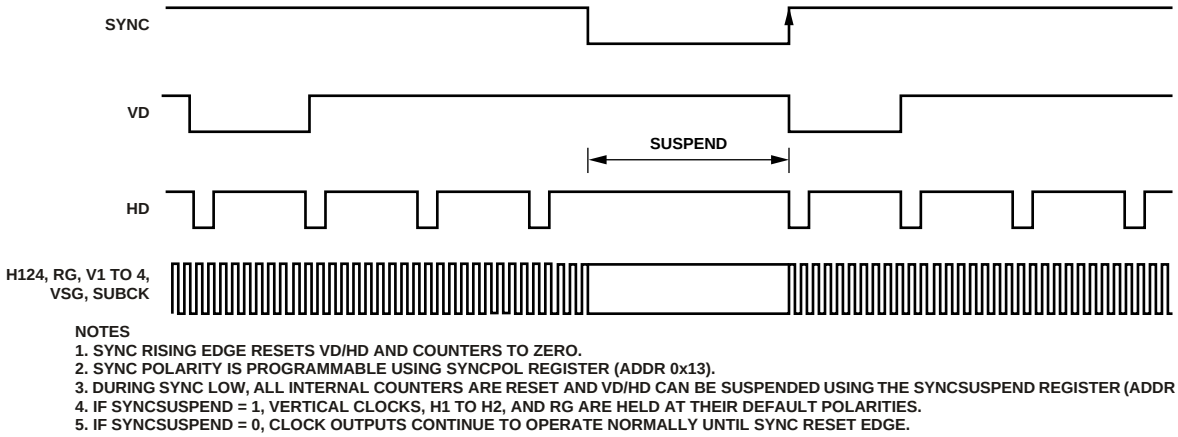


Figure 68. SYNC Timing to Synchronize AD9925 with External Timing

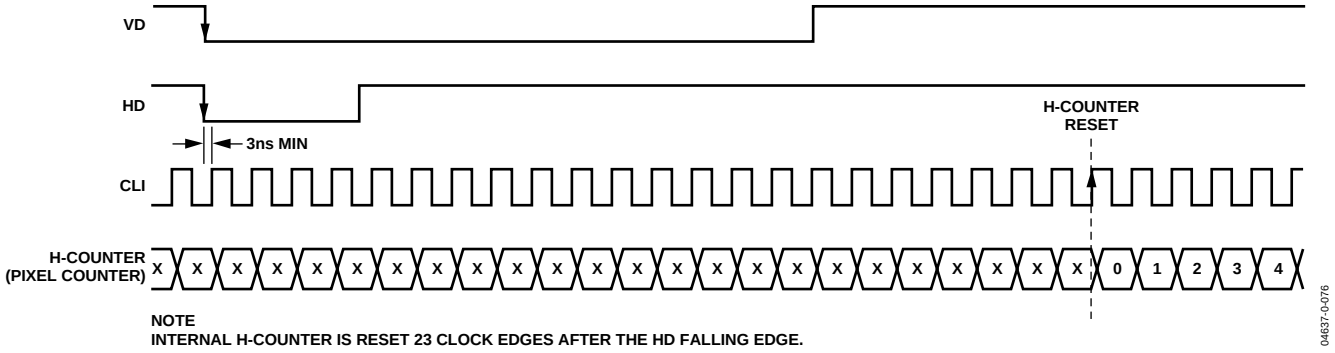


Figure 69. External VD/HD and Internal H-Counter Synchronization, Slave Mode

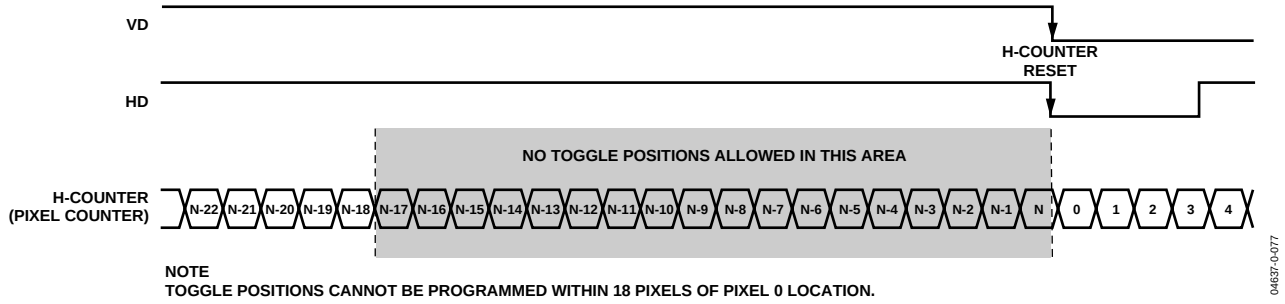


Figure 70. Toggle Position Inhibit Area, Master Mode

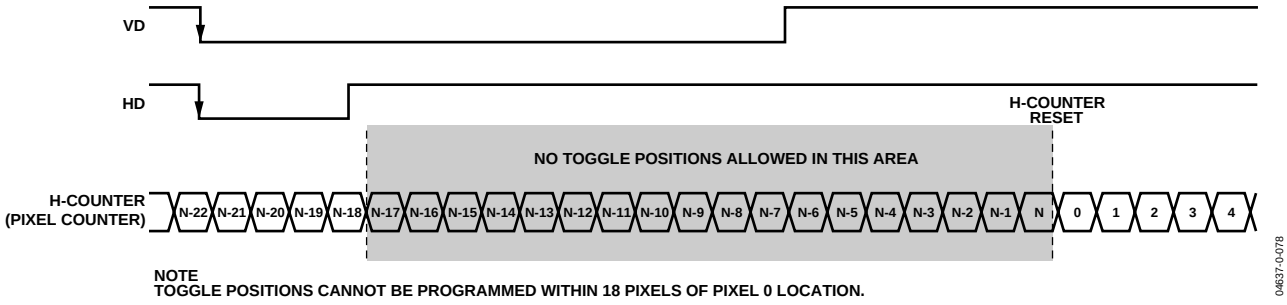


Figure 71. Toggle Position Inhibit Area, Slave Mode

STANDBY MODE OPERATION

The AD9925 contains three different standby modes to optimize the overall power dissipation in a particular application. Bits [1:0] of the OPRMODE register control the power-down state of the device:

OPRMODE[1:0] = 00 = Normal Operation (Full Power)
OPRMODE[1:0] = 01 = Standby 1 Mode
OPRMODE[1:0] = 10 = Standby 2 Mode
OPRMODE[1:0] = 11 = Standby 3 Mode (Lowest Overall Power)

Table 34 and Table 35 summarize the operation of each power-down mode. Note that the OUT_CONTROL register takes priority over the standby 1 and standby 2 modes in determining the digital output states, but the standby 3 mode takes priority over OUT_CONTROL. Standby 3 mode has the lowest power consumption and even shuts down the crystal oscillator circuit between CLI and CLO. Thus, if CLI and CLO are being used with a crystal to generate the master clock, this circuit will be powered down and there will be no clock signal. When returning from standby 3 mode to normal operation, the timing core must be reset at least 500 µs after the OPRMODE register is written to. This will allow sufficient time for the crystal circuit to settle.

The XV and shutter outputs can also be programmed to hold a specific value during any of the standby modes, as detailed in Table 35.

Table 34. Standby Mode Operation

I/O Block	Standby 3 (Default)[1, 2]	OUT_CONT= LO[2]	Standby 2[3, 4]	Standby 1[3, 4]
AFE	Off	No Change	Off	Off
Timing Core	Off	No Change	Off	Off
CLO Oscillator	Off	No Change	On	On
CLO	High	Running	Running	Running
H1	Hi-Z	Low	Low (4.3 mA)	Low (4.3 mA)
H2	Hi-Z	High	High (4.3 mA)	High (4.3 mA)
H3	Hi-Z	Low	Low (4.3 mA)	Low (4.3 mA)
H4	Hi-Z	High	High (4.3 mA)	High (4.3 mA)
RG	Hi-Z	Low	Low (4.3 mA)	Low (4.3 mA)
VD	Low	VDHDPOL Value	VDHDPOL Value	Undefined in Master Mode
HD	Low	VDHDPOL Value	VDHDPOL Value	Undefined in Master Mode
DCLK	Low	Low	Low	Running if DCLK MODE =1
DOUT	Low	Low	Low	Low

[1] To exit standby 3 mode, first write a 00 to OPRMODE[1:0], then reset the timing core after ~500 µs to guarantee proper settling of the oscillator.
[2] Standby 3 mode takes priority over OUT_CONTROL for determining the output polarities.
[3] These polarities assume OUT_CONT = High., because OUT_CONTROL = Low takes priority over standby 1 and standby 2 modes.
[4] Standby 1 and standby 2 modes will set H and RG drive strength to minimum value (4.3 mA).

Table 35. Standby Mode Operation—Vertical and Shutter Outputs (Programmable Polarities Available)

I/O Block	Standby 3 (Default)[1, 2]	OUT_CONT = Low[2, 3]	Standby 2[3]	Standby 1[3]
XV1	Low	Low	Low	Low
XV8	Low	Low	Low	Low
XV3	Low	Low	Low	Low
XV7	Low	Low	Low	Low
XV6	Low	High	High	High
XSG6	Low	High	High	High
XV5	Low	High	High	High
XV4	Low	High	High	High
XSG5	Low	High	High	High
XSG4	Low	High	High	High
XV2	Low	High	High	High
XSG3	Low	High	High	High
XSG1	Low	High	High	High
XSG2	Low	High	High	High
SUBCK	Low	High	High	High
VSUB	Low	Low	Low	Low
MSHUT	Low	Low	Low	Low
STROBE	Low	Low	Low	Low

[1] Polarities for vertical and shutter outputs are programmable for each standby mode, using the STBYPOL registers.
[2] Default register values are:
STBY3POL = Bin 00000000000000000 = 0x00
OCONTPOL = STBY2POL = STBY1POL = Bin 000011111111111000 = 0x3FF8
[3] Bit assignments for programming polarity registers: (MSB) XV1, XV8, XV3, XV7, XV6, XSG6, XV5, XV4, XSG5, XSG4, XV2, XSG3, XSG1, XSG2, SUBCK, VSUB, MSHUT, and STROBE (LSB).

CIRCUIT LAYOUT INFORMATION

The AD9925 typical circuit connections are shown in Figure 73. The PCB layout is critical in achieving good image quality from the AD9925. All of the supply pins, particularly the AVDD, TCVDD, RGVDD, and HVDD supplies, must be decoupled to ground with good quality, high frequency chip capacitors. The decoupling capacitors should be located as close as possible to the supply pins and should have a very low impedance path to a continuous ground plane. There should also be a 4.7 µF or larger value bypass capacitor near each main supply—AVDD, HVDD, DRVDD, VL, and VH—although this is not necessary for each individual pin. In most applications, it is easier to share the supply for RGVDD and HVDD, which may be done as long as the individual supply pins are separately bypassed. A separate 3 V supply may also be used for DRVDD, but this supply pin should still be decoupled to the same ground plane as the rest of the chip. A separate ground for DRVSS is not recommended.

The analog bypass pins (REFT and REFB) should also be carefully decoupled to ground as close as possible to their respective pins. The analog input (CCDIN) capacitor should also be located close to the pin.

The H1 to H4 and RG traces should be designed to have low inductance to avoid excessive distortion of the signals. Heavier traces are recommended because of the large transient current demand on H1 to H4 by the CCD. If possible, physically locating the AD9925 closer to the CCD will reduce the inductance on these lines. As always, the routing path should be as direct as possible from the AD9925 to the CCD.

The AD9925 also contains an on-chip oscillator for driving an external crystal. Figure 72 shows an example of an application using a typical 24 MHz crystal. For the exact values of the external resistors and capacitors, it is best to consult with the crystal manufacturer's data sheet.

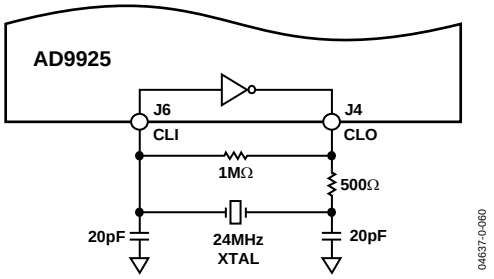


Figure 72. Crystal Driver Application

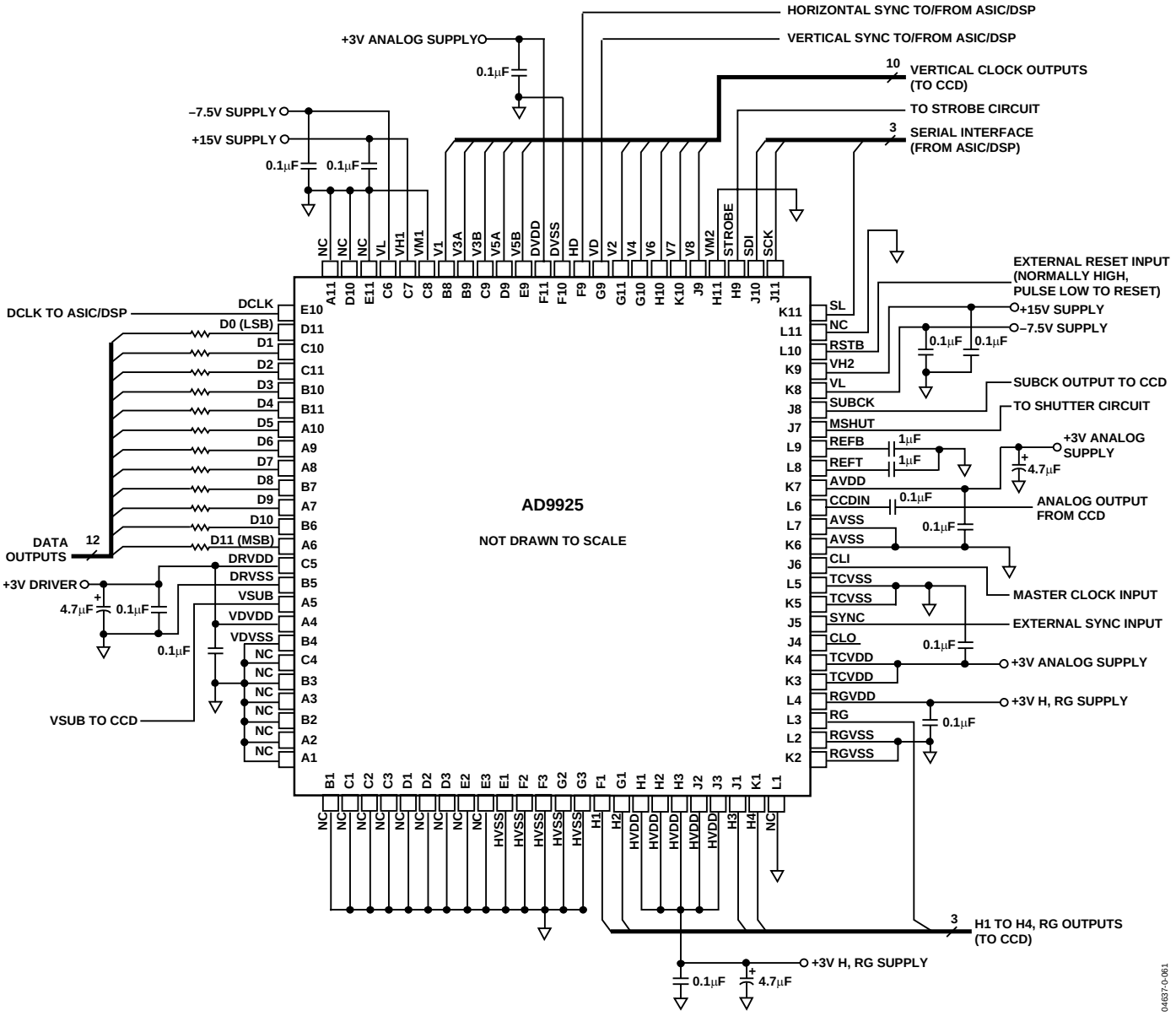


Figure 73. AD9925 Typical Circuit Configuration

SERIAL INTERFACE TIMING

All of the internal registers of the AD9925 are accessed through a 3-wire serial interface. Each register consists of an 8-bit address and a 24-bit data-word. Both the 8-bit address and 24-bit data-word are written starting with the LSB. To write to each register, a 32-bit operation is required, as shown in Figure 74. Although many registers are fewer than 24 bits wide, all 24 bits must be written for each register. For example, if the register is only 10 bits wide, then the upper 14 bits are Don't Cares and may be filled with 0s during the serial write operation. If fewer than 24 bits are written, the register will not be updated with new data.

Figure 75 shows a more efficient way to write to the registers, using the AD9925's address automatic increment capability. Using this method, the lowest desired address is written first, followed by multiple 24-bit data-words. Each new 24-bit data-word will automatically be written to the next highest register address. By eliminating the need to write each 8-bit address, faster register loading is achieved. Continuous write operations may be used starting with any register location and may be used to write to as few as two registers or to as many as the entire register space.

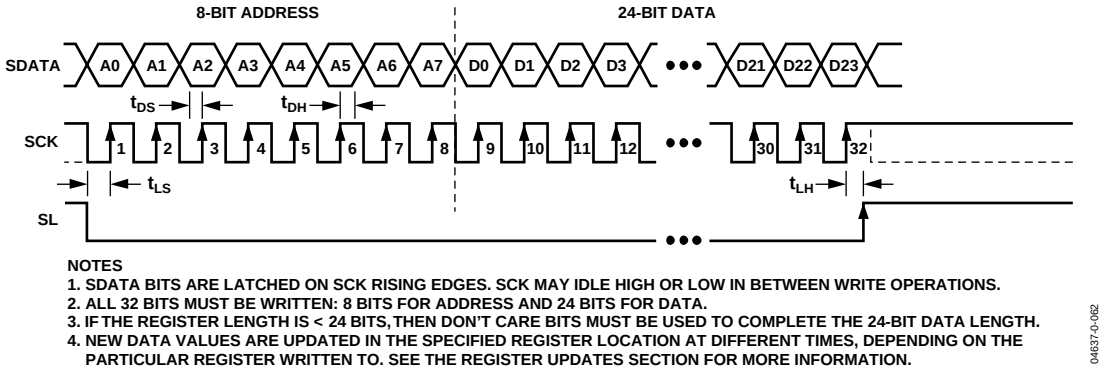


Figure 74. Serial Write Operation

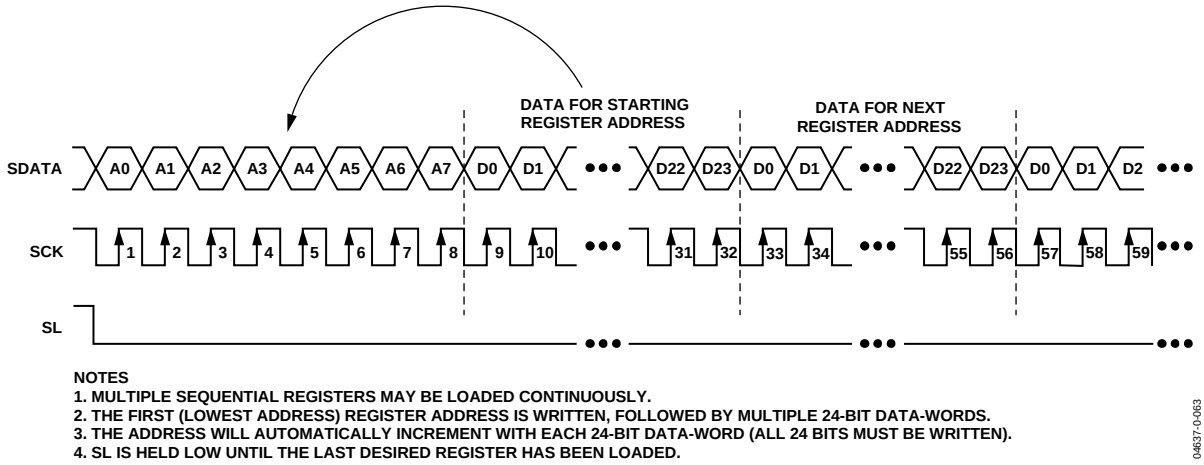


Figure 75. Continuous Serial Write Operation

Register Address BANK 1, BANK 2, and BANK 3

The AD9925 address space is divided into three different register banks, referred to as Register Bank 1, Register Bank 2, and Register Bank 3. Figure 76 illustrates how the three banks are divided. Register Bank 1 and Bank 2 are backward compatible with the AD9995 registers. Register Bank 1 contains the registers for the AFE, miscellaneous functions, VD/HD parameters, timing core, CLPOB masking, VSG patterns, and shutter functions. Register Bank 2 contains all of the information for the vertical pattern groups, vertical sequences, and field information.

Register Bank 3 contains new registers for accessing the XV7 and XV8 functionality. These additional outputs allow the AD9925 to support newer CCDs that require 8-phases of vertical clocking.

When writing to the AD9925, Addr 0x7F is used to specify which address bank is being written to. To write to Bank 1, a data value of 0 is written. To write to Bank 2, a data value of 1 is written. To write to Bank 3, a data value of 2 is written.

Note that Register Bank 1 contains many unused addresses. Undefined addresses between Addr 0x00 and Addr 0x7F are considered Don't Cares, and it is acceptable if these addresses are filled in with all 0s during a continuous register write operation. However, the undefined addresses above 0x7F must not be written to, or the AD9925 may not operate properly. The exceptions are the FG_TRIG registers 0xE7, 0xEB, and 0xF2 through 0xF6, which may be written as specified on Page 43.

Default values for Register Bank 2 and Bank 3 are undefined after power-up. Appropriate values should be written into these register banks to ensure proper operation. In applications where the XV7 and XV8 signals are not used, the Bank 3 registers should still be programmed with known values to prevent unpredictable behavior in the V-driver circuit.

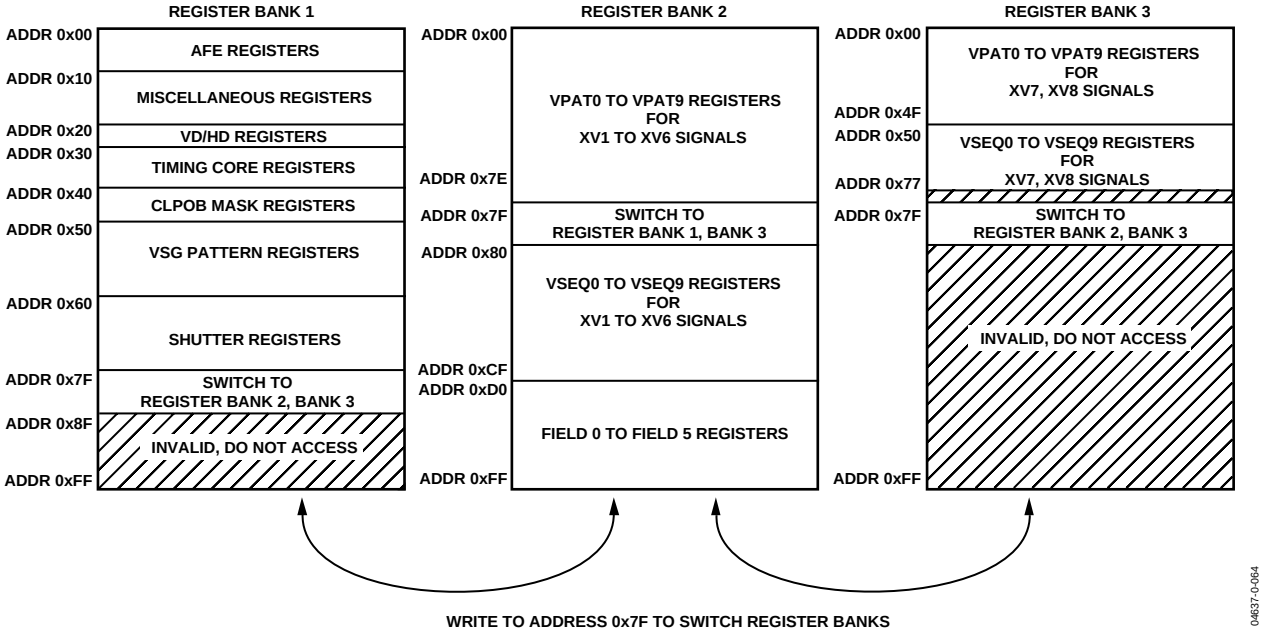


Figure 76. Layout of Internal Register Bank 1, Bank 2, and Bank 3

Updating New Register Values

The AD9925's internal registers are updated at different times, depending on the particular register. Table 36 summarizes the four different types of register updates:

1. **SCK Updated**: Some of the registers in Bank 1 are updated as soon as the 24th data bit (D23) is written. These registers, shaded in gray in the Bank 1 register list, are used for functions that do not require gating with the next VD boundary, such as power-up and reset functions. The bank select register (Addr 0x7F in Bank 1 and Bank 2) is also SCK updated.

2. **VD Updated**: Most of the registers in Bank 1, as well as the field registers in Bank 2, are updated at the next VD falling edge. By updating these values at the next VD edge, the current field will not be corrupted, and the new register values will be applied to the next field. Bank 1 register updates may be further delayed past the VD falling edge by using the UPDATE register (Addr 0x19). This will delay VD updates to any HD line in the field. Note that the Bank 2 field registers are not affected by the UPDATE register.

3. **SG Line Updated**: A few of the registers in Bank 1 are updated at the end of the SG active line, at the HD falling edge. These registers control the SUBCK signal, so that the SUBCK output will not update until after the SG line has been completed. These registers are crosshatched in the Bank 1 register list.

4. **SCP Updated**: In Bank 2 and Bank 3, all of the vertical pattern group and vertical sequence registers (Addr 0x00 through Addr 0xCF, excluding Addr 0×7F) are updated at the next SCP, where they will be used. For example, in Figure 77, this field has selected Region 1 to use Vertical Sequence 3 for the vertical outputs. This means that a write to any of the Vertical Sequence 3 registers, or any of the vertical pattern group registers that are referenced by Vertical Sequence 3, will be updated at SCP1. If multiple writes are done to the same register, the last one done before SCP1 will be the one that is updated. Likewise, register writes to any Vertical Sequence 5 registers will be updated at SCP2, and register writes to any Vertical Sequence 8 registers will be updated at SCP3.

Table 36. Register Update Locations

Update Type	Register Bank	Description
SCK Updated	Bank 1 Only	Register is immediately updated when the 24th data bit (D23) is clocked in.
VD Updated	Bank 1, Bank 2	Register is updated at the VD falling edge. VD updated registers in Bank 1 may be delayed further by using the UPDATE register at Addr 0x19 in Bank 1. Bank 2 updates will not be affected by the UPDATE register.
SG Line Updated	Bank 1 Only	Register is updated at the HD falling edge at the end of the SG active line.
SCP Updated	Bank 2, Bank 3	Register is updated at the next SCP when the register will be used.

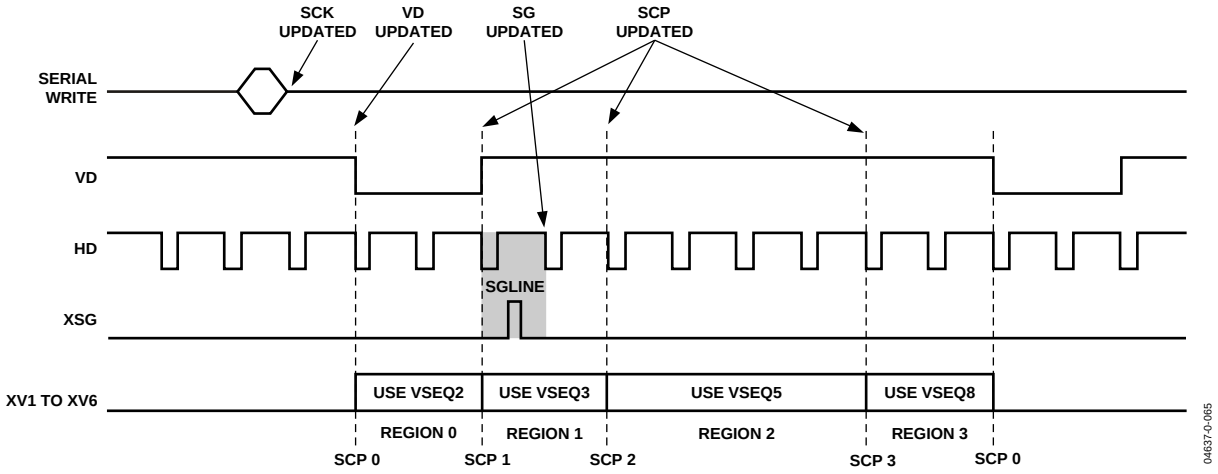


Figure 77. Register Update Locations (See Table 40 for Definitions)

COMPLETE LISTING FOR REGISTER BANK 1

All registers are VD updated, except where noted. Light gray cells = SCK updated, and dark gray cells = SG line updated.

Table 37. AFE Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
00	[11:0]	7	OPRMODE	AFE Operation Modes (See Table 45 for detail)
01	[9:0]	0	VGAGAIN	VGA Gain
02	[7:0]	80	CLAMPLEVEL	Optical Black Clamp Leve
03	[11:0]	4	CTLMODE	AFE Control Modes (See Table 46 for detail)

Table 38. Miscellaneous Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
0A	[17:0]	3FF8	STBY1POL	Polarities for Output Signals during Standby 1 Mode.
0B	[17:0]	3FF8	STBY2POL	Polarities for Output Signals during Standby 2 Mode.
0C	[17:0]	0	STBY3POL	Polarities for Output Signals during Standby 3 Mode.
0D	[17:0]	3FF8	OCONTPOL	Polarities for Output Signals When OUTCONTROL = 0.
10	[0]	0	SW_RST	Software Reset. 1: Reset all registers to default, then self clear back to 0.
11	[0]	0	OUTCONTROL	Output Control. 0: Make all outputs dc inactive.
12	[0]	1	SYNCENABLE	Configures Pin 52 as a SYNC Input (= 1) or CLPOB/PBLK Output (= 0).
13	[0]	0	SYNCPOL	SYNC Active Polarity (0: Active Low).
14	[0]	0	SYNCSUSPEND	Suspend Clocks during SYNC Active (1: Suspend).
15	[0]	0	TGCORE_RSTB	Timing Core Reset Bar. 0: Reset TG Core, 1: Resume Operation.
16	[0]	1	OSC_PWRDOWN	CLO Oscillator Power-Down (0: Oscillator Is Powered Down).
17			UNUSED	Set to 0.
18	[0]	0	TEST	Internal Use Only. Must be set to 0.
19	[11:0]	0	UPDATE	Serial Update. Line (HD) in the field to update VD updated registers.
1A	[0]	0	PREVENTUP-DATE	Prevents the update of the VD updated registers. 1: Prevent Update.
1B	[23:0]	0	MODE	MODE Register.
1C			UNUSED	Set to 0.
1D	[0]	0	OUTPUTPBLK	Assigns Output for Pin 52 When Configured as Output. 0: CLPOB, 1: PBLK.
1E	[0]	0	DVCMODE	1: Enable DVC Mode. VD counter will reset every 2 fields, instead of every field. VDLEN register should be programmed to the total number of lines contained in 2 fields, e.g., VDLEN = 525 lines will results in 262.5 lines in each field.
1F	[0]	0	INVERT_DCLK	1: Invert the DCLK Output.
E7	[2:0] [3] [5:4] [6] [7] [8]	0	SHUT_EXTRA	Set to 0. Selects FG_TRIG Signal to VSUB Pin (See Page 43). Set to 0. H3HBLKOFF, Set to 1 to Enable H3/H4 Outputs during HBLK (See Page 19). Set to 0. Combines FG_TRIG and VSUB Signals (See Page 43).
EB	[3:0]	0	FG_TRIGEN	FG_TRIG Signal Enable (See Page 43).
F2	[0]	0	FG_TRIGPOL	FG_TRIG Start Polarity.
F3	[11:0]	0	FG_TRIGLIN1	FG_TRIG First Toggle Position, Line Location.
F4	[12:0]	0	FG_TRIGPIX1	FG_TRIG First Toggle Position, Pixel Location.
F5	[11:0]	0	FG_TRIGLIN2	FG_TRIG Second Toggle Position, Line Location.
F6	[12:0]	0	FG_TRIGPIX2	FG_TRIG Second Toggle Position, Pixel Location.

Table 39. VD/HD Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
20	[0]	0	MASTER	VD/HD Master or Slave Timing (0 = Slave Mode).
21	[0]	0	VDHDPOL	VD/HD Active Polarity. 0 = Low and 1 = High.
22	[11:0] [17:12]	0 0	HDRISE VDRISE	Rising Edge Location for HD. Rising Edge Location for VD.
23	[11:0]	0	SCP0	SCP0. Used for All Fields.

Table 40. Timing Core Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
30	[0]	0	CLIDIVIDE	Divide CLI Input Clock by 2. 1 = Divide by 2.
31	[0] [6:1] [12:7]	1 0 20	H1POL H1POSLOC H1NEGLOC	H1 Polarity. 0: Inversion, 1: No Inversion. H1 Positive Edge Location. H1 Negative Edge Location.
32	[0] [6:1] [12:7]	1 0 20	H3POL H3POSLOC H3NEGLOC	H3 Polarity. 0: Inversion, 1: No Inversion. H3 Positive Edge Location. H3 Negative Edge Location.
33	[0] [6:1] [12:7]	1 0 20	RGPOL RGPOSLOC RGNEGLOC	RG Polarity. 0: Inversion, 1: No Inversion. RG Positive Edge Location. RG Negative Edge Location.
34	[0] [1]	0 0	H1RETIME H3RETIME	Retime H1/H3 HBLK to Internal H1/H3 Clocks. Preferred setting is 1 for each bit, which adds one cycle of delay to the programmed HBLK toggle positions.
35	[2:0] [5:3] [8:6] [11:9] [14:12]	1 1 1 1 1	H1DRV H2DRV H3DRV H4DRV RGDRV	Drive Strength Control for H1. 0: Off. 1: 4.3 mA. 2: 8.6 mA. 3: 12.9 mA. 4: 17.2 mA. 5: 21.5 mA. 6: 25.8 mA. 7: 30.1 mA. Drive Strength Control for H2 (Same Values as H1DRV). Drive Strength Control for H3 (Same Values as H1DRV). Drive Strength Control for H4 (Same Values as H1DRV). Drive Strength Control for RG (Same Values as H1DRV).
36	[5:0] [11:6]	24 0	SHPLOC SHDLOC	SHP Sampling Location. SHD Sampling Location.
37	[5:0] [6] [8:7]	0 0 2	DOUTPHASE DCLKMODE DOUTDLY	DOUT Phase Control. 0: DCLK Tracks DOUTPHASE. 1: DCLK Does Not Track DOUTPHASE, Remains Fixed with Regards to CLI Data Output Delay (t_{OD}) with Respect to DCLK. 0: No Delay, 1: ~4 ns, 2: ~8 ns, and 3: ~12 ns.
38	[2:0]	0	HBLKWIDTH	Controls HBLK Width as a Fraction of H1 to H4 Frequency. 0: same, 1: 1/2, 2: 1/4, 3: 1/6, 4: 1/8, 5: 1/10, 6: 1/12, and 7: 1/14.

Table 41. CLPOB Masking Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
40	[11:0] [23:12]	FFF FFF	CLPMASK0 CLPMASK1	CLPOB Line Masking Line No. 0, or Mask0 Range, Start Line CLPOB Line Masking Line No. 1, or Mask0 Range, End Line
41	[11:0] [23:12]	FFF FFF	CLPMASK2 CLPMASK3	CLPOB Line Masking Line No. 2, or Mask1 Range, Start Line CLPOB Line Masking Line No. 3, or Mask1 Range, End Line
42	[11:0]	FFF	CLPMASK4	CLPOB Line Masking Line No. 4, or Mask2 Range, Start Line
43	[11:0] [12]	FFF 0	CLPMASK5 CLPMASKTYPE	CLPOB Line Masking Line No. 5, or Mask2 Range, End Line 0: CLPOB Line Masking, 1: Enable CLPOB Range Masking

Table 42. SG Pattern Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
50	[0]	1	SGPOL_0	Start Polarity for SG Pattern No. 0.
	[1]	1	SGPOL_1	Start Polarity for SG Pattern No. 1.
	[2]	1	SGPOL_2	Start Polarity for SG Pattern No. 2.
	[3]	1	SGPOL_3	Start Polarity for SG Pattern No. 3.
51	[11:0]	FFF	SGTOG1_0	Pattern No. 0 Toggle Position 1.
	[23:12]	FFF	SGTOG2_0	Pattern No. 0 Toggle Position 2.
52	[11:0]	FFF	SGTOG1_1	Pattern No. 1 Toggle Position 1.
	[23:12]	FFF	SGTOG2_1	Pattern No. 1 Toggle Position 2.
53	[11:0]	FFF	SGTOG1_2	Pattern No. 2 Toggle Position 1.
	[23:12]	FFF	SGTOG2_2	Pattern No. 2 Toggle Position 2.
54	[11:0]	FFF	SGTOG1_3	Pattern No. 3 Toggle Position 1.
	[23:12]	FFF	SGTOG2_3	Pattern No. 3 Toggle Position 2.
55	[5:0]	0	SGMASK_OVR	SGMASK Override. These values will immediately override the SG masking values located in the field registers.
	[6]	0	SGMASKOVR_EN	0: Use SG Masking in Field Registers, 1: Enable SGMASK Override.

Table 43. Shutter Control Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
60	[4:0]	0	TRIGGER	Trigger for VSUB [0], MSHUT [1], STROBE [2], Exposure [3], and Readout [4]. Note that to trigger the readout to automatically occur after the exposure period, both exposure and readout should be triggered together.
61	[2:0]	2	READOUT	Number of Fields to Suppress the SUBCK Pulses after the VSG Line.
62	[11:0]	0	EXPOSURE	Number of Fields to Suppress the SUBCK and VSG Pulses.
	[12]	0	VDHDOFF	Set = 1 to disable the VD/HD outputs during exposure (when >1 field).
63	[11:0]	0	SUBCKSUPPRESS	Number of SUBCK Pulses to Suppress after VSG Line.
	[23:12]	0	SUBCKNUM	Number of SUBCK Pulses per Field.
64	[0]	1	SUBCKPOL	SUBCK Pulse Start Polarity.
65	[11:0]	FFF	SUBCK1TOG1	First SUBCK Pulse. Toggle Position 1.
	[23:12]	FFF	SUBCK1TOG2	First SUBCK Pulse. Toggle Position 2.
66	[11:0]	FFF	SUBCK2TOG1	Second SUBCK Pulse. Toggle Position 1.
	[23:12]	FFF	SUBCK2TOG2	Second SUBCK Pulse. Toggle Position 2.
67	[0]	0	VSUBMODE	VSUB Readout Mode. 0: Mode 0, 1: Mode 1.
	[1]	0	VSUBKEEPON	0: Turn Off VSUB after Readout, 1: Keep VSUB On after Readout.
68	[11:0]	0	VSUBON	VSUB Online Position.
	[12]	1	VSUBPOL	VSUB Active Polarity.
69	[0]	1	MSHUTPOL	MSHUT Active Polarity.
	[1]	0	MSHUTON	MSHUT Manual Enable (Opens Shutter at Next VD Edge).
6A	[11:0]	0	MSHUTON_LN	MSHUT On Position—Line.
	[23:12]	0	MSHUTON_PX	MSHUT On Position—Pixel.
6B	[11:0]	0	MSHUTOFF_FD	MSHUT Off Position—Field.
6C	[11:0]	0	MSHUTOFF_LN	MSHUT Off Position—Line.
	[23:12]	0	MSHUTOFF_PX	MSHUT Off Position—Pixel.
6D	[0]	1	STROBPOL	STROBE Active Polarity.
6E	[11:0]	0	STROBON_FD	STROBE On Position—Field.
6F	[11:0]	0	STROBON_LN	STROBE On Position—Line.
	[23:12]	0	STROBON_PX	STROBE On Position—Pixel.
70	[11:0]	0	STROBOFF_FD	STROBE Off Position—Field.
71	[11:0]	0	STROBOFF_LN	STROBE Off Position—Line.
	[23:12]	0	STROBOFF_PX	STROBE Off Position—Pixel.
72	[3:0]	0	SUBCKTOG13	13th Bit for SUBCK Toggle Position Placement.

Table 44. Register Map Selection

Address	Data Bit Content	Default Value	Register Name	Register Description
7F	[1:0]	0	BANKSELECT	Register Bank Access for Bank 1, Bank 2, and Bank 3. 0: Bank 1, 1: Bank 2, 2: Bank 3, and 3: Bank 1.

Table 45. AFE Operation Register Detail

Address	Data Bit Content	Default Value	Name	Description
00	[1:0]	3	PWRDOWN	0: Normal Operation, 1: Standby 1, 2: Standby 2, 3: Standby 3.
	[2]	1	CLPENABLE	0: Disable OB Clamp, 1: Enable OB Clamp.
	[3]	0	CLPSPEED	0: Select Normal OB Clamp Settling, 1: Select Fast OB Clamp Settling.
	[4]	0	FASTUPDATE	1: Select Temporary Fast Clamping When VGA Gain Is Updated.
	[5]	0	PBLK_LVL	DOUT Value during PBLK: 0: Blank to 0, 1: Blank to Clamp Level.
	[7:6]	0	TEST	Test Operation Only. Set to 0.
	[8]	0	DCBYP	0: Enable DC Restore Circuit, 1: Bypass DC Restore Circuit during PBLK.
	[9]	0	TEST	Test Use Only. Set to 0.
	[11:10]	0	CDSGAIN	0: 0 dB, 1: 2 dB, 2: 4 dB, and 3: 0 dB.

Table 46. AFE Control Register Detail

Address	Data Bit Content	Default Value	Name	Description
03	[1:0]	0	TEST	Test Use Only. Set to 0.
	[2]	1	TEST	Test Use Only. Recommended setting is 0.
	[3]	0	DOUTDISABLE	0 = Data Outputs Are Driven, 1 = Data Outputs Are Three-Stated.
	[4]	0	DOUTLATCH	0 = Latch Data Outputs with DOUT Phase, 1 = Output Latch Transparent.
	[5]	0	GRAYENCODE	0 = Binary Encode Data Outputs, 1 = Gray Encode Data Outputs.

COMPLETE LISTING FOR REGISTER BANK 2

All vertical pattern group and vertical sequence registers are SCP updated, and all field registers are VD updated. Default register values are undefined.

Table 47. Vertical Pattern Group 0 (VPAT0) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
00	[5:0] [11:6] [23:12]	X X X	VPOL_0 UNUSED VPATLEN_0	VPAT0 Start Polarity. XV1[0], XV2[1], XV3[2], XV4[3], XV5[4], XV6[5]. Unused. Total Length of VPAT0. Note: If using VPAT0 as a second vertical sequence in the VSG active line, this value is the start position for the second vertical sequence.
01	[11:0] [23:12]	X X	XV1TOG1_0 XV1TOG2_0	XV1 Toggle Position 1. XV1 Toggle Position 2.
02	[11:0] [23:12]	X X	XV1TOG3_0 XV2TOG1_0	XV1 Toggle Position 3. XV2 Toggle Position 1.
03	[11:0] [23:12]	X X	XV2TOG2_0 XV2TOG3_0	XV2 Toggle Position 2. XV2 Toggle Position 3.
04	[11:0] [23:12]	X X	XV3TOG1_0 XV3TOG2_0	XV3 Toggle Position 1. XV3 Toggle Position 2.
05	[11:0] [23:12]	X X	XV3TOG3_0 XV4TOG1_0	XV3 Toggle Position 3. XV4 Toggle Position 1.
06	[11:0] [23:12]	X X	XV4TOG2_0 XV4TOG3_0	XV4 Toggle Position 2. XV4 Toggle Position 3.
07	[11:0] [23:12]	X X	XV5TOG1_0 XV5TOG2_0	XV5 Toggle Position 1. XV5 Toggle Position 2.
08	[11:0] [23:12]	X X	XV5TOG3_0 XV6TOG1_0	XV5 Toggle Position 3. XV6 Toggle Position 1.
09	[11:0] [23:12]	X X	XV6TOG2_0 XV6TOG3_0	XV6 Toggle Position 2. XV6 Toggle Position 3.
0A	[11:0] [23:12]	X X	FREEZE1_0 RESUME1_0	XV1 to XV6 Freeze Position 1. XV1 to XV6 Resume Position 1.
0B	[11:0] [23:12]	X X	FREEZE2_0 RESUME2_0	XV1 to XV6 Freeze Position 2. XV1 to XV6 Resume Position 2.

Table 48. Vertical Pattern Group 1 (VPAT1) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
0C	[5:0]	X	VPOL_1	VPAT1 Start Polarity. XV1[0], XV2[1], XV3[2], XV4[3], XV5[4], XV6[5].
	[11:6]	X	UNUSED	Unused.
	[23:12]	X	VPATLEN_1	Total Length of VPAT1. Note: If using VPAT1 as a second vertical sequence in the VSG active line, this value is the start position for the second vertical sequence.
0D	[11:0]	X	XV1TOG1_1	XV1 Toggle Position 1.
	[23:12]	X	XV1TOG2_1	XV1 Toggle Position 2.
0E	[11:0]	X	XV1TOG3_1	XV1 Toggle Position 3.
	[23:12]	X	XV2TOG1_1	XV2 Toggle Position 1.
0F	[11:0]	X	XV2TOG2_1	XV2 Toggle Position 2.
	[23:12]	X	XV2TOG3_1	XV2 Toggle Position 3.
10	[11:0]	X	XV3TOG1_1	XV3 Toggle Position 1.
	[23:12]	X	XV3TOG2_1	XV3 Toggle Position 2.
11	[11:0]	X	XV3TOG3_1	XV3 Toggle Position 3.
	[23:12]	X	XV4TOG1_1	XV4 Toggle Position 1.
12	[11:0]	X	XV4TOG2_1	XV4 Toggle Position 2.
	[23:12]	X	XV4TOG3_1	XV4 Toggle Position 3.
13	[11:0]	X	XV5TOG1_1	XV5 Toggle Position 1.
	[23:12]	X	XV5TOG2_1	XV5 Toggle Position 2.
14	[11:0]	X	XV5TOG3_1	XV5 Toggle Position 3.
	[23:12]	X	XV6TOG1_1	XV6 Toggle Position 1.
15	[11:0]	X	XV6TOG2_1	XV6 Toggle Position 2.
	[23:12]	X	XV6TOG3_1	XV6 Toggle Position 3.
16	[11:0]	X	FREEZE1_1	XV1 to XV6 Freeze Position 1.
	[23:12]	X	RESUME1_1	XV1 to XV6 Resume Position 1.
17	[11:0]	X	FREEZE2_1	XV1 to XV6 Freeze Position 2.
	[23:12]	X	RESUME2_1	XV1 to XV6 Resume Position 2.

Table 49. Vertical Pattern Group 2 (VPAT2) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
18	[5:0] [11:6] [23:12]	X X X	VPOL_2 UNUSED VPATLEN_2	VPAT2 Start Polarity. XV1[0], XV2[1], XV3[2], XV4[3], XV5[4], XV6[5]. Unused. Total Length of VPAT2. Note: If using VPAT2 as a second vertical sequence in the VSG active line, this value is the start position for second vertical sequence.
19	[11:0] [23:12]	X X	XV1TOG1_2 XV1TOG2_2	XV1 Toggle Position 1. XV1 Toggle Position 2.
1A	[11:0] [23:12]	X X	XV1TOG3_2 XV2TOG1_2	XV1 Toggle Position 3. XV2 Toggle Position 1.
1B	[11:0] [23:12]	X X	XV2TOG2_2 XV2TOG3_2	XV2 Toggle Position 2. XV2 Toggle Position 3.
1C	[11:0] [23:12]	X X	XV3TOG1_2 XV3TOG2_2	XV3 Toggle Position 1. XV3 Toggle Position 2.
1D	[11:0] [23:12]	X X	XV3TOG3_2 XV4TOG1_2	XV3 Toggle Position 3. XV4 Toggle Position 1.
1E	[11:0] [23:12]	X X	XV4TOG2_2 XV4TOG3_2	XV4 Toggle Position 2. XV4 Toggle Position 3.
1F	[11:0] [23:12]	X X	XV5TOG1_2 XV5TOG2_2	XV5 Toggle Position 1. XV5 Toggle Position 2.
20	[11:0] [23:12]	X X	XV5TOG3_2 XV6TOG1_2	XV5 Toggle Position 3. XV6 Toggle Position 1.
21	[11:0] [23:12]	X X	XV6TOG2_2 XV6TOG3_2	XV6 Toggle Position 2. XV6 Toggle Position 3.
22	[11:0] [23:12]	X X	FREEZE1_2 RESUME1_2	XV1 to XV6 Freeze Position 1. XV1 to XV6 Resume Position 1.
23	[11:0] [23:12]	X X	FREEZE2_2 RESUME2_2	XV1 to XV6 Freeze Position 2. XV1 to XV6 Resume Position 2.

Table 50. Vertical Pattern Group 3 (VPAT3) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
24	[5:0] [11:6] [23:12]	X X X	VPOL_3 UNUSED VPATLEN_3	VPAT3 Start Polarity. XV1[0], XV2[1], XV3[2], XV4[3], XV5[4], XV6[5]. Unused. Total Length of VPAT3. Note: If using VPAT3 as a second vertical sequence in the VSG active line, this value is the start position for the second vertical sequence.
25	[11:0] [23:12]	X X	XV1TOG1_3 XV1TOG2_3	XV1 Toggle Position 1. XV1 Toggle Position 2.
26	[11:0] [23:12]	X X	XV1TOG3_3 XV2TOG1_3	XV1 Toggle Position 3. XV2 Toggle Position 1.
27	[11:0] [23:12]	X X	XV2TOG2_3 XV2TOG3_3	XV2 Toggle Position 2. XV2 Toggle Position 3.
28	[11:0] [23:12]	X X	XV3TOG1_3 XV3TOG2_3	XV3 Toggle Position 1. XV3 Toggle Position 2.
29	[11:0] [23:12]	X X	XV3TOG3_3 XV4TOG1_3	XV3 Toggle Position 3. XV4 Toggle Position 1.
2A	[11:0] [23:12]	X X	XV4TOG2_3 XV4TOG3_3	XV4 Toggle Position 2. XV4 Toggle Position 3.
2B	[11:0] [23:12]	X X	XV5TOG1_3 XV5TOG2_3	XV5 Toggle Position 1. XV5 Toggle Position 2.
2C	[11:0] [23:12]	X X	XV5TOG3_3 XV6TOG1_3	XV5 Toggle Position 3. XV6 Toggle Position 1.
2D	[11:0] [23:12]	X X	XV6TOG2_3 XV6TOG3_3	XV6 Toggle Position 2. XV6 Toggle Position 3.
2E	[11:0] [23:12]	X X	FREEZE1_3 RESUME1_3	XV1 to XV6 Freeze Position 1. XV1 to XV6 Resume Position 1.
2F	[11:0] [23:12]	X X	FREEZE2_3 RESUME2_3	XV1 to XV6 Freeze Position 2. XV1 to XV6 Resume Position 2.

Table 51. Vertical Pattern Group 4 (VPAT4) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
30	[5:0] [11:6] [23:12]	X X X	VPOL_4 UNUSED VPATLEN_4	VPAT4 Start Polarity. XV1[0], XV2[1], XV3[2], XV4[3], XV5[4], XV6[5]. Unused . Total Length of VPAT4. Note: If using VPAT4 as a second vertical sequence in the VSG active line, this value is the start position for the second vertical sequence.
31	[11:0] [23:12]	X X	XV1TOG1_4 XV1TOG2_4	XV1 Toggle Position 1. XV1 Toggle Position 2.
32	[11:0] [23:12]	X X	XV1TOG3_4 XV2TOG1_4	XV1 Toggle Position 3. XV2 Toggle Position 1.
33	[11:0] [23:12]	X X	XV2TOG2_4 XV2TOG3_4	XV2 Toggle Position 2. XV2 Toggle Position 3.
34	[11:0] [23:12]	X X	XV3TOG1_4 XV3TOG2_4	XV3 Toggle Position 1. XV3 Toggle Position 2.
35	[11:0] [23:12]	X X	XV3TOG3_4 XV4TOG1_4	XV3 Toggle Position 3. XV4 Toggle Position 1.
36	[11:0] [23:12]	X X	XV4TOG2_4 XV4TOG3_4	XV4 Toggle Position 2. XV4 Toggle Position 3.
37	[11:0] [23:12]	X X	XV5TOG1_4 XV5TOG2_4	XV5 Toggle Position 1. XV5 Toggle Position 2.
38	[11:0] [23:12]	X X	XV5TOG3_4 XV6TOG1_4	XV5 Toggle Position 3. XV6 Toggle Position 1.
39	[11:0] [23:12]	X X	XV6TOG2_4 XV6TOG3_4	XV6 Toggle Position 2. XV6 Toggle Position 3.
3A	[11:0] [23:12]	X X	FREEZE1_4 RESUME1_4	XV1 to XV6 Freeze Position 1. XV1 to XV6 Resume Position 1.
3B	[11:0] [23:12]	X X	FREEZE2_4 RESUME2_4	XV1 to XV6 Freeze Position 2. XV1 to XV6 Resume Position 2.

Table 52. Vertical Pattern Group 5 (VPAT5) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
3C	[5:0]	X	VPOL_5	VPAT5 Start Polarity. XV1[0], XV2[1], XV3[2], XV4[3], XV5[4], XV6[5].
	[11:6]	X	UNUSED	Unused.
	[23:12]	X	VPATLEN_5	Total Length of VPAT5. Note: If using VPAT5 as a second vertical sequence in the VSG active line, this value is the start position for the second vertical sequence.
3D	[11:0]	X	XV1TOG1_5	XV1 Toggle Position 1.
	[23:12]	X	XV1TOG2_5	XV1 Toggle Position 2.
3E	[11:0]	X	XV1TOG3_5	XV1 Toggle Position 3.
	[23:12]	X	XV2TOG1_5	XV2 Toggle Position 1.
3F	[11:0]	X	XV2TOG2_5	XV2 Toggle Position 2.
	[23:12]	X	XV2TOG3_5	XV2 Toggle Position 3.
40	[11:0]	X	XV3TOG1_5	XV3 Toggle Position 1.
	[23:12]	X	XV3TOG2_5	XV3 Toggle Position 2.
41	[11:0]	X	XV3TOG3_5	XV3 Toggle Position 3.
	[23:12]	X	XV4TOG1_5	XV4 Toggle Position 1.
42	[11:0]	X	XV4TOG2_5	XV4 Toggle Position 2.
	[23:12]	X	XV4TOG3_5	XV4 Toggle Position 3.
43	[11:0]	X	XV5TOG1_5	XV5 Toggle Position 1.
	[23:12]	X	XV5TOG2_5	XV5 Toggle Position 2.
44	[11:0]	X	XV5TOG3_5	XV5 Toggle Position 3.
	[23:12]	X	XV6TOG1_5	XV6 Toggle Position 1.
45	[11:0]	X	XV6TOG2_5	XV6 Toggle Position 2.
	[23:12]	X	XV6TOG3_5	XV6 Toggle Position 3.
46	[11:0]	X	FREEZE1_5	XV1 to XV6 Freeze Position 1.
	[23:12]	X	RESUME1_5	XV1 to XV6 Resume Position 1.
47	[11:0]	X	FREEZE2_5	XV1 to XV6 Freeze Position 2.
	[23:12]	X	RESUME2_5	XV1 to XV6 Resume Position 2.

Table 53. Vertical Pattern Group 6 (VPAT6) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
48	[5:0] [11:6] [23:12]	X X X	VPOL_6 UNUSED VPATLEN_6	VPAT6 Start Polarity. XV1[0], XV2[1], XV3[2], XV4[3], XV5[4], XV6[5]. Unused. Total Length of VPAT6. Note: If using VPAT6 as a second vertical sequence in the VSG Active line, this value is the start position for the second vertical sequence.
49	[11:0] [23:12]	X X	XV1TOG1_6 XV1TOG2_6	XV1 Toggle Position 1. XV1 Toggle Position 2.
4A	[11:0] [23:12]	X X	XV1TOG3_6 XV2TOG1_6	XV1 Toggle Position 3. XV2 Toggle Position 1.
4B	[11:0] [23:12]	X X	XV2TOG2_6 XV2TOG3_6	XV2 Toggle Position 2. XV2 Toggle Position 3.
4C	[11:0] [23:12]	X X	XV3TOG1_6 XV3TOG2_6	XV3 Toggle Position 1. XV3 Toggle Position 2.
4D	[11:0] [23:12]	X X	XV3TOG3_6 XV4TOG1_6	XV3 Toggle Position 3. XV4 Toggle Position 1.
4E	[11:0] [23:12]	X X	XV4TOG2_6 XV4TOG3_6	XV4 Toggle Position 2. XV4 Toggle Position 3.
4F	[11:0] [23:12]	X X	XV5TOG1_6 XV5TOG2_6	XV5 Toggle Position 1. XV5 Toggle Position 2.
50	[11:0] [23:12]	X X	XV5TOG3_6 XV6TOG1_6	XV5 Toggle Position 3. XV6 Toggle Position 1.
51	[11:0] [23:12]	X X	XV6TOG2_6 XV6TOG3_6	XV6 Toggle Position 2. XV6 Toggle Position 3.
52	[11:0] [23:12]	X X	FREEZE1_6 RESUME1_6	XV1 to XV6 Freeze Position 1. XV1 to XV6 Resume Position 1.
53	[11:0] [23:12]	X X	FREEZE2_6 RESUME2_6	XV1 to XV6 Freeze Position 2. XV1 to XV6 Resume Position 2.

Table 54. Vertical Pattern Group 7 (VPAT7) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
54	[5:0] [11:6] [23:12]	X X X	VPOL_7 UNUSED VPATLEN_7	VPAT7 Start Polarity. XV1[0], XV2[1], XV3[2], XV4[3], XV5[4], XV6[5]. Unused. Total Length of VPAT7. Note: If using VPAT7 as a second vertical sequence in the VSG active line, this value is the start position for the second vertical sequence.
55	[11:0] [23:12]	X X	XV1TOG1_7 XV1TOG2_7	XV1 Toggle Position 1. XV1 Toggle Position 2.
56	[11:0] [23:12]	X X	XV1TOG3_7 XV2TOG1_7	XV1 Toggle Position 3. XV2 Toggle Position 1.
57	[11:0] [23:12]	X X	XV2TOG2_7 XV2TOG3_7	XV2 Toggle Position 2. XV2 Toggle Position 3.
58	[11:0] [23:12]	X X	XV3TOG1_7 XV3TOG2_7	XV3 Toggle Position 1. XV3 Toggle Position 2.
59	[11:0] [23:12]	X X	XV3TOG3_7 XV4TOG1_7	XV3 Toggle Position 3. XV4 Toggle Position 1.
5A	[11:0] [23:12]	X X	XV4TOG2_7 XV4TOG3_7	XV4 Toggle Position 2. XV4 Toggle Position 3.
5B	[11:0] [23:12]	X X	XV5TOG1_7 XV5TOG2_7	XV5 Toggle Position 1. XV5 Toggle Position 2.
5C	[11:0] [23:12]	X X	XV5TOG3_7 XV6TOG1_7	XV5 Toggle Position 3. XV6 Toggle Position 1.
5D	[11:0] [23:12]	X X	XV6TOG2_7 XV6TOG3_7	XV6 Toggle Position 2. XV6 Toggle Position 3.
5E	[11:0] [23:12]	X X	FREEZE1_7 RESUME1_7	XV1 to XV6 Freeze Position 1. XV1 to XV6 Resume Position 1.
5F	[11:0] [23:12]	X X	FREEZE2_7 RESUME2_7	XV1 to XV6 Freeze Position 2. XV1 to XV6 Resume Position 2.

Table 55. Vertical Pattern Group 8 (VPAT8) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
60	[5:0] [11:6] [23:12]	X X X	VPOL_8 UNUSED VPATLEN_8	VPAT8 Start Polarity. XV1[0], XV2[1], XV3[2], XV4[3], XV5[4], XV6[5]. Unused. Total Length of VPAT8. Note: If using VPAT8 as a second vertical sequence in the VSG active line, this value is the start position for the second vertical sequence.
61	[11:0] [23:12]	X X	XV1TOG1_8 XV1TOG2_8	XV1 Toggle Position 1. XV1 Toggle Position 2.
62	[11:0] [23:12]	X X	XV1TOG3_8 XV1TOG4_8	XV1 Toggle Position 3. XV1 Toggle Position 4.
63	[11:0] [23:12]	X X	XV2TOG1_8 XV2TOG2_8	XV2 Toggle Position 1. XV2 Toggle Position 2.
64	[11:0] [23:12]	X X	XV2TOG3_8 XV2TOG4_8	XV2 Toggle Position 3. XV2 Toggle Position 4.
65	[11:0] [23:12]	X X	XV3TOG1_8 XV3TOG2_8	XV3 Toggle Position 1. XV3 Toggle Position 2.
66	[11:0] [23:12]	X X	XV3TOG3_8 XV3TOG4_8	XV3 Toggle Position 3. XV3 Toggle Position 4.
67	[11:0] [23:12]	X X	XV4TOG1_8 XV4TOG2_8	XV4 Toggle Position 1. XV4 Toggle Position 2.
68	[11:0] [23:12]	X X	XV4TOG3_8 XV4TOG4_8	XV4 Toggle Position 3. XV4 Toggle Position 4.
69	[11:0] [23:12]	X X	XV5TOG1_8 XV5TOG2_8	XV5 Toggle Position 1. XV5 Toggle Position 2.
6A	[11:0] [23:12]	X X	XV5TOG3_8 XV5TOG4_8	XV5 Toggle Position 3. XV5 Toggle Position 4.
6B	[11:0] [23:12]	X X	XV6TOG1_8 XV6TOG2_8	XV6 Toggle Position 1. XV6 Toggle Position 2.
6C	[11:0] [23:12]	X X	XV6TOG3_8 XV6TOG4_8	XV6 Toggle Position 3. XV6 Toggle Position 4.
6D	[11:0] [23:12]	X X	FREEZE1_8 RESUME1_8	XV1 to XV6 Freeze Position 1. XV1 to XV6 Resume Position 1.
6E	[11:0] [23:12]	X X	FREEZE2_8 RESUME2_8	XV1 to XV6 Freeze Position 2. XV1 to XV6 Resume Position 2.
6F			UNUSED	Unused.

Table 56. Vertical Pattern Group 9 (VPAT9) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
70	[5:0] [11:6] [23:12]	X X X	VPOL_9 UNUSED VPATLEN_9	VPAT9 Start Polarity. XV1[0], XV2[1], XV3[2], XV4[3], XV5[4], XV6[5]. Unused. Total Length of VPAT9. Note: If using VPAT9 as a second vertical sequence in the VSG active line, this value is the start position for the second vertical sequence.
71	[11:0] [23:12]	X X	XV1TOG1_9 XV1TOG2_9	XV1 Toggle Position 1. XV1 Toggle Position 2.
72	[11:0] [23:12]	X X	XV1TOG3_9 XV1TOG4_9	XV1 Toggle Position 3. XV1 Toggle Position 4.
73	[11:0] [23:12]	X X	XV2TOG1_9 XV2TOG2_9	XV2 Toggle Position 1. XV2 Toggle Position 2.
74	[11:0] [23:12]	X X	XV3TOG3_9 XV3TOG4_9	XV2 Toggle Position 3. XV2 Toggle Position 4.
75	[11:0] [23:12]	X X	XV3TOG1_9 XV4TOG2_9	XV3 Toggle Position 1. XV3 Toggle Position 2.
76	[11:0] [23:12]	X X	XV4TOG3_9 XV4TOG4_9	XV3 Toggle Position 3. XV3 Toggle Position 4.
77	[11:0] [23:12]	X X	XV5TOG1_9 XV5TOG2_9	XV4 Toggle Position 1. XV4 Toggle Position 2.
78	[11:0] [23:12]	X X	XV5TOG3_9 XV6TOG4_9	XV4 Toggle Position 3. XV4 Toggle Position 4.
79	[11:0] [23:12]	X X	XV6TOG1_9 XV6TOG2_9	XV5 Toggle Position 1. XV5 Toggle Position 2.
7A	[11:0] [23:12]	X X	XV6TOG3_9 XV6TOG4_9	XV5 Toggle Position 3. XV5 Toggle Position 4.
7B	[11:0] [23:12]	X X	XV6TOG1_9 XV6TOG2_9	XV6 Toggle Position 1. XV6 Toggle Position 2.
7C	[11:0] [23:12]	X X	XV6TOG3_9 XV6TOG4_9	XV6 Toggle Position 3. XV6 Toggle Position 4.
7D	[11:0] [23:12]	X X	FREEZE1_9 RESUME1_9	XV1 to XV6 Freeze Position 1. XV1 to XV6 Resume Position 1.
7E	[11:0] [23:12]	X X	FREEZE2_9 RESUME2_9	XV1 to XV6 Freeze Position 2. XV1 to XV6 Resume Position 2.

Table 57. Register Map Selection (SCK Updated Register)

Address	Data Bit Content	Default Value	Register Name	Register Description
7F	[1:0]	0	BANKSELECT	Register Bank Access for Bank 1, Bank 2, and Bank 3.

Table 58. Vertical Sequence 0 (VSEQ0) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
80	[1:0]	X	HBLKMASK_0	Masking Polarity during HBLK. H1 [0], H3 [1].
	[2]	X	CLPOBPOL_0	CLPOB Start Polarity.
	[3]	X	PBLKPOL_0	PBLK Start Polarity.
	[7:4]	X	VPATSEL_0	Selected Vertical Pattern Group for Vertical Sequence 0.
	[9:8]	X	VMASK_0	Enable Masking of Vertical Outputs (Specified by FREEZE/RESUME Registers).
	[11:10]	X	HBLKALT_0	Enable HBLK Alternation.
	[12]	X	HDLEN13_0	13th Bit for HD Length Counter Allows HD Length up to 8191 Pixels.
	[23:12]		UNUSED	Unused.
81	[11:0]	X	VPATREPO_0	Number of Selected Vertical Pattern Group Repetitions for Odd Lines.
	[23:12]	X	VPATREPE_0	Number of Selected Vertical Pattern Group Repetitions for Even Lines.
82	[11:0]	X	VPATSTART_0	Start Position in the Line for the Selected Vertical Pattern Group.
	[23:12]	X	HDLEN_0	HD Line Length (Number of Pixels) for Vertical Sequence 0.
83	[11:0]	X	PBLKTOG1_0	PBLK Toggle Position 1 for Vertical Sequence 0.
	[23:12]	X	PBLKTOG2_0	PBLK Toggle Position 2 for Vertical Sequence 0.
84	[11:0]	X	HBLKTOG1_0	HBLK Toggle Position 1 for Vertical Sequence 0.
	[23:12]	X	HBLKTOG2_0	HBLK Toggle Position 2 for Vertical Sequence 0.
85	[11:0]	X	HBLKTOG3_0	HBLK Toggle Position 3 for Vertical Sequence 0.
	[23:12]	X	HBLKTOG4_0	HBLK Toggle Position 4 for Vertical Sequence 0.
86	[11:0]	X	HBLKTOG5_0	HBLK Toggle Position 5 for Vertical Sequence 0.
	[23:12]	X	HBLKTOG6_0	HBLK Toggle Position 6 for Vertical Sequence 0.
87	[11:0]	X	CLPOBTOG1_0	CLPOB Toggle Position 1 for Vertical Sequence 0.
	[23:12]	X	CLPOBTOG2_0	CLPOB Toggle Position 2 for Vertical Sequence 0.

Table 59. Vertical Sequence 1 (VSEQ1) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
88	[1:0]	X	HBLKMASK_1	Masking Polarity during HBLK. H1 [0], H3 [1].
	[2]	X	CLPOBPOL_1	CLPOB Start Polarity.
	[3]	X	PBLKPOL_1	PBLK Start Polarity.
	[7:4]	X	VPATSEL_1	Selected Vertical Pattern Group for Vertical Sequence 1.
	[9:8]	X	VMASK_1	Enable Masking of Vertical Outputs (Specified by FREEZE/RESUME Registers).
	[11:10]	X	HBLKALT_1	Enable HBLK Alternation.
	[12]	X	HDLEN13_1	13th Bit for HD Length Counter Allows HD Length up to 8191 Pixels.
	[23:12]		UNUSED	Unused.
89	[11:0]	X	VPATREPO_1	Number of Selected Vertical Pattern Group Repetitions for Odd Lines.
	[23:12]	X	VPATREPE_1	Number of Selected Vertical Pattern Group Repetitions for Even Lines.
8A	[11:0]	X	VPATSTART_1	Start Position in the Line for the Selected Vertical Pattern Group.
	[23:12]	X	HDLEN_1	HD Line Length (Number of Pixels) for Vertical Sequence 1.
8B	[11:0]	X	PBLKTOG1_1	PBLK Toggle Position 1 for Vertical Sequence 1.
	[23:12]	X	PBLKTOG2_1	PBLK Toggle Position 2 for Vertical Sequence 1.
8C	[11:0]	X	HBLKTOG1_1	HBLK Toggle Position 1 for Vertical Sequence 1.
	[23:12]	X	HBLKTOG2_1	HBLK Toggle Position 2 for Vertical Sequence 1.
8D	[11:0]	X	HBLKTOG3_1	HBLK Toggle Position 3 for Vertical Sequence 1.
	[23:12]	X	HBLKTOG4_1	HBLK Toggle Position 4 for Vertical Sequence 1.
8E	[11:0]	X	HBLKTOG5_1	HBLK Toggle Position 5 for Vertical Sequence 1.
	[23:12]	X	HBLKTOG6_1	HBLK Toggle Position 6 for Vertical Sequence 1.
8F	[11:0]	X	CLPOBTOG1_1	CLPOB Toggle Position 1 for Vertical Sequence 1.
	[23:12]	X	CLPOBTOG2_1	CLPOB Toggle Position 2 for Vertical Sequence 1.

Table 60. Vertical Sequence 2 (VSEQ2) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
90	[1:0]	X	HBLKMASK_2	Masking Polarity during HBLK. H1 [0], H3 [1].
	[2]	X	CLPOBPOL_2	CLPOB Start Polarity.
	[3]	X	PBLKPOL_2	PBLK Start Polarity.
	[7:4]	X	VPATSEL_2	Selected Vertical Pattern Group for Vertical Sequence 2.
	[9:8]	X	VMASK_2	Enable Masking of Vertical Outputs (Specified by FREEZE/RESUME Registers).
	[11:10]	X	HBLKALT_2	Enable HBLK Alternation .
	[12]	X	HDLEN13_2	13th Bit for HD Length Counter Allows HD Length up to 8191 Pixels.
	[23:12]		UNUSED	Unused.
91	[11:0]	X	VPATREPO_2	Number of Selected Vertical Pattern Group Repetitions for Odd Lines.
	[23:12]	X	VPATREPE_2	Number of Selected Vertical Pattern Group Repetitions for Even Lines.
92	[11:0]	X	VPATSTART_2	Start Position in the Line for the Selected Vertical Pattern Group.
	[23:12]	X	HDLEN_2	HD Line Length (Number of Pixels) for Vertical Sequence 2.
93	[11:0]	X	PBLKTOG1_2	PBLK Toggle Position 1 for Vertical Sequence 2.
	[23:12]	X	PBLKTOG2_2	PBLK Toggle Position 2 for Vertical Sequence 2.
94	[11:0]	X	HBLKTOG1_2	HBLK Toggle Position 1 for Vertical Sequence 2.
	[23:12]	X	HBLKTOG2_2	HBLK Toggle Position 2 for Vertical Sequence 2.
95	[11:0]	X	HBLKTOG3_2	HBLK Toggle Position 3 for Vertical Sequence 2.
	[23:12]	X	HBLKTOG4_2	HBLK Toggle Position 4 for Vertical Sequence 2.
96	[11:0]	X	HBLKTOG5_2	HBLK Toggle Position 5 for Vertical Sequence 2.
	[23:12]	X	HBLKTOG6_2	HBLK Toggle Position 6 for Vertical Sequence 2.
97	[11:0]	X	CLPOBTOG1_2	CLPOB Toggle Position 1 for Vertical Sequence 2.
	[23:12]	X	CLPOBTOG2_2	CLPOB Toggle Position 2 for Vertical Sequence 2.

Table 61. Vertical Sequence 3 (VSEQ3) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
98	[1:0]	X	HBLKMASK_3	Masking Polarity during HBLK. H1 [0], H3 [1].
	[2]	X	CLPOBPOL_3	CLPOB Start Polarity.
	[3]	X	PBLKPOL_3	PBLK Start Polarity.
	[7:4]	X	VPATSEL_3	Selected Vertical Pattern Group for Vertical Sequence 3.
	[9:8]	X	VMASK_3	Enable Masking of Vertical Outputs (Specified by FREEZE/RESUME Registers).
	[11:10]	X	HBLKALT_3	Enable HBLK Alternation
	[12]	X	HDLEN13_3	13th Bit for HD Length Counter Allows HD Length up to 8191 Pixels.
	[23:12]		UNUSED	Unused.
99	[11:0]	X	VPATREPO_3	Number of Selected Vertical Pattern Group Repetitions for Odd Lines.
	[23:12]	X	VPATREPE_3	Number of Selected Vertical Pattern Group Repetitions for Even Lines.
9A	[11:0]	X	VPATSTART_3	Start Position in the Line for the Selected Vertical Pattern Group.
	[23:12]	X	HDLEN_3	HD Line Length (Number of Pixels) for Vertical Sequence 3.
9B	[11:0]	X	PBLKTOG1_3	PBLK Toggle Position 1 for Vertical Sequence 3.
	[23:12]	X	PBLKTOG2_3	PBLK Toggle Position 2 for Vertical Sequence 3.
9C	[11:0]	X	HBLKTOG1_3	HBLK Toggle Position 1 for Vertical Sequence 3.
	[23:12]	X	HBLKTOG2_3	HBLK Toggle Position 2 for Vertical Sequence 3.
9D	[11:0]	X	HBLKTOG3_3	HBLK Toggle Position 3 for Vertical Sequence 3.
	[23:12]	X	HBLKTOG4_3	HBLK Toggle Position 4 for Vertical Sequence 3.
9E	[11:0]	X	HBLKTOG5_3	HBLK Toggle Position 5 for Vertical Sequence 3.
	[23:12]	X	HBLKTOG6_3	HBLK Toggle Position 6 for Vertical Sequence 3.
9F	[11:0]	X	CLPOBTOG1_3	CLPOB Toggle Position 1 for Vertical Sequence 3.
	[23:12]	X	CLPOBTOG2_3	CLPOB Toggle Position 2 for Vertical Sequence 3.

Table 62. Vertical Sequence 4 (VSEQ4) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
A0	[1:0]	X	HBLKMASK_4	Masking Polarity during HBLK. H1 [0], H3 [1].
	[2]	X	CLPOBPOL_4	CLPOB Start Polarity.
	[3]	X	PBLKPOL_4	PBLK Start Polarity.
	[7:4]	X	VPATSEL_4	Selected Vertical Pattern Group for Vertical Sequence 4.
	[9:8]	X	VMASK_4	Enable Masking of Vertical Outputs (Specified by FREEZE/RESUME Registers).
	[11:10]	X	HBLKALT_4	Enable HBLK Alternation.
	[12]	X	HDLEN13_4	13th Bit for HD Length Counter Allows HD Length up to 8191 Pixels.
	[23:12]		UNUSED	Unused.
A1	[11:0]	X	VPATREPO_4	Number of Selected Vertical Pattern Group Repetitions for Odd Lines.
	[23:12]	X	VPATREPE_4	Number of Selected Vertical Pattern Group Repetitions for Even Lines.
A2	[11:0]	X	VPATSTART_4	Start Position in the Line for the Selected Vertical Pattern Group.
	[23:12]	X	HDLEN_4	HD Line Length (Number of Pixels) for Vertical Sequence 4.
A3	[11:0]	X	PBLKTOG1_4	PBLK Toggle Position 1 for Vertical Sequence 4.
	[23:12]	X	PBLKTOG2_4	PBLK Toggle Position 2 for Vertical Sequence 4.
A4	[11:0]	X	HBLKTOG1_4	HBLK Toggle Position 1 for Vertical Sequence 4.
	[23:12]	X	HBLKTOG2_4	HBLK Toggle Position 2 for Vertical Sequence 4.
A5	[11:0]	X	HBLKTOG3_4	HBLK Toggle Position 3 for Vertical Sequence 4.
	[23:12]	X	HBLKTOG4_4	HBLK Toggle Position 4 for Vertical Sequence 4.
A6	[11:0]	X	HBLKTOG5_4	HBLK Toggle Position 5 for Vertical Sequence 4.
	[23:12]	X	HBLKTOG6_4	HBLK Toggle Position 6 for Vertical Sequence 4.
A7	[11:0]	X	CLPOBTOG1_4	CLPOB Toggle Position 1 for Vertical Sequence 4.
	[23:12]	X	CLPOBTOG2_4	CLPOB Toggle Position 2 for Vertical Sequence 4.

Table 63. Vertical Sequence 5 (VSEQ5)Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
A8	[1:0]	X	HBLKMASK_5	Masking Polarity during HBLK. H1 [0], H3 [1].
	[2]	X	CLPOBPOL_5	CLPOB Start Polarity.
	[3]	X	PBLKPOL_5	PBLK Start Polarity.
	[7:4]	X	VPATSEL_5	Selected Vertical Pattern Group for Vertical Sequence 5.
	[9:8]	X	VMASK_5	Enable Masking of Vertical Outputs (Specified by FREEZE/RESUME registers).
	[11:10]	X	HBLKALT_5	Enable HBLK Alternation.
	[12]	X	HDLEN13_5	13th Bit for HD Length Counter Allows HD Length up to 8191 Pixels.
	[23:12]		UNUSED	Unused.
A9	[11:0]	X	VPATREPO_5	Number of Selected Vertical Pattern Group Repetitions for Odd Lines.
	[23:12]	X	VPATREPE_5	Number of Selected Vertical Pattern Group Repetitions for Even Lines.
AA	[11:0]	X	VPATSTART_5	Start Position in the Line for the Selected Vertical Pattern Group.
	[23:12]	X	HDLEN_5	HD Line Length (Number of Pixels) for Vertical Sequence 5.
AB	[11:0]	X	PBLKTOG1_5	PBLK Toggle Position 1 for Vertical Sequence 5.
	[23:12]	X	PBLKTOG2_5	PBLK Toggle Position 2 for Vertical Sequence 5.
AC	[11:0]	X	HBLKTOG1_5	HBLK Toggle Position 1 for Vertical Sequence 5.
	[23:12]	X	HBLKTOG2_5	HBLK Toggle Position 2 for Vertical Sequence 5.
AD	[11:0]	X	HBLKTOG3_5	HBLK Toggle Position 3 for Vertical Sequence 5.
	[23:12]	X	HBLKTOG4_5	HBLK Toggle Position 4 for Vertical Sequence 5.
AE	[11:0]	X	HBLKTOG5_5	HBLK Toggle Position 5 for Vertical Sequence 5.
	[23:12]	X	HBLKTOG6_5	HBLK Toggle Position 6 for Vertical Sequence 5.
AF	[11:0]	X	CLPOBTOG1_5	CLPOB Toggle Position 1 for Vertical Sequence 5.
	[23:12]	X	CLPOBTOG2_5	CLPOB Toggle Position 2 for Vertical Sequence 5.

Table 64. Vertical Sequence 6 (VSEQ6) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
B0	[1:0]	X	HBLKMASK_6	Masking Polarity during HBLK. H1 [0], H3 [1].
	[2]	X	CLPOBPOL_6	CLPOB Start Polarity.
	[3]	X	PBLKPOL_6	PBLK Start Polarity.
	[7:4]	X	VPATSEL_6	Selected Vertical Pattern Group for Vertical Sequence 6.
	[9:8]	X	VMASK_6	Enable Masking of Vertical outputs (specified by FREEZE/RESUME registers).
	[11:10]	X	HBLKALT_6	Enable HBLK Alternation.
	[12]	X	HDLEN13_6	13th Bit for HD Length Counter Allows HD Length up to 8191 Pixels.
	[23:12]		UNUSED	Unused.
B1	[11:0]	X	VPATREPO_6 V	Number of Selected Vertical Pattern Group Repetitions for Odd Lines.
	[23:12]	X	PATREPE_6	Number of Selected Vertical Pattern Group Repetitions for Even Lines.
B2	[11:0]	X	VPATSTART_6	Start Position in the Line for the Selected Vertical Pattern Group.
	[23:12]	X	HDLEN_6	HD Line Length (Number of Pixels) for Vertical Sequence 6.
B3	[11:0]	X	PBLKTOG1_6	PBLK Toggle Position 1 for Vertical Sequence 6.
	[23:12]	X	PBLKTOG2_6	PBLK Toggle Position 2 for Vertical Sequence 6.
B4	[11:0]	X	HBLKTOG1_6	HBLK Toggle Position 1 for Vertical Sequence 6.
	[23:12]	X	HBLKTOG2_6	HBLK Toggle Position 2 for Vertical Sequence 6.
B5	[11:0]	X	HBLKTOG3_6	HBLK Toggle Position 3 for Vertical Sequence 6.
	[23:12]	X	HBLKTOG4_6	HBLK Toggle Position 4 for Vertical Sequence 6.
B6	[11:0]	X	HBLKTOG5_6	HBLK Toggle Position 5 for Vertical Sequence 6.
	[23:12]	X	HBLKTOG6_6	HBLK Toggle Position 6 for Vertical Sequence 6.
B7	[11:0]	X	CLPOBTOG1_6	CLPOB Toggle Position 1 for Vertical Sequence 6.
	[23:12]	X	CLPOBTOG2_6	CLPOB Toggle Position 2 for Vertical Sequence 6.

Table 65. Vertical Sequence 7 (VSEQ7) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
B8	[1:0]	X	HBLKMASK_7	Masking Polarity during HBLK. H1 [0], H3 [1].
	[2]	X	CLPOBPOL_7	CLPOB Start Polarity.
	[3]	X	PBLKPOL_7	PBLK Start Polarity.
	[7:4]	X	VPATSEL_7	Selected Vertical Pattern Group for Vertical Sequence 7.
	[9:8]	X	VMASK_7	Enable Masking of Vertical Outputs (Specified by FREEZE/RESUME Registers).
	[11:10]	X	HBLKALT_7	Enable HBLK Alternation.
	[12]	X	HDLEN13_7	13th Bit for HD Length Counter Allows HD Length up to 8191 Pixels.
	[23:12]		UNUSED	Unused.
B9	[11:0]	X	VPATREPO_7	Number of Selected Vertical Pattern Group Repetitions for Odd Lines.
	[23:12]	X	VPATREPE_7	Number of Selected Vertical Pattern Group Repetitions for Even Lines.
BA	[11:0]	X	VPATSTART_7	Start Position in the Line for the Selected Vertical Pattern Group.
	[23:12]	X	HDLEN_7	HD Line Length (Number of Pixels) for Vertical Sequence 7.
BB	[11:0]	X	PBLKTOG1_7	PBLK Toggle Position 1 for Vertical Sequence 7.
	[23:12]	X	PBLKTOG2_7	PBLK Toggle Position 2 for Vertical Sequence 7.
BC	[11:0]	X	HBLKTOG1_7	HBLK Toggle Position 1 for Vertical Sequence 7.
	[23:12]	X	HBLKTOG2_7	HBLK Toggle Position 2 for Vertical Sequence 7.
BD	[11:0]	X	HBLKTOG3_7	HBLK Toggle Position 3 for Vertical Sequence 7.
	[23:12]	X	HBLKTOG4_7	HBLK Toggle Position 4 for Vertical Sequence 7.
BE	[11:0]	X	HBLKTOG5_7	HBLK Toggle Position 5 for Vertical Sequence 7.
	[23:12]	X	HBLKTOG6_7	HBLK Toggle Position 6 for Vertical Sequence 7.
BF	[11:0]	X	CLPOBTOG1_7	CLPOB Toggle Position 1 for Vertical Sequence 7.
	[23:12]	X	CLPOBTOG2_7	CLPOB Toggle Position 2 for Vertical Sequence 7.

Table 66. Vertical Sequence 8 (VSEQ8) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
C0	[1:0]	X	HBLKMASK_8	Masking Polarity during HBLK. H1 [0], H3 [1].
	[2]	X	CLPOBPOL_8	CLPOB Start Polarity.
	[3]	X	PBLKPOL_8	PBLK Start Polarity.
	[7:4]	X	VPATSEL_8	Selected Vertical Pattern Group for Vertical Sequence 8.
	[9:8]	X	VMASK_8	Enable Masking of Vertical Outputs (Specified by FREEZE/RESUME Registers).
	[11:10]	X	HBLKALT_8	Enable HBLK Alternation.
	[12]	X	HDLEN13_8	13th Bit for HD Length Counter Allows HD Length up to 8191 Pixels.
	[23:12]		UNUSED	Unused.
C1	[11:0]	X	VPATREPO_8	Number of Selected Vertical Pattern Group Repetitions for Odd Lines.
	[23:12]	X	VPATREPE_8	Number of Selected Vertical Pattern Group Repetitions for Even Lines.
C2	[11:0]	X	VPATSTART_8	Start Position in the Line for the Selected Vertical Pattern Group.
	[23:12]	X	HDLEN_8	HD Line Length (Number of Pixels) for Vertical Sequence 8.
C3	[11:0]	X	PBLKTOG1_8	PBLK Toggle Position 1 for Vertical Sequence 8.
	[23:12]	X	PBLKTOG2_8	PBLK Toggle Position 2 for Vertical Sequence 8.
C4	[11:0]	X	HBLKTOG1_8	HBLK Toggle Position 1 for Vertical Sequence 8.
	[23:12]	X	HBLKTOG2_8	HBLK Toggle Position 2 for Vertical Sequence 8.
C5	[11:0]	X	HBLKTOG3_8	HBLK Toggle Position 3 for Vertical Sequence 8.
	[23:12]	X	HBLKTOG4_8	HBLK Toggle Position 4 for Vertical Sequence 8.
C6	[11:0]	X	HBLKTOG5_8	HBLK Toggle Position 5 for Vertical Sequence 8.
	[23:12]	X	HBLKTOG6_8	HBLK Toggle Position 6 for Vertical Sequence 8.
C7	[11:0]	X	CLPOBTOG1_8	CLPOB Toggle Position 1 for Vertical Sequence 8.
	[23:12]	X	CLPOBTOG2_8	CLPOB Toggle Position 2 for Vertical Sequence 8.

Table 67. Vertical Sequence 9 (VSEQ9) Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
C8	[1:0]	X	HBLKMASK_9	Masking Polarity during HBLK. H1 [0], H3 [1].
	[2]	X	CLPOBPOL_9	CLPOB Start Polarity.
	[3]	X	PBLKPOL_9	PBLK Start Polarity.
	[7:4]	X	VPATSEL_9	Selected Vertical Pattern Group for Vertical Sequence 9.
	[9:8]	X	VMASK_9	Enable Masking of Vertical Outputs (Specified by FREEZE/RESUME registers).
	[11:10]	X	HBLKALT_9	Enable HBLK Alternation.
	[12]	X	HDLEN13_9	13th Bit for HD Length Counter Allows HD Length up to 8191 Pixels.
	[23:12]		UNUSED	Unused.
C9	[11:0]	X	VPATREPO_9	Number of Selected Vertical Pattern Group Repetitions for Odd Lines.
	[23:12]	X	VPATREPE_9	Number of Selected Vertical Pattern Group Repetitions for Even Lines.
CA	[11:0]	X	VPATSTART_9	Start Position in the Line for the Selected Vertical Pattern Group.
	[23:12]	X	HDLEN_9	HD Line Length (Number of Pixels) for Vertical Sequence 9.
CB	[11:0]	X	PBLKTOG1_9	PBLK Toggle Position 1 for Vertical Sequence 9.
	[23:12]	X	PBLKTOG2_9	PBLK Toggle Position 2 for Vertical Sequence 9.
CC	[11:0]	X	HBLKTOG1_9	HBLK Toggle Position 1 for Vertical Sequence 9.
	[23:12]	X	HBLKTOG2_9	HBLK Toggle Position 2 for Vertical Sequence 9.
CD	[11:0]	X	HBLKTOG3_9	HBLK Toggle Position 3 for Vertical Sequence 9.
	[23:12]	X	HBLKTOG4_9	HBLK Toggle Position 4 for Vertical Sequence 9.
CE	[11:0]	X	HBLKTOG5_9	HBLK Toggle Position 5 for Vertical Sequence 9.
	[23:12]	X	HBLKTOG6_9	HBLK Toggle Position 6 for Vertical Sequence 9.
CF	[11:0]	X	CLPOBTOG1_9	CLPOB Toggle Position 1 for Vertical Sequence 9.
	[23:12]	X	CLPOBTOG2_9	CLPOB Toggle Position 2 for Vertical Sequence 9.

Table 68. Field 0 Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
D0	[3:0]	X	VSEQSEL0_0	Selected Vertical Sequence for Region 0.
	[4]	X	SWEEP0_0	Select Sweep Region for Region 0. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI0_0	Select Multiplier Region for Region 0. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL1_0	Selected Vertical Sequence for Region 1.
	[10]	X	SWEEP1_0	Select Sweep Region for Region 1. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI1_0	Select Multiplier Region for Region 1. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL2_0	Selected Vertical Sequence for Region 2.
	[16]	X	SWEEP2_0	Select Sweep Region for Region 2. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI2_0	Select Multiplier Region for Region 2. 0 = No Multiplier, 1 = Multiplier.
	[21:18]	X	VSEQSEL3_0	Selected Vertical Sequence for Region 3.
	[22]	X	SWEEP3_0	Select Sweep Region for Region 3. 0 = No Sweep, 1 = Sweep.
	[23]	X	MULTI3_0	Select Multiplier Region for Region 3. 0 = No Multiplier, 1 = Multiplier.
D1	[3:0]	X	VSEQSEL4_0	Selected Vertical Sequence for Region 4.
	[4]	X	SWEEP4_0	Select Sweep Region for Region 4. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI4_0	Select Multiplier Region for Region 4. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL5_0	Selected Vertical Sequence for Region 5.
	[10]	X	SWEEP5_0	Select Sweep Region for Region 5. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI5_0	Select Multiplier Region for Region 5. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL6_0	Selected Vertical Sequence for Region 6.
	[16]	X	SWEEP6_0	Select Sweep Region for Region 6. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI6_0	Select Multiplier Region for Region 6. 0 = No Multiplier, 1 = Multiplier.
	[23:18]		UNUSED	Unused.
D2	[11:0]	X	SCP1_0	Vertical Sequence Change Position No. 1 for Field 0.
	[23:12]	X	SCP2_0	Vertical Sequence Change Position No. 2 for Field 0.
D3	[11:0]	X	SCP3_0	Vertical Sequence Change Position No. 3 for Field 0.
	[23:12]	X	SCP4_0	Vertical Sequence Change Position No. 4 for Field 0.
D4	[11:0]	X	VDLEN_0	VD Field Length (Number of Lines) for Field 0.
	[23:12]	X	HDLAST_0	HD Line Length (Number of Pixels) for Last Line in Field 0.
D5	[3:0]	X	VPATSECOND_0	Selected Second Vertical Pattern Group for VSG Active Line.
	[9:4]	X	SGMASK_0	Masking of VSG Outputs during VSG Active Line.
	[21:10]		SGPATSEL_0	Selection of VSG Patterns for Each VSG Output.
	[22]		HDLAST13_0	MSB for 13-Bit Last Line Length
D6	[11:0]	X	SGLINE1_0	VSG Active Line 1.
	[23:12]	X	SGLINE2_0	VSG Active Line 2 (If No Second Line Is Needed, Set to Same as Line 1 or Maximum).
D7	[11:0]	X	SCP5_0	Vertical Sequence Change Position No. 5 for Field 0.
	[23:12]	X	SCP6_0	Vertical Sequence Change Position No. 6 for Field 0.

Table 69. Field 1 Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
D8	[3:0]	X	VSEQSEL0_1	Selected Vertical Sequence for Region 0.
	[4]	X	SWEEP0_1	Select Sweep Region for Region 0. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI0_1	Select Multiplier Region for Region 0. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL1_1	Selected Vertical Sequence for Region 1.
	[10]	X	SWEEP1_1	Select Sweep Region for Region 1. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI1_1	Select Multiplier Region for Region 1. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL2_1	Selected Vertical Sequence for Region 2.
	[16]	X	SWEEP2_1	Select Sweep Region for Region 2. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI2_1	Select Multiplier Region for Region 2. 0 = No Multiplier, 1 = Multiplier.
	[21:18]	X	VSEQSEL3_1	Selected Vertical Sequence for Region 3.
	[22]	X	SWEEP3_1	Select Sweep Region for Region 3. 0 = No Sweep, 1 = Sweep.
	[23]	X	MULTI3_1	Select Multiplier Region for Region 3. 0 = No Multiplier, 1 = Multiplier.
D9	[3:0]	X	VSEQSEL4_1	Selected Vertical Sequence for Region 4.
	[4]	X	SWEEP4_1	Select Sweep Region for Region 4. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI4_1	Select Multiplier Region for Region 4. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL5_1	Selected Vertical Sequence for Region 5.
	[10]	X	SWEEP5_1	Select Sweep Region for Region 5. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI5_1	Select Multiplier Region for Region 5. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL6_1	Selected Vertical Sequence for Region 6.
	[16]	X	SWEEP6_1	Select Sweep Region for Region 6. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI6_1	Select Multiplier Region for Region 6. 0 = No Multiplier, 1 = Multi-
	[23:18]		UNUSED	plier. Unused.
DA	[11:0]	X	SCP1_1	Vertical Sequence Change Position No. 1 for Field 1.
	[23:12]	X	SCP2_1	Vertical Sequence Change Position No. 2 for Field 1.
DB	[11:0]	X	SCP3_1	Vertical Sequence Change Position No. 3 for Field 1.
	[23:12]	X	SCP4_1	Vertical Sequence Change Position No. 4 for Field 1.
DC	[11:0]	X	VDLEN_1	VD Field Length (Number of Lines) for Field 1.
	[23:12]	X	HDLAST_1	HD Line Length (Number of Pixels) for Last Line in Field 1.
DD	[3:0]	X	VPATSECOND_1	Selected Second Vertical Pattern Group for VSG Active Line.
	[9:4]	X	SGMASK_1	Masking of VSG Outputs during VSG Active Line.
	[21:10]	X	SGPATSEL_1	Selection of VSG Patterns for Each VSG Output.
	[22]	X	HDLAST13_1	MSB for 13-Bit Last Line Length
DE	[11:0]	X	SGLINE1_1	VSG Active Line 1.
	[23:12]	X	SGLINE2_1	VSG Active Line 2. (If No Second Line Is Needed, Set to Same as Line 1 or Maximum).
DF	[11:0]	X	SCP5_1	Vertical Sequence Change Position No. 5 for Field 1.
	[23:12]	X	SCP6_1	Vertical Sequence Change Position No. 6 for Field 1.

Table 70. Field 2 Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
E0	[3:0]	X	VSEQSEL_2	Selected Vertical Sequence for Region 0 Sequence for Region 1.
	[4]	X	SWEEP0_2	Select Sweep Region for Region 0. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI0_2	Select Multiplier Region for Region 0. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL1_2	Selected Vertical Sequence for Region 1.
	[10]	X	SWEEP1_2	Select Sweep Region for Region 1. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI1_2	Select Multiplier Region for Region 1. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL2_2	Selected Vertical Sequence for Region 2.
	[16]	X	SWEEP2_2	Vertical Select Sweep Region for Region 2. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI2_2	Select Multiplier Region for Region 2. 0 = No Multiplier, 1 = Multiplier.
	[21:18]	X	VSEQSEL3_2	Selected Vertical Sequence for Region 3.
	[22]	X	SWEEP3_2	Select Sweep Region for Region 3. 0 = No Sweep, 1 = Sweep.
	[23]	X	MULTI3_2	Select Multiplier Region for Region 3. 0 = No Multiplier, 1 = Multiplier.
E1	[3:0]	X	VSEQSEL4_2	Selected Vertical Sequence for Region 4.
	[4]	X	SWEEP4_2	Select Sweep Region for Region 4. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI4_2	Select Multiplier Region for Region 4. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL5_2	Selected Vertical Sequence for Region 5.
	[10]	X	SWEEP5_2	Select Sweep Region for Region 5. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI5_2	Select Multiplier Region for Region 5. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL6_2	Selected Vertical Sequence for Region 6.
	[16]	X	SWEEP6_2	Select Sweep Region for Region 6. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI6_2	Select Multiplier Region for Region 6. 0 = No Multiplier, 1 = Multi-
	[23:18]		UNUSED	plier. Unused.
E2	[11:0]	X	SCP1_2	Vertical Sequence Change Position No. 1 for Field 2.
	[23:12]	X	SCP2_2	Vertical Sequence Change Position No. 2 for Field 2.
E3	[11:0]	X	SCP3_2	Vertical Sequence Change Position No. 3 for Field 2.
	[23:12]	X	SCP4_2	Vertical Sequence Change Position No. 4 for Field 2.
E4	[11:0]	X	VDLEN0_2	VD Field Length (Number of Lines) for Field 2.
	[23:12]	X	HDLAST_2	HD Line Length (Number of Pixels) for Last Line in Field 2.
E5	[3:0]	X	VPATSECOND_2	Selected Second Vertical Pattern Group for VSG Active Line.
	[9:4]	X	SGMASK_2	Masking of VSG Outputs during VSG Active Line.
	[21:10]	X	SGPATSEL_2	Selection of VSG Patterns for Each VSG Output.
	[22]	X	HDLAST13_2	MSB for 13-Bit Last Line Length
E6	[11:0]	X	SGLINE1_2	VSG Active Line 1.
	[23:12]	X	SGLINE2_2	VSG Active Line 2. (If No Second Line Is Needed, Set to Same as Line 1 or Maximum).
E7	[11:0]	X	SCP5_2	Vertical Sequence Change Position No. 5 for Field 2.
	[23:12]	X	SCP6_2	Vertical Sequence Change Position No. 6 for Field 2.

Table 71. Field 3 Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
E8	[3:0]	X	VSEQSEL_3	Selected Vertical Sequence for Region 0.
	[4]	X	SWEEP0_3	Select Sweep Region for Region 0. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI0_3	Select Multiplier Region for Region 0. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL1_3	Selected Vertical Sequence for Region 1.
	[10]	X	SWEEP1_3	Select Sweep Region for Region 1. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI1_3	Select Multiplier Region for Region 1. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL2_3	Selected Vertical Sequence for Region 2.
	[16]	X	SWEEP2_3	Select Sweep Region for Region 2. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI2_3	Select Multiplier Region for Region 2. 0 = No Multiplier, 1 = Multiplier.
	[21:18]	X	VSEQSEL3_3	Selected Vertical Sequence for Region 3.
	[22]	X	SWEEP3_3	Select Sweep Region for Region 3. 0 = No Sweep, 1 = Sweep.
	[23]	X	MULTI3_3	Select Multiplier Region for Region 3. 0 = No Multiplier, 1 = Multiplier.
E9	[3:0]	X	VSEQSEL4_3	Selected Vertical Sequence for Region 4.
	[4]	X	SWEEP4_3	Select Sweep Region for Region 4. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI4_3	Select Multiplier Region for Region 4. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL5_3	Selected Vertical Sequence for Region 5.
	[10]	X	SWEEP5_3	Select Sweep Region for Region 5. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI5_3	Select Multiplier Region for Region 5. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL6_3	Selected Vertical Sequence for Region 6.
	[16]	X	SWEEP6_3	Select Sweep Region for Region 6. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI6_3	Select Multiplier Region for Region 6. 0 = No Multiplier, 1 = Multiplier.
	[23:18]		UNUSED	Unused .
EA	[11:0]	X	SCP1_3	Vertical Sequence Change Position No. 1 for Field 3.
	[23:12]	X	SCP2_3	Vertical Sequence Change Position No. 2 for Field 3.
EB	[11:0]	X	SCP3_3	Vertical Sequence Change Position No. 3 for Field 3.
	[23:12]	X	SCP4_3	Vertical Sequence Change Position No. 4 for Field 3.
EC	[11:0]	X	VDLEN_3	VD Field Length (Number of Lines) for Field 3.
	[23:12]	X	HDLAST_3	HD Line Length (Number of Pixels) for Last Line in Field 3.
ED	[3:0]	X	VPATSECOND_3	Selected Second Vertical Pattern Group for VSG Active Line.
	[9:4]	X	SGMASK_3	Masking of VSG Outputs during VSG Active Line.
	[21:10]	X	SGPATSEL_3	Selection of VSG Patterns for Each VSG Output.
	[22]	X	HDLAST13_3	MSB for 13-Bit Last Line Length
EE	[11:0]	X	SGLINE1_3	VSG Active Line 1.
	[23:12]	X	SGLINE2_3	VSG Active Line 2. (If No Second Line Is Needed, Set to Same as Line 1 or Maximum).
EF	[11:0]	X	SCP5_3	Vertical Sequence Change Position No. 5 for Field 3.
	[23:12]	X	SCP6_3	Vertical Sequence Change Position No. 6 for Field 3.

Table 72. Field 4 Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
F0	[3:0]	X	VSEQSEL0_4	Selected Vertical Sequence for Region 0.
	[4]	X	SWEEP0_4	Select Sweep Region for Region 0. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI0_4	Select Multiplier Region for Region 0. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL1_4	Selected Vertical Sequence for Region 1.
	[10]	X	SWEEP1_4	Select Sweep Region for Region 1. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI1_4	Select Multiplier Region for Region 1. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL2_4	Selected Vertical Sequence for Region 2.
	[16]	X	SWEEP2_4	Select Sweep Region for Region 2. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI2_4	Select Multiplier Region for Region 2. 0 = No Multiplier, 1 = Multiplier.
	[21:18]	X	VSEQSEL3_4	Selected Vertical Sequence for Region 3.
	[22]	X	SWEEP3_4	Select Sweep Region for Region 3. 0 = No Sweep, 1 = Sweep.
	[23]	X	MULTI3_4	Select Multiplier Region for Region 3. 0 = No Multiplier, 1 = Multiplier.
F1	[3:0]	X	VSEQSEL4_4	Selected Vertical Sequence for Region 4.
	[4]	X	SWEEP4_4	Select Sweep Region for Region 4. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI4_4	Select Multiplier Region for Region 4. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL5_4	Selected Vertical Sequence for Region 5.
	[10]	X	SWEEP5_4	Select Sweep Region for Region 5. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI5_4	Select Multiplier Region for Region 5. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL6_4	Selected Vertical Sequence for Region 6.
	[16]	X	SWEEP6_4	Select Sweep Region for Region 6. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI6_4	Select Multiplier Region for Region 6. 0 = No Multiplier, 1 = Multiplier.
	[23:18]		UNUSED	Unused.
F2	[11:0]	X	SCP1_4	Vertical Sequence Change Position No. 1 for Field 4.
	[23:12]	X	SCP2_4	Vertical Sequence Change Position No. 2 for Field 4.
F3	[11:0]	X	SCP3_4	Vertical Sequence Change Position No. 3 for Field 4.
	[23:12]	X	SCP4_4	Vertical Sequence Change Position No. 4 for Field 4.
F4	[11:0]	X	VDLEN_4	VD Field Length (Number of Lines) for Field 4.
	[23:12]	X	HDLAST_4	HD Line Length (Number of Pixels) for Last Line in Field 4.
F5	[3:0]	X	VPATSECOND_4	Selected Second Vertical Pattern Group for VSG Active Line.
	[9:4]	X	SGMASK_4	Masking of VSG Outputs during VSG Active Line.
	[21:10]	X	SGPATSEL_4	Selection of VSG Patterns for Each VSG Output.
	[22]	X	HDLAST13_4	MSB for 13-Bit Last Line Length
F6	[11:0]	X	SGLINE1_4	VSG Active Line 1.
	[23:12]	X	SGLINE2_4	VSG Active Line 2. (If No Second Line Is Needed, Set to Same as Line 1 or Maximum).
F7	[11:0]	X	SCP5_4	Vertical Sequence Change Position No. 5 for Field 4.
	[23:12]	X	SCP6_4	Vertical Sequence Change Position No. 6 for Field 4.

Table 73. Field 5 Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
F8	[3:0]	X	VSEQSEL0_5	Selected Vertical Sequence for Region 0.
	[4]	X	SWEEP0_5	Select Sweep Region for Region 0. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI0_5	Select Multiplier Region for Region 0. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL1_5	Selected Vertical Sequence for Region 1.
	[10]	X	SWEEP1_5	Select Sweep Region for Region 1. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI1_5	Select Multiplier Region for Region 1. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL2_5	Selected Vertical Sequence for Region 2.
	[16]	X	SWEEP2_5	Select Sweep Region for Region 2. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI2_5	Select Multiplier Region for Region 2. 0 = No Multiplier, 1 = Multiplier.
	[21:18]	X	VSEQSEL3_5	Selected Vertical Sequence for Region 3.
	[22]	X	SWEEP3_5	Select Sweep Region for Region 3. 0 = No Sweep, 1 = Sweep.
	[23]	X	MULTI3_5	Select Multiplier Region for Region 3. 0 = No Multiplier, 1 = Multiplier.
F9	[3:0]	X	VSEQSEL4_5	Selected Vertical Sequence for Region 4.
	[4]	X	SWEEP4_5	Select Sweep Region for Region 4. 0 = No Sweep, 1 = Sweep.
	[5]	X	MULTI4_5	Select Multiplier Region for Region 4. 0 = No Multiplier, 1 = Multiplier.
	[9:6]	X	VSEQSEL5_5	Selected Vertical Sequence for Region 5.
	[10]	X	SWEEP5_5	Select Sweep Region for Region 5. 0 = No Sweep, 1 = Sweep.
	[11]	X	MULTI5_5	Select Multiplier Region for Region 5. 0 = No Multiplier, 1 = Multiplier.
	[15:12]	X	VSEQSEL6_5	Selected Vertical Sequence for Region 6.
	[16]	X	SWEEP6_5	Select Sweep Region for Region 6. 0 = No Sweep, 1 = Sweep.
	[17]	X	MULTI6_5	Select Multiplier Region for Region 6. 0 = No Multiplier, 1 = Multiplier.
	[23:18]		UNUSED	Unused.
FA	[11:0]	X	SCP1_5	Vertical Sequence Change Position No.1 for Field 5.
	[23:12]	X	SCP2_5	Vertical Sequence Change Position No.2 for Field 5.
FB	[11:0]	X	SCP3_5	Vertical Sequence Change Position No.3 for Field 5.
	[23:12]	X	SCP4_5	Vertical Sequence Change Position No.4 for Field 5.
FC	[11:0]	X	VDLEN_5	VD Field Length (Number of Lines) for Field 5.
	[23:12]	X	HDLAST_5	HD Line Length (Number of Pixels) for Last Line in Field 5.
FD	[3:0]	X	VPATSECOND_5	Selected Second Vertical Pattern Group for VSG Active Line.
	[9:4]	X	SGMASK_5	Masking of VSG Outputs during VSG Active Line.
	[21:10]	X	SGPATSEL_5	Selection of VSG Patterns for Each VSG Output.
	[22]	X	HDLAST13_5	MSB for 13-Bit Last Line Length
FE	[11:0]	X	SGLINE1_5	VSG Active Line 1.
	[23:12]	X	SGLINE2_5	VSG Active Line 2. (If No Second Line Is Needed, Set to Same as Line 1 or Maximum).
FF	[11:0]	X	SCP5_5	Vertical Sequence Change Position No.5 for Field 5.
	[23:12]	X	SCP6_5	Vertical Sequence Change Position No.6 for Field 5.

COMPLETE LISTING FOR REGISTER BANK 3

All vertical pattern group and vertical sequence registers are SCP updated. Default register values are undefined.

Table 74. XV7 and XV8 Pattern Group 0 (VPAT0) Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
00	[0]	X	XV7POL_0	VPAT0 XV7 Start Polarity
	[1]	X	XV8POL_0	VPAT0 XV8 Start Polarity
	[11:2]	X	UNUSED	Unused
	[23:12]	X	XV78LEN_0	Total Length of XV7 and XV8 Pattern for VPAT0
01	[11:0]	X	XV7TOG1_0	XV7 Toggle Position 1
	[23:12]	X	XV7TOG2_0	XV7 Toggle Position 2
02	[11:0]	X	XV7TOG3_0	XV7 Toggle Position 3
	[23:12]	X	XV8TOG1_0	XV8 Toggle Position 1
03	[11:0]	X	XV8TOG2_0	XV8 Toggle Position 2
	[23:12]	X	XV8TOG3_0	XV8 Toggle Position 3
04	[11:0]	X	XV7TOG4_0	XV7 Toggle Position 4
	[23:12]	X	XV8TOG4_0	XV8 Toggle Position 4
05	[23:0]	X	UNUSED	Unused
06	[23:0]	X	UNUSED	Unused
07	[23:0]	X	UNUSED	Unused

Table 75. XV7 and XV8 Pattern Group 1 (VPAT1) Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
08	[0]	X	XV7POL_1	VPAT1 XV7 Start Polarity
	[1]	X	XV8POL_1	VPAT1 XV8 Start Polarity
	[11:2]	X	UNUSED	Unused
	[23:12]	X	XV78LEN_1	Total Length of XV7 and XV8 Pattern for VPAT2
09	[11:0]	X	XV7TOG1_1	XV7 Toggle Position 1
	[23:12]	X	XV7TOG2_1	XV7 Toggle Position 2
0A	[11:0]	X	XV7TOG3_1	XV7 Toggle Position 3
	[23:12]	X	XV8TOG1_1	XV8 Toggle Position 1
0B	[11:0]	X	XV8TOG2_1	XV8 Toggle Position 2
	[23:12]	X	XV8TOG3_1	XV8 Toggle Position 3
0C	[11:0]	X	XV7TOG4_1	XV7 Toggle Position 4
	[23:12]	X	XV8TOG4_1	XV8 Toggle Position 4
0D	[23:0]	X	UNUSED	Unused
0E	[23:0]	X	UNUSED	Unused
0F	[23:0]	X	UNUSED	Unused

Table 76. XV7 and XV8 Pattern Group 2 (VPAT2) Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
10	[0]	X	XV7POL_2	VPAT2 XV7 Start Polarity
	[1]	X	XV8POL_2	VPAT2 XV8 Start Polarity
	[11:2]	X	UNUSED	Unused
	[23:12]	X	XV78LEN_2	Total Length of XV7 and XV8 Pattern for VPAT2
11	[11:0]	X	XV7TOG1_2	XV7 Toggle Position 1
	[23:12]	X	XV7TOG2_2	XV7 Toggle Position 2
12	[11:0]	X	XV7TOG3_2	XV7 Toggle Position 3
	[23:12]	X	XV8TOG1_2	XV8 Toggle Position 1
13	[11:0]	X	XV8TOG2_2	XV8 Toggle Position 2
	[23:12]	X	XV8TOG3_2	XV8 Toggle Position 3
14	[11:0]	X	XV7TOG4_2	XV7 Toggle Position 4
	[23:12]	X	XV8TOG4_2	XV8 Toggle Position 4
15	[23:0]	X	UNUSED	Unused
16	[23:0]	X	UNUSED	Unused
17	[23:0]	X	UNUSED	Unused

Table 77. XV7 and XV8 Pattern Group 3 (VPAT3) Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
18	[0]	X	XV7POL_3	VPAT3 XV7 Start Polarity
	[1]	X	XV8POL_3	VPAT3 XV8 Start Polarity
	[11:2]	X	UNUSED	Unused
	[23:12]	X	XV78LEN_3	Total Length of XV7 and XV8 Pattern for VPAT3
19	[11:0]	X	XV7TOG1_3	XV7 Toggle Position 1
	[23:12]	X	XV7TOG2_3	XV7 Toggle Position 2
1A	[11:0]	X	XV7TOG3_3	XV7 Toggle Position 3
	[23:12]	X	XV8TOG1_3	XV8 Toggle Position 1
1B	[11:0]	X	XV8TOG2_3	XV8 Toggle Position 2
	[23:12]	X	XV8TOG3_3	XV8 Toggle Position 3
1C	[11:0]	X	XV7TOG4_3	XV7 Toggle Position 4
	[23:12]	X	XV8TOG4_3	XV8 Toggle Position 4
1D	[23:0]	X	UNUSED	Unused
1E	[23:0]	X	UNUSED	Unused
1F	[23:0]	X	UNUSED	Unused

Table 78. XV7 and XV8 Pattern Group 4 (VPAT4) Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
20	[0]	X	XV7POL_4	VPAT4 XV7 Start Polarity
	[1]	X	XV8POL_4	VPAT4 XV8 Start Polarity
	[11:2]	X	UNUSED	Unused
	[23:12]	X	XV78LEN_4	Total Length of XV7 and XV8 Pattern for VPAT4
21	[11:0]	X	XV7TOG1_4	XV7 Toggle Position 1
	[23:12]	X	XV7TOG2_4	XV7 Toggle Position 2
22	[11:0]	X	XV7TOG3_4	XV7 Toggle Position 3
	[23:12]	X	XV8TOG1_4	XV8 Toggle Position 1
23	[11:0]	X	XV8TOG2_4	XV8 Toggle Position 2
	[23:12]	X	XV8TOG3_4	XV8 Toggle Position 3
24	[11:0]	X	XV7TOG4_4	XV7 Toggle Position 4
	[23:12]	X	XV8TOG4_4	XV8 Toggle Position 4
25	[23:0]	X	UNUSED	Unused
26	[23:0]	X	UNUSED	Unused
27	[23:0]	X	UNUSED	Unused

Table 79. XV7 and XV8 Pattern Group 5 (VPAT5) Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
28	[0]	X	XV7POL_5	VPAT5 XV7 Start Polarity
	[1]	X	XV8POL_5	VPAT5 XV8 Start Polarity
	[11:2]	X	UNUSED	Unused
	[23:12]	X	XV78LEN_5	Total Length of XV7 and XV8 Pattern for VPAT5
29	[11:0]	X	XV7TOG1_5	XV7 Toggle Position 1
	[23:12]	X	XV7TOG2_5	XV7 Toggle Position 2
2A	[11:0]	X	XV7TOG3_5	XV7 Toggle Position 3
	[23:12]	X	XV8TOG1_5	XV8 Toggle Position 1
2B	[11:0]	X	XV8TOG2_5	XV8 Toggle Position 2
	[23:12]	X	XV8TOG3_5	XV8 Toggle Position 3
2C	[11:0]	X	XV7TOG4_5	XV7 Toggle Position 4
	[23:12]	X	XV8TOG4_5	XV8 Toggle Position 4
2D	[23:0]	X	UNUSED	Unused
2E	[23:0]	X	UNUSED	Unused
2F	[23:0]	X	UNUSED	Unused

Table 80. XV7 and XV8 Pattern Group 6 (VPAT6) Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
30	[0]	X	XV7POL_6	VPAT6 XV7 Start Polarity
	[1]	X	XV8POL_6	VPAT6 XV8 Start Polarity
	[11:2]	X	UNUSED	Unused
	[23:12]	X	XV78LEN_6	Total Length of XV7 and XV8 Pattern for VPAT6
31	[11:0]	X	XV7TOG1_6	XV7 Toggle Position 1
	[23:12]	X	XV7TOG2_6	XV7 Toggle Position 2
32	[11:0]	X	XV7TOG3_6	XV7 Toggle Position 3
	[23:12]	X	XV8TOG1_6	XV8 Toggle Position 1
33	[11:0]	X	XV8TOG2_6	XV8 Toggle Position 2
	[23:12]	X	XV8TOG3_6	XV8 Toggle Position 3
34	[11:0]	X	XV7TOG4_6	XV7 Toggle Position 4
	[23:12]	X	XV8TOG4_6	XV8 Toggle Position 4
35	[23:0]	X	UNUSED	Unused
36	[23:0]	X	UNUSED	Unused
37	[23:0]	X	UNUSED	Unused

Table 81. XV7 and XV8 Pattern Group 7 (VPAT7) Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
38	[0]	X	XV7POL_7	VPAT7 XV7 Start Polarity
	[1]	X	XV8POL_7	VPAT7 XV8 Start Polarity
	[11:2]	X	UNUSED	Unused
	[23:12]	X	XV78LEN_7	Total Length of XV7 and XV8 Pattern for VPAT7
39	[11:0]	X	XV7TOG1_7	XV7 Toggle Position 1
	[23:12]	X	XV7TOG2_7	XV7 Toggle Position 2
3A	[11:0]	X	XV7TOG3_7	XV7 Toggle Position 3
	[23:12]	X	XV8TOG1_7	XV8 Toggle Position 1
3B	[11:0]	X	XV8TOG2_7	XV8 Toggle Position 2
	[23:12]	X	XV8TOG3_7	XV8 Toggle Position 3
3C	[11:0]	X	XV7TOG4_7	XV7 Toggle Position 4
	[23:12]	X	XV8TOG4_7	XV8 Toggle Position 4
3D	[23:0]	X	UNUSED	Unused
3E	[23:0]	X	UNUSED	Unused
3F	[23:0]	X	UNUSED	Unused

Table 82. XV7 and XV8 Pattern Group 8 (VPAT8) Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
40	[0]	X	XV7POL_8	VPAT8 XV7 Start Polarity
	[1]	X	XV8POL_8	VPAT8 XV8 Start Polarity
	[11:2]	X	UNUSED	Unused
	[23:12]	X	XV78LEN_8	Total Length of XV7 and XV8 Pattern for VPAT8
41	[11:0]	X	XV7TOG1_8	XV7 Toggle Position 1
	[23:12]	X	XV7TOG2_8	XV7 Toggle Position 2
42	[11:0]	X	XV7TOG3_8	XV7 Toggle Position 3
	[23:12]	X	XV8TOG1_8	XV8 Toggle Position 1
43	[11:0]	X	XV8TOG2_8	XV8 Toggle Position 2
	[23:12]	X	XV8TOG3_8	XV8 Toggle Position 3
44	[11:0]	X	XV7TOG4_8	XV7 Toggle Position 4
	[23:12]	X	XV8TOG4_8	XV8 Toggle Position 4
45	[23:0]	X	UNUSED	Unused
46	[23:0]	X	UNUSED	Unused
47	[23:0]	X	UNUSED	Unused

Table 83. XV7 and XV8 Pattern Group 9 (VPAT9) Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
48	[0]	X	XV7POL_9	VPAT9 XV7 Start Polarity
	[1]	X	XV8POL_9	VPAT9 XV8 Start Polarity
	[11:2]	X	UNUSED	Unused
	[23:12]	X	XV78LEN_9	Total Length of XV7 and XV8 Pattern for VPAT9
49	[11:0]	X	XV7TOG1_9	XV7 Toggle Position 1
	[23:12]	X	XV7TOG2_9	XV7 Toggle Position 2
4A	[11:0]	X	XV7TOG3_9	XV7 Toggle Position 3
	[23:12]	X	XV8TOG1_9	XV8 Toggle Position 1
4B	[11:0]	X	XV8TOG2_9	XV8 Toggle Position 2
	[23:12]	X	XV8TOG3_9	XV8 Toggle Position 3
4C	[11:0]	X	XV7TOG4_9	XV7 Toggle Position 4
	[23:12]	X	XV8TOG4_9	XV8 Toggle Position 4
4D	[23:0]	X	UNUSED	Unused
4E	[23:0]	X	UNUSED	Unused
4F	[23:0]	X	UNUSED	Unused

Table 84. XV7 and XV8 Vertical Sequence 0 Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
50	[0]	X	HOLD_0	0: Vertical Masking Operation, 1: Hold Area instead of Vertical Masking
	[11:1]	X	UNUSED	Unused
	[23:12]	X	XV78START_0	Start Position for XV7 and XV8
51	[11:0]	X	XV78REPO_0	Number of Selected XV7, XV8 Repetitions for Odd Lines
	[23:12]	X	XV78REPE_0	Number of Selected XV7, XV8 Repetitions for Even Lines
52	[0]	X	XV78HOLDEN_0	0: No Hold Area for XV7 and XV8,1: Enable Hold Area for XV7 and XV8
	[23:1]	X	UNUSED	Unused
53	[23:0]	X	UNUSED	Unused

Table 85. XV7 and XV8 Vertical Sequence 1 Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
54	[0]	X	HOLD_1	0: Vertical Masking Operation, 1: Hold Area instead of Vertical Masking
	[11:1]	X	UNUSED	Unused
	[23:12]	X	XV78START_1	Start Position for XV7 and XV8
55	[11:0]	X	XV78REPO_1	Number of Selected XV7, XV8 Repetitions for Odd Lines
	[23:12]	X	XV78REPE_1	Number of Selected XV7, XV8 Repetitions for Even Lines
56	[0]	X	XV78HOLDEN_1	0: No Hold Area for XV7 and XV8, 1: Enable Hold Area for XV7 and XV8
	[23:1]	X	UNUSED	Unused
57	[23:0]	X	UNUSED	Unused

Table 86. XV7 and XV8 Vertical Sequence 2 Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
58	[0]	X	HOLD_2	0: Vertical Masking Operation, 1: Hold Area instead of Vertical Masking
	[11:1]	X	UNUSED	Unused
	[23:12]	X	XV78START_2	Start Position for XV7 and XV8
59	[11:0]	X	XV78REPO_2	Number of Selected XV7, XV8 Repetitions for Odd Lines
	[23:12]	X	XV78REPE_2	Number of Selected XV7, XV8 Repetitions for Even Lines
5A	[0]	X	XV78HOLDEN_2	0: No Hold Area for XV7 and XV8, 1: Enable Hold Area for XV7 and XV8
	[23:1]	X	UNUSED	Unused
5B	[23:0]	X	UNUSED	Unused

Table 87. XV7 and XV8 Vertical Sequence 3 Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
5C	[0]	X	HOLD_3	0: Vertical Masking Operation, 1: Hold Area instead of Vertical Masking
	[11:1]	X	UNUSED	Unused
	[23:12]	X	XV78START_3	Start Position for XV7 and XV8
5D	[11:0]	X	XV78REPO_3	Number of Selected XV7, XV8 Repetitions for Odd Lines
	[23:12]	X	XV78REPE_3	Number of Selected XV7, XV8 Repetitions for Even Lines
5E	[0]	X	XV78HOLDEN_3	0: No Hold Area for XV7 and XV8, 1: Enable Hold Area for XV7 and XV8
	[23:1]	X	UNUSED	Unused
5F	[23:0]	X	UNUSED	Unused

Table 88. XV7 and XV8 Vertical Sequence 4 Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
60	[0]	X	HOLD_4	0: Vertical Masking Operation, 1: Hold Area instead of Vertical Masking
	[11:1]	X	UNUSED	Unused
	[23:12]	X	XV78START_4	Start Position for XV7 and XV8
61	[11:0]	X	XV78REPO_4	Number of Selected XV7, XV8 Repetitions for Odd Lines
	[23:12]	X	XV78REPE_4	Number of Selected XV7, XV8 Repetitions for Even Lines
62	[0]	X	XV78HOLDEN_4	0: No Hold Area for XV7 and XV8, 1: Enable Hold Area for XV7 and XV8
	[23:1]	X	UNUSED	Unused
63	[23:0]	X	UNUSED	Unused

Table 89. XV7 and XV8 Vertical Sequence 5 Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
64	[0]	X	HOLD_5	0: Vertical Masking Operation, 1: Hold Area instead of Vertical Masking
	[11:1]	X	UNUSED	Unused
	[23:12]	X	XV78START_5	Start Position for XV7 and XV8
65	[11:0]	X	XV78REPO_5	Number of Selected XV7, XV8 Repetitions for Odd Lines
	[23:12]	X	XV78REPE_5	Number of Selected XV7, XV8 Repetitions for Even Lines
66	[0]	X	XV78HOLDEN_5	0: No Hold Area for XV7 and XV8, 1: Enable Hold Area for XV7 and XV8
	[23:1]	X	UNUSED	Unused
67	[23:0]	X	UNUSED	Unused

Table 90. XV7 and XV8 Vertical Sequence 6 Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
68	[0]	X	HOLD_6	0: Vertical Masking Operation, 1: Hold Area instead of Vertical Masking
	[11:1]	X	UNUSED	Unused
	[23:12]	X	XV78START_6	Start Position for XV7 and XV8
69	[11:0]	X	XV78REPO_6	Number of Selected XV7, XV8 Repetitions for Odd Lines
	[23:12]	X	XV78REPE_6	Number of Selected XV7, XV8 Repetitions for Even Lines
6A	[0]	X	XV78HOLDEN_6	0: No Hold Area for XV7 and XV8, 1: Enable Hold Area for XV7 and XV8
	[23:1]	X	UNUSED	Unused
6B	[23:0]	X	UNUSED	Unused

Table 91. XV7 and XV8 Vertical Sequence 7 Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
6C	[0]	X	HOLD_7	0: Vertical Masking Operation, 1: Hold Area instead of Vertical Masking
	[11:1]	X	UNUSED	Unused
	[23:12]	X	XV78START_7	Start Position for XV7 and XV8
6D	[11:0]	X	XV78REPO_7	Number of Selected XV7, XV8 Repetitions for Odd Lines
	[23:12]	X	XV78REPE_7	Number of Selected XV7, XV8 Repetitions for Even Lines
6E	[0]	X	XV78HOLDEN_7	0: No Hold Area for XV7 and XV8, 1: Enable Hold Area for XV7 and XV8
	[23:1]	X	UNUSED	Unused
6F	[23:0]	X	UNUSED	Unused

Table 92. XV7 and XV8 Vertical Sequence 8 Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
70	[0]	X	HOLD_8	0: Vertical Masking Operation, 1: Hold Area instead of Vertical Masking
	[11:1]	X	UNUSED	Unused
	[23:12]	X	XV78START_8	Start Position for XV7 and XV8
71	[11:0]	X	XV78REPO_8	Number of Selected XV7, XV8 Repetitions for Odd Lines
	[23:12]	X	XV78REPE_8	Number of Selected XV7, XV8 Repetitions for Even Lines
72	[0]	X	XV78HOLDEN_8	0: No Hold Area for XV7 and XV8, 1: Enable Hold Area for XV7 and XV8
	[23:1]	X	UNUSED	Unused
73	[23:0]	X	UNUSED	Unused

Table 93. XV7 and XV8 Vertical Sequence 9 Registers

Address	Data Bit Content	Default Value	Register Name	Register Description
74	[0]	X	HOLD_9	0: Vertical Masking Operation, 1: Hold Area instead of Vertical Masking
	[11:1]	X	UNUSED	Unused
	[23:12]	X	XV78START_9	Start Position for XV7 and XV8
75	[11:0]	X	XV78REPO_9	Number of Selected XV7, XV8 Repetitions for Odd Lines
	[23:12]	X	XV78REPE_9	Number of Selected XV7, XV8 Repetitions for Even Lines
76	[0]	X	XV78HOLDEN_9	0: No Hold Area for XV7 and XV8, 1: Enable Hold Area for XV7 and XV8
	[23:1]	X	UNUSED	Unused
77	[23:0]	X	UNUSED	Unused

OUTLINE DIMENSIONS

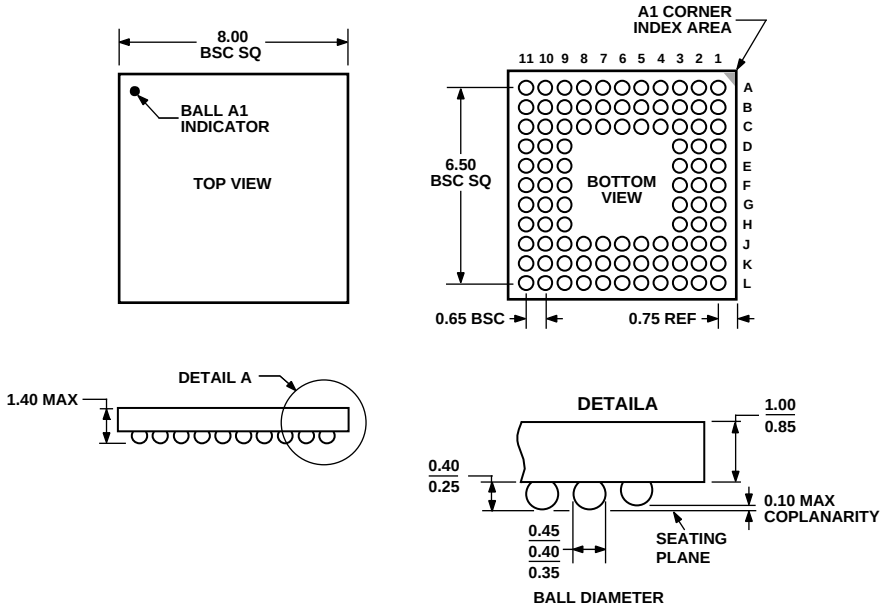


Figure 78. 96-Lead Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-96)
Dimensions shown in millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Option
AD9925BBCZ[1]	–25°C to +85°C	CSP_BGA	BC-96
AD9925BBCZRL[1]	–25°C to +85°C	CSP_BGA Tape and Reel	BC-96

[1] Z = Pb-free part.

NOTES

NOTES

D04637–0–10/04(A)