PM73122/PM8315

AAL1GATOR-32/TEMUX

AAL1GATOR-32/TEMUX DEVELOPMENT KIT

PRELIMINARY

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REVISION HISTORY

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2	November 2000	COMET-QUAD details added.
3	December 2000	Registers in EEPROM (Table 3, register 0x28 and 0x2A) changed for microprocessor bus timing.
4	June 2001	Updated COMET-QUAD analog decoupling (C45, C48, C54, C65) in the schematics. Updated power calculations

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1 INTRODUCTION

1.1 Purpose

The purpose of the AAL1gator-32/TEMUX Development Kit is to provide software designers with a platform on which to implement and test software for the PM73122 AAL1gator-32 and PM8315 TEMUX, as well as the PM7350 S/UNI-DUPLEX, and PM4354 COMET-QUAD. Customers planning to use other variants of the AAL1gator device (i.e. AAL1gator-8 or AAL1gator-4) can also use this development kit by porting the core functions to another platform using a different AAL1gator variant.

1.2 Scope

This document details the hardware design of the AAL1gator-32/TEMUX Development Kit. This document includes a detailed description of each of the functional blocks of the kit, as well as schematics, bill of materials and CPLD code for the design. The AAL1gator-32/TEMUX Development Kit system is complete with software to setup the hardware. The software is written in ANSI C for the VxWorks operating system. Details of the software are available in the AAL1gator-32/TEMUX Development Kit Platform document [1].

1.3 Application

Traditional enterprise networks have evolved to comprise two physically separate networks – one for data and one for voice/video traffic. For example, Asynchronous Transfer Mode (ATM) or Frame Relay may be used for data, while traditional copper T1 connections are used for linking voice/private branch exchange (PBX) and videoconferencing devices together. PMC-Sierra's customers want a scalable solution that allows them to easily and efficiently move onto a single physical network by integrating voice, video, and data traffic. The solution is to carry constant bit rate (CBR) or "circuit" traffic over Asynchronous Transfer Mode (ATM) networks. The ATM Forum has defined a circuit emulation service (CES) specification that provides a virtual circuit connection emulating the characteristics of a real, constant-bit-rate, dedicated-bandwidth circuit. PMC-Sierra's PM73122 AAL1gator-32 implements this CES functionality in silicon.

2 FEATURES

- Provides full access to the AAL1gator-32, TEMUX, S/UNI-DUPLEX, and COMET-QUAD devices.
- 5V PCI Card Compatible.
- Internal Diagnostic Loopbacks of the TEMUX, COMET-QUAD, AAL1gator-32, and S/UNI-DUPLEX.
- A high-speed LVDS Interface capable of data rates up to 200 MB/s.
- Supports 4 T1, 4 E1, or 1 DS3 link for transport over ATM.

3 GENERAL DESCRIPTION

A block diagram for the AAL1gator-32/TEMUX Development Kit is shown in Figure 1. The T1/E1/DS3 ports of the design are contained within the T1/E1 Line Interface block and the DS3 Line Interface block. Within the T1/E1 Line Interface block 4 T1 or E1 channels interface to the PM4354 COMET-QUAD through 8 bantam connectors and line protection circuitry. PMC-Sierra's PM4354 COMET-QUAD is a four channel combined T1 or E1 transceiver and framer. The system side of the COMET-QUAD communicates with the PM73122 AAL1gator-32 using framed T1/E1 clock and data.

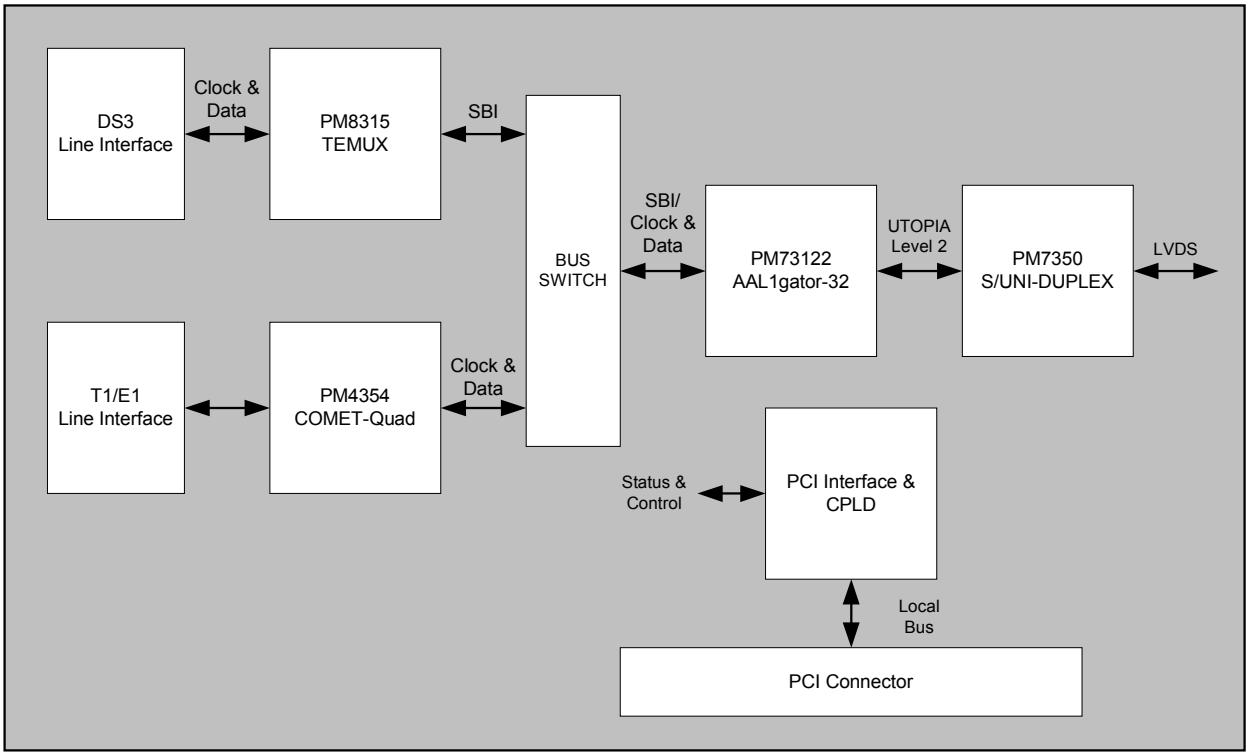
Within the DS3 Line Interface block one DS3 channel connects to the PM8315 TEMUX through 2 SMB connectors, line protection circuitry and a line interface IC. PMC-Sierra's PM8315 TEMUX is configured as a DS3 framer and SBI bus interface within this design. The TEMUX communicates with the DS3 Line Interface IC on the line side, and the PM73122 AAL1gator-32 on the system side.

Note in Figure 1 that both the COMET-QUAD and the TEMUX communicate with the AAL1gator-32 through a bus switch. The COMET-QUAD uses clock and data lines to communicate with the AAL1gator-32 and the TEMUX uses PMC-Sierra's Scalable Bandwidth Interconnect (SBI) bus. The COMET-QUAD and TEMUX cannot communicate with the AAL1gator-32 simultaneously because two different buses are used that share the same pins. Therefore, a bus switch is used and reconfiguration of the AAL1gator-32 is required when switching between DS3 and T1/E1.

As shown in Figure 1, the AAL1gator-32 communicates with PMC-Sierra's PM7350 S/UNI-DUPLEX via a UTOPIA high-speed parallel bus. The S/UNI-DUPLEX interfaces the UTOPIA bus to a high speed Low Voltage Differential Signal (LVDS) serial link. This LVDS link is suitable for transmission across a cable and can interface with another AAL1gator-32/TEMUX Development Kit board or any other S/UNI-DUPLEX configured with a UTOPIA interface.

A PCI Interface chip allows the card to be controlled and monitored via the PCI bus.

Figure 1 AAL1gator-32/TEMUX Development Kit Block Diagram



4 BLOCK DESCRIPTION

The following sections describe the function of each hardware block shown in Figure 1.

4.1 PCI Bridge

The PCI Bridge used is PLX Technology's PCI9050 PCI Bus Target Interface Chip. The PCI9050 provides a target only interface, and as such does not initiate PCI bus transactions. The local bus interface of the PCI9050 is generic and very flexible supporting: 8, 16, and 32-bit transfers, multiplexed or non-multiplexed modes, big or little endian, and clock rates asynchronous to the PCI bus up to 40MHz. The local bus is partitioned into 4 distinct user-definable address spaces that can be configured independently. The timing of each address space is specifiable via a set of programmable wait states as well as supporting a ready signal used to insert additional wait states. Please refer to the PCI9050 datasheet [2] for more information.

The local address spaces are allocated in the following fashion:

Table 1 PCI9050 Local Address Space Allocation

Address Space	Function
0	AAL1gator-32
1	TEMUX
2	COMET-QUAD
3	S/UNI-DUPLEX

All four address spaces are configured as 32-bit non-multiplexed, big endian, non-burst, and non-prefetchable. Although the devices on the microprocessor bus have only a 16- or 8-bit data bus, the PCI9050 is configured as a 32-bit bus to simplify the timing of the hardware design. Also, the devices do not support burst mode transfers and therefore bursting is disabled. Prefetching is not possible as some of the registers have read side effects (i.e. interrupt status registers).

The local bus is clocked at 33MHz by looping the buffered PCI clock output (BCLKO) available from the PCI9050 back to the local bus clock input.

4.2 SEEP

The NM93CS46 Serial EEPROM from National Semiconductor is used to store configuration information for the PCI9050 interface chip. This specific SEEP (or equivalent) is required by the PCI9050 because it supports sequential read operations. The SEEP can be programmed over the PCI bus through a rudimentary interface provided by the PCI9050 or using an EEPROM programmer.

The SEEP is 1Kbit deep, 800 bits of which are occupied by the PCI9050 configuration data, leaving 224 bits (28 bytes) unused.

Refer to the PCI9050 datasheet [2] for information on the format of the configuration data stored in the SEEP.

4.3 Power Supply

Power requirements of the board are +5V, +3.3V and +2.5V. +5V is available from the PCI bus through the PCI edge connector and is used to power the PCI9050 PCI Interface chip. +3.3V is available from the PCI bus, but is regulated from +5V in order to provide cleaner power. +2.5V is provided by a regulator using +3.3V regulated power. LEDs mounted to the card bracket are used to indicate power status.

4.4 CPLD

A Xilinx XC95144XL CPLD provides the miscellaneous logic required for the board. A schematic representation of the CPLD logic is shown in Figure 2. This logic is written in VHDL and the code is given in appendix D. The timing requirements of the design require a 7.5 ns CPLD. There are address and data lines routed to the CPLD from the PCI9050 such that registers can be created within the CPLD and modified via the PCI interface.

The CPLD logic controls the control lines of the microprocessor port of each PMC-Sierra chip. Yellow LEDs indicate an interrupt from each of the chips. The reset signal RSTB is wired such that the MAX700 Power-supply Monitor or the PCI9050 chip can issue a reset to the board. Also, as TRSTB must go low at least once after reset, TRSTB can be controlled via the JTAG header and goes low with RSTB.

Clock dividers inside the CPLD divide down an external network clock for use in the AAL1gator-32 for synchronous residual timestamp (SRTS) support. A 2.43 MHz clock is required for SRTS, which can be derived from a 155.52 MHz network clock supplied through a SMA connector. The AAL1gator-32 has an

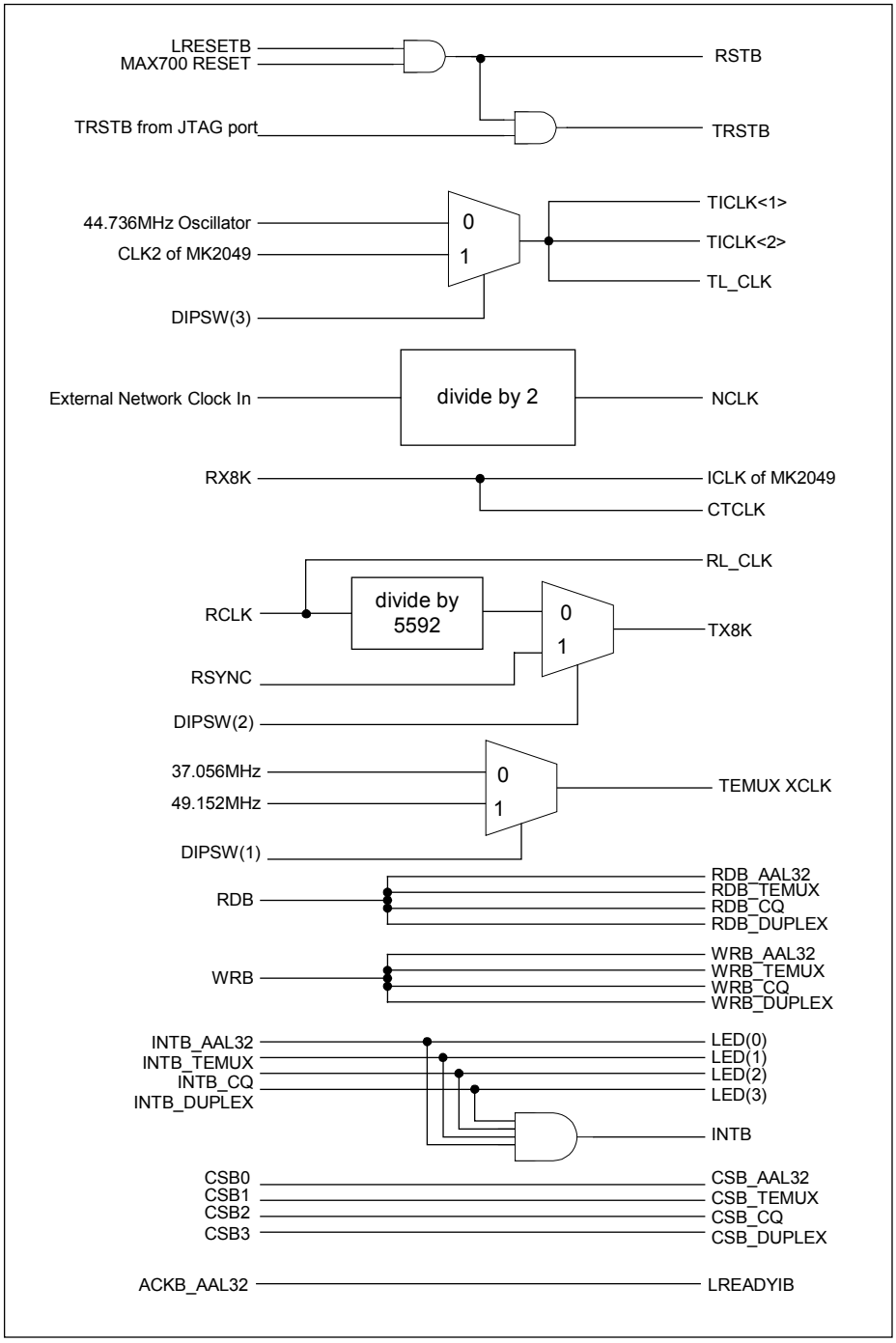
internal divider but it can only divide a 77.76 MHz clock down to 2.43 MHz, hence the need for another divider within the CPLD.

The other CPLD divider divides down the DS3 RCLK from 44.736 MHz to 8 kHz so that it can be transmitted across the LVDS link and used as a timing reference at the far end. Similarly, the development kit is capable of receiving an 8 kHz reference from an external timing source across the LVDS link and multiply it up to a nominal rate of 44.736 MHz for clocking out the DS3 signal. The CPLD is connected to a MK2049 phase locked loop to implement this clock multiplier.

A DIP switch is used to select between the two different XCLK rates required by the TEMUX. The switch is also used to select other clocking options as shown in Figure 2.

The CPLD is in-system programmable and is programmed via its JTAG port header.

Figure 2 CPLD Logic



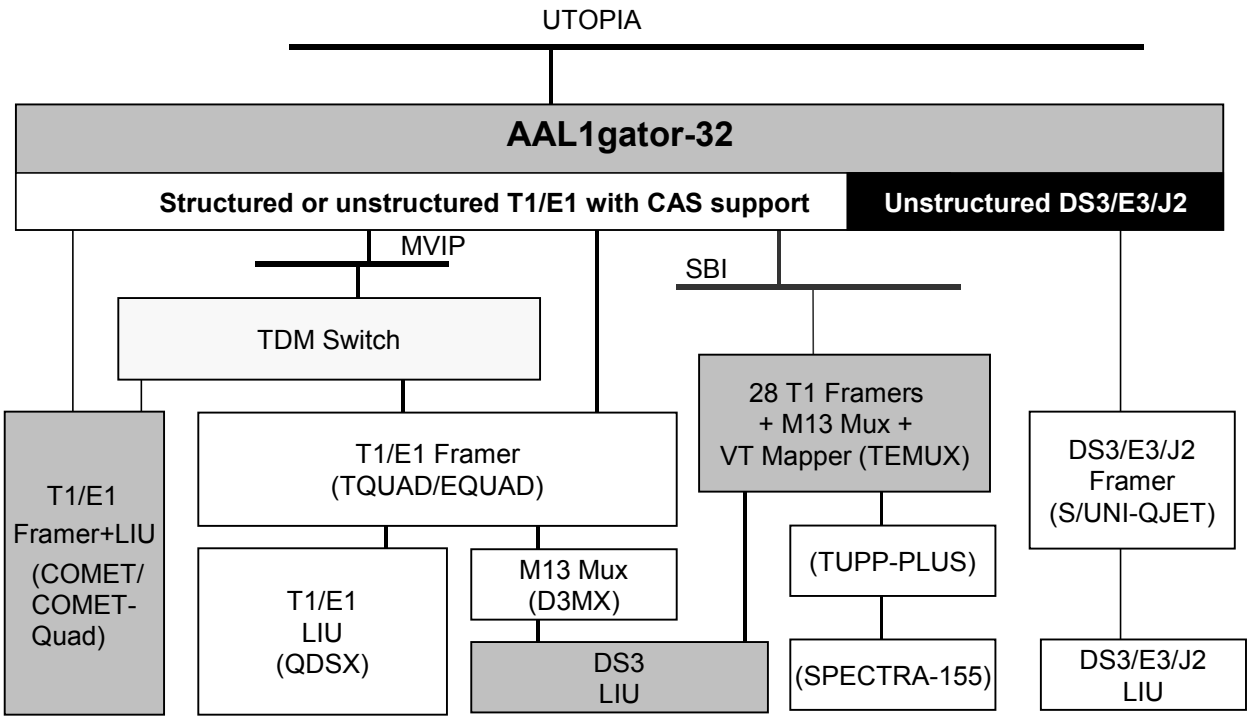
4.5 PM73122 AAL1gator-32

The PM73122 AAL1 Segmentation and Reassembly (SAR) Processor (AAL1gator-32) is a monolithic single chip device that provides T1, E1, E3, or DS3 line interface access to an ATM Adaptation Layer One (AAL1) Constant Bit Rate (CBR) ATM network. It arbitrates access to an external SRAM for storage of configuration, user, and statistics data. Some of the device's important functionality is as follows:

- Compliant with the ATM Forum's Circuit Emulation Services (CES) specification (AF-VTOA-0078), and the ITU-T I.363.1
- Supports Dynamic Bandwidth Circuit Emulation Services (DBCES). Compliant with the ATM Forum's DBCES specification (AF-VTOA-0085).
- Supports idle channel detection via processor intervention, CAS signaling, or data pattern detection.
- Provides idle channel indication on a per channel basis.
- Provides AAL1 segmentation and reassembly of 16 individual E1 or T1 lines in the direct low speed mode, 8 H-MVIP lines at 8 Mb/s in the H-MVIP mode, or 2 E3 or DS3 lines in the high speed mode.
- Using the Scalable Bandwidth Interconnect (SBI) Interface, provides AAL1 segmentation and reassembly of up to 32 T1, E1, links, or 2 DS3 links.
- Provides a standard UTOPIA level 2 Interface which optionally supports parity and runs up to 52 MHz. The following modes are supported:
    - 16-bit Level 2, Multi-Phy Mode (MPHY)
    - 8/16-bit Level 1, SPHY
    - 8-bit Level 1, ATM Master
- Provides an optional 8/16-bit Any-PHY slave interface.
- Supports up to 1024 Virtual Channels (VC).
- Supports n x 64 (consecutive channels) and m x 64 (non-consecutive channels) structured data format.

Figure 3 indicates the ways in which an AAL1gator-32 can be used to connect to T1/E1 or DS3/E3/J2 line interfaces. The shaded devices represent the configurations used in the AAL1gator-32/TEMUX Development Kit.

Figure 3 AAL1gator-32 Configurations



In this design one AAL1gator-32 is used to interface with either one TEMUX or one COMET-QUAD through a bus switch. A bus switch is used because the AAL1gator-32 communicates with the TEMUX using SBI mode, and the COMET-QUAD via Direct Low Speed mode. These two modes are not supported simultaneously by the AAL1gator-32 and therefore a bus switch is needed to switch the common system side signals. When the AAL1gator-32/TEMUX Development Kit is configured for DS3 operation the AAL1gator-32 and TEMUX interface via the SBI bus to support 28 structured/unstructured T1s or 21 structured/unstructured E1s. When the AAL1gator-32/TEMUX Development Kit is configured for T1/E1 operation the AAL1gator-32 communicates with the COMET-QUAD using the clock and data signals from 4 T1s or 4 E1s.

For a more detailed description of the AAL1gator-32, please refer to [3] of the references.

4.6 PM8315 TEMUX

The PM8315 TEMUX is an integrated circuit that combines 28 T1 framers, 21 E1 framers, a SONET/SDH VT1.5/V2/TU-11/TU-12 bit asynchronous mapper and a full-featured M13 multiplexer with DS3 framer. The TEMUX also contains a SONET/SDH DS3 mapper for terminating DS3 multiplexed T1 streams, SONET/SDH mapped T1 streams or SONET/SDH mapped E1 streams.

Within the AAL1gator-32/TEMUX Development Kit the TEMUX is configured to support a byte serial Scalable Bandwidth Interconnect (SBI) bus interconnection to the AAL1gator-32. On the line side the TEMUX is configured to support the dual-rail DS3 signals from the DS3 line interface unit. An 8-bit microprocessor bus interface provides configuration, control, and status monitoring.

For more information about the TEMUX, please refer to [4] of the references.

4.7 PM4354 COMET-QUAD

The PM4354 Four Channel Combined E1/T1/J1 Transceiver and Framer (COMET-QUAD) is a feature-rich monolithic integrated circuit suitable for use in long haul and short haul T1, J1 and E1 systems with a minimum of external circuitry. The COMET-QUAD is software configurable, allowing feature selection without changes to external wiring.

Analog circuitry is provided to allow direct reception of long haul E1 and T1/J1 compatible signals typically with up to 43 dB cable loss at 1024 kHz (E1) and up to 44 dB cable loss at 772 kHz (T1/J1) using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required.

The COMET-QUAD recovers clock and data from the line and frames to incoming data. In T1 mode, it can frame to SF and ESF signal formats. In E1 mode, the COMET-QUAD frames to basic G.704 E1 signals and CRC-4 multiframe alignment signals, and automatically performs the G.706 interworking procedure. AMI, HDB3 and B8ZS line codes are supported.

The COMET-QUAD supports detection of various alarm conditions such as loss of signal, pulse density violation, Red alarm, Yellow alarm, and AIS alarm in T1 mode and loss of signal, loss of frame, loss of signaling multiframe and loss of CRC multiframe in E1 mode. The COMET-QUAD also supports reception of remote alarm signal, remote multiframe alarm signal, and alarm indication signal in E1 mode. The presence of Yellow and AIS patterns in T1 mode and remote alarm and AIS patterns in E1 mode is detected and indicated. In T1 mode, the COMET-QUAD integrates Yellow, Red, and AIS alarms as per industry specifications. In E1 mode, the COMET-QUAD integrates Red and AIS alarms.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, line code violations, and loss of frame events are provided in T1 mode. In E1 mode, CRC-4 errors, far end block errors, framing bit errors, and line code violation are monitored and accumulated.

In the transmit path, the COMET-QUAD supports signaling insertion, idle code substitution, digital milliwatt tone substitution, data inversion, and zero code suppression on a per-channel basis. Zero code suppression may be configured to Bell (bit 7), GTE, or DDS standards, and can also be disabled. Transmit side data and signaling trunk conditioning is also provided. Signaling bit transparency from the backplane may be enabled.

Each channel of the COMET-QUAD can generate a low jitter transmit clock from a variety of clock references, and also provides jitter attenuation in the receive path. A low jitter recovered T1 clock can be routed outside the COMET-QUAD for network timing applications.

Serial PCM interfaces to each T1/E1 framer allow 1.544 Mbit/s or 2.048 Mbit/s backplane receive/backplane transmit system interfaces to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic.

For synchronous backplane systems, 8.192 Mbit/s H-MVIP interfaces are provided for access to PCM data, channel associated signaling (CAS) and common channel signaling (CCS) for each T1 or E1. The CCS signaling H-MVIP interface is independent of the 64 Kbit/s PCM and CAS H-MVIP access. The use of the H-MVIP interface requires that common clocks and frame pulse be used along with T1/E1 elastic stores.

The COMET-QUAD is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be masked and acknowledged through the microprocessor interface.

For further information, please see the COMET-QUAD Datasheet [5].

4.8 PM7350 S/UNI-DUPLEX

The PM7350 S/UNI-DUPLEX is a monolithic integrated circuit typically used for traffic concentration within a Digital Subscriber Line Access Multiplexer (DSLAM). The DUPLEX is ATM specific and it exchanges contiguous 53 byte cells with PHY devices. The PHY interface can be either clocked serial data or SCI-PHY/Any-PHY.

With a clocked serial data configuration up to sixteen channels are supported. In the AAL1gator-32/TEMUX Development Kit, however, UTOPIA Level 2 is used at this interface.

All cell streams are multiplexed into a high-speed serial stream. The high-speed interfaces use NRZ data-only differential signals compatible with LVDS levels. The internal transmit clock is synthesized from a lower frequency reference. An extended cell format provides four extra bytes for the encoding of flow control, timing reference, PHY identification and link maintenance information. A redundant link is provided to allow connection to two cell processing cards.

A microprocessor port provides access to internal configuration and monitoring registers. The port may also be used to insert and extract cells in support of a control channel.

For further information, please see the S/UNI-DUPLEX Datasheet PMC-1980581 [6].

5 DESIGN ISSUES

The following sections describe detailed design considerations of the reference design.

5.1 AAL1gator-32 Design Considerations

5.1.1 Line Interface

The line interface block of the AAL1gator-32 is responsible for passing TDM data to the AAL1 Segmentation and Reassembly Processor. There are 4 possible options, which are selected using the LINE_MODE pins: Direct Low Speed Mode, H-MVIP Mode, SBI Mode, and High Speed Mode. The AAL1gator-32 uses Low Speed Mode to communicate with the COMET-QUAD. In Low Speed Mode the AAL1gator-32 can support up to 16 structured or unstructured T1/E1 links. H-MVIP mode can also be used to communicate with eight COMET-QUADs allowing use of all 32 links within the AAL1gator-32. H-MVIP Mode, however, does not allow the use of unstructured data formats.

SBI Mode is used to communicate with the TEMUX. Because the AAL1gator-32 Line Interface is configured in both SBI Mode and Direct Low Speed Mode within this design, a bus switch and jumper are required. The jumper configures the LINE_MODE0 pin of the AAL1gator-32 for either Low Speed (0) mode or SBI (1), and the bus switch switches the pins that are common to both bus types.

5.1.2 UTOPIA Interface

The AAL1gator-32 UTOPIA Interface manages and responds to all control signals on the UTOPIA bus. The following UTOPIA modes are supported:

- UTOPIA Level 1 ATM Master (8-bit only)
- UTOPIA Level 1 8/16-bit SPHY
- UTOPIA Level 2 Multi-phy Mode (MPHY)
- 8/16-bit Any-PHY Slave

The AAL1gator-32/TEMUX Development Kit is configured to run with a 25MHz UTOPIA Level 2 bus. The S/UNI-DUPLEX is configured as the bus master, and the AAL1gator-32 is configured as a bus slave. Because the S/UNI-DUPLEX can only run at up to 33 MHz in UTOPIA Level 2 Master mode, the oscillator must be less than or equal to 33 MHz (but large enough to satisfy the required

bandwidth of the bus) in order to run the AAL1gator-32 in UTOPIA Level 2 Slave mode.

5.1.3 SRAM

The AAL1gator-32 arbitrates access to two external 256K x 18 bit SRAMs for storage of configuration, user, and statistic data. The AAL1gator-32 memory interface is timed by SYSCLK, which is a 38.88MHz clock. There are two possible choices for the external SRAM: pipelined synchronous SRAM or pipelined ZBT SRAM. Standard Synchronous SRAM can be used in most applications. For high performance applications where many RAM accesses are necessary (such as many partial cell VCs), Zero Bus Turnaround (ZBT) SRAM should be used. ZBT RAM utilizes more bus bandwidth by eliminating the need to insert deselect cycles when the device is switched from read to write cycles. The AAL1gator-32/TEMUX Development Kit uses ZBT SRAM so that maximum performance can be obtained if needed.

5.1.4 Microprocessor Interface

The Microprocessor Interface provides access to normal mode registers and memory-mapped registers of the AAL1gator-32. The AAL1gator-32 microprocessor interface data and address buses are connected to the PCI9050 PCI Interface chip and the other signals connect through the CPLD for chip select decoding and then to the PCI9050. The microprocessor interface is configured as a non-multiplexed bus by pulling the ALE input high.

5.2 S/UNI-DUPLEX Design Considerations

5.2.1 Parallel Bus Interface

The SCI-PHY/Any-PHY Interface (SCIANY pin) input selects either parallel bus or a clocked serial data interface to the S/UNI-DUPLEX. To configure the S/UNI-DUPLEX for a UTOPIA Level 2 interface this pin must be logic high. The parallel bus interface supports three types of buses: UTOPIA Level 2, SCI-PHY, and Any-PHY. In this design UTOPIA Level 2 is used, although the other two types will also work.

The S/UNI-DUPLEX interface is configured as 16-bit UTOPIA Level 2 master by setting the IBUS8, OBUS8, IANYPHY, and OANYPHY inputs low, and the IMASTER and OMASTER inputs high.

5.2.2 LVDS Connections

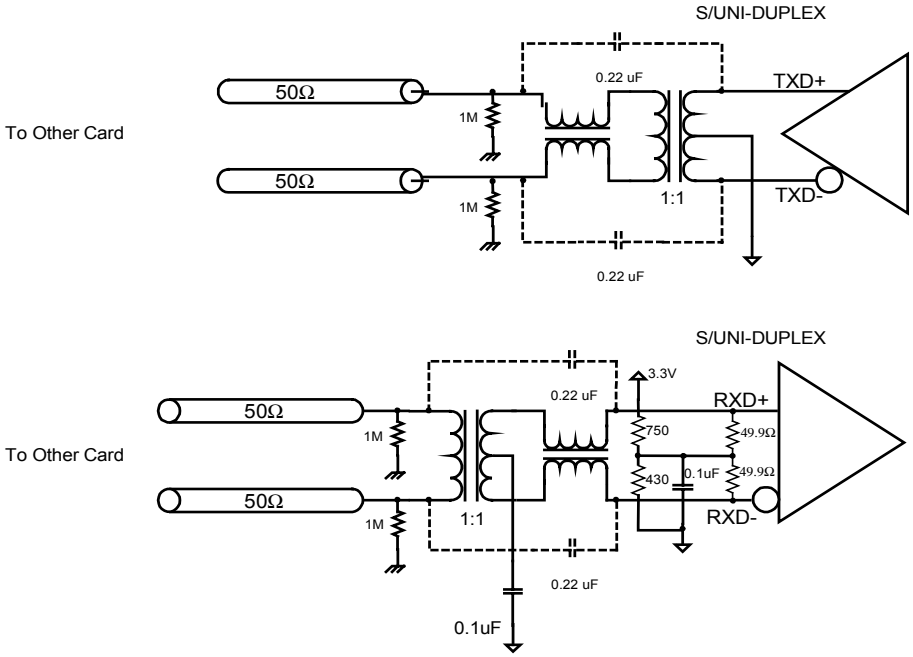
The LVDS differential signals should be routed together such that any coupling on the TX/RX path is common-mode and not differential. The two traces that form a differential TX/RX path should have equal trace lengths from the chip to the connector. Traces for the LVDS signals should be 50Ω controlled impedance.

The termination scheme used in the LVDS section of the development kit is shown in Figure 4. Two additional termination methods are possible for these LVDS signals: capacitive coupling and transformer coupling.

Capacitive coupling, as indicated by the dashed lines offers a low cost, low board space alternative for LVDS signals that originate from shelves on the same ground system. To use the capacitive coupling option, do not install the transformers. Install the 0.22µF and 1MΩ resistors instead.

For shelf to shelf termination where the shelves are on different ground systems, transformers are required to provide isolation. Common mode chokes are also used to reduce the amount of radiated and received electromagnetic interference (EMI). Only one end of the connection requires transformers, the other can use capacitive coupling. However, when connecting two AAL1gator-32/TEMUX Development Kits both boards could be transformer coupled or capacitively coupled.

Figure 4 LVDS Termination Scheme



In all termination methods, the LVDS receive signals are terminated by two 49.9Ω resistors and a 0.1uF capacitor. This termination network should be placed as physically close to the S/UNI-DUPLEX as possible.

5.2.3 Power Supply

During power-up, the BIAS pin must be equal to or greater than the voltage on the VDD pins. This is accomplished by the configuration of the voltage regulators. The voltage on the BIAS pin is also the same one used to regulate the VDD voltage. Therefore, the worst case is that the regulator malfunctions and shorts, which still leaves the BIAS pin equal to VDD. Also, an extra protection diode is used to limit the VDD to a maximum of 0.5V above the BIAS voltage.

Analog power pins QAVD, CAVD, RAVD and TAVD must be applied after VDD or they must be current limited to the maximum latch-up current of 100mA. A simple solution is to use a small filtering network between the VDD and AVD plane to delay the power to the AVD plane, which will delay power to each AVD pin.

5.2.4 Decoupling

A 0.01μF capacitor is placed between 3.3 V power and ground for every other VDD pin. The capacitors should be placed as close as possible to the actual pins.

The AVD pins require a filtering network between the VDD_A plane and each AVD pin. The network is a single low-pass RC network. Please refer to the bill of materials in Appendix A for component values.

5.3 COMET-QUAD Design Considerations

5.3.1 Line Interface

The COMET-QUAD Line Interface is configurable to operate in both E1 and T1 short-haul and long-haul applications without changing external line protection circuitry. The Line Interface circuitry used on the AAL1gator-32/TEMUX Development Kit is the recommended external protection circuitry for designs required to meet surge immunity and electrical safety standards for intra-building communications. Refer to the COMET-QUAD Datasheet [5] for more information on this protection.

5.3.2 Backplane System Interface

The Backplane System Interface of the COMET-QUAD provides system side serial clock and data access for 4 T1 or E1 streams. In this design the backplane system interface is configured for serial clock and data. The corresponding signaling and frame pulse signals for each line are routed to the AAL1gator-32 as well, which are optionally used by the AAL1gator-32.

5.3.3 Microprocessor Interface

The Microprocessor Interface provides access to normal and test mode registers, as well as memory-mapped registers. The COMET-QUAD microprocessor interface data and address buses are connected to the PCI9050 PCI Interface chip and the other signals connect through the CPLD for chip select decoding and then to the PCI9050. The microprocessor interface is configured as a non-multiplexed bus by tying the ALE input high and not using it.

5.3.4 Power Supply Sequencing

The following power up sequence for the COMET-QUAD must be followed:

1. +3.3V digital pins

2. +3.3V analog pins (TAVDx, CAVD, RAVDx, QAVD)

3. +2.5V digital pins

Power to the +3.3V pins, both analog and digital, must be applied before +2.5V. Power to the +3.3V digital pins must be applied before power to the +3.3V analog. A simple solution for the latter statement is to use a small filtering network between the +3.3V digital and +3.3V analog pins to delay the power.

5.3.5 Decoupling

0.01μF and 0.1μF capacitors are placed between power and ground for the VDD (+2.5 V and +3.3V) pins. The capacitors should be placed as close to the actual pins as possible.

The AVD pins require a filtering network between the VDD plane and each AVD pin. The network is a single RC network with the resistor between the VDD plane and the AVD pin and the capacitor from the AVD pin to the GND plane. Please refer to the schematics in Appendix A for component values.

5.4 TEMUX Design Considerations

5.4.1 DS3 Interface

The DS3 Interface of the TEMUX interfaces the DS3 Line Interface Unit with the DS3 framer of the TEMUX. The TEMUX DS3 framer decodes the incoming B3ZS-encoded signal and frames to the resulting DS3 stream. In the opposite direction the framer generates the B3ZS-encoded signal from the DS3 stream. Depending on the type of line interface required, the TEMUX can be configured for dual rail or single rail format. The AAL1gator-32/TEMUX Development Kit uses dual rail format to interface with the TDK 78P2241 DS3 Transceiver. Single rail format is used when the LIU handles B3ZS encoding/decoding.

When a DS3 signal is not applied to the DS3 Line Interface Unit it is not possible to recover a DS3 line rate clock for the TEMUX (RCLK). When the TEMUX is not receiving RCLK it cannot accurately maintain its registers, and therefore RCLK should be a nominal 44.736 MHz clock at all times. The 78P2241 DS3 Transceiver provides a loss of signal (LOS) active-low signal that is used to switch in a 44.736 MHz clock. Tri-state non-inverting buffers are used to switch in the clock when LOS goes low. A non-inverting buffer is placed on the RPOS and RNEG signals of the TEMUX as well so that timing can be met.

5.4.2 System Interface

The system side interface of the TEMUX can be configured for serial clock and data, H-MVIP, SBI bus, SBI bus with CAS or CCS H-MVIP, and serial clock and data with CCS H-MVIP. In this design the system side interface is configured for SBI bus or SBI bus with CAS, depending on whether the M13 multiplexing capability of the TEMUX is used.

5.4.3 Microprocessor Interface

The Microprocessor Interface provides access to normal and test mode registers, as well as memory-mapped registers. The TEMUX microprocessor interface data and address buses are connected to the PCI9050 PCI Interface chip and the other signals connect through the CPLD for chip select decoding and then to the PCI9050. The microprocessor interface is configured as a non-multiplexed bus by pulling the ALE input high.

5.5 DS3 Line Interface Design Considerations

The AAL1gator-32/TEMUX Development Kit uses a 78P2241 line interface transceiver IC by TDK Semiconductor Corp. This transceiver IC recovers clock and data from the B3ZS coded DS3 signal and interfaces to the TEMUX. The 78P2241 also provides diagnostic loopbacks for troubleshooting and testing.

5.6 Bus Switch Jumper Configuration

There is one jumper on the board that is used to select the bus switch between the TEMUX and the COMET-QUAD. The jumper should be shorted when using the COMET-QUAD (T1/E1) and left open when using the TEMUX (DS3).

5.7 Power Requirements

Table 2 provides the estimated power requirements for the AAL1gator-32/TEMUX Development Kit.

Table 2 Power Requirement Table

5V Components	Quantity	Current (mA)	Power (mW)
PCI Bridge PCI9050	1	130	650
SEEP, NM93CS46	1	10	50
Misc, pullups/downs	1	40	200
MK2049-01S	1	55	275
3.3V Regulator	1	2876.5	14382.5
Total 5V Power		3111.5	15557.5

3.3V Components	Quantity	Current (mA)	Power (mW)
74HC04	1	1	3.3
74AC125	4	40	132
78P2241	1	80	264
QS53805	1	30	99
CY7C1352	2	600	1980
MAX700C	1	0.5	2
Oscillators	7	119	393
PI3B16233	1	80	264
XC95144XL-7TQ1	1	80	264
PM8315	1	4	13.2
PM7350	1	450	1485
PM73122	1	85	280.5
PM4354	1	441	1455.3
Misc, pullups/downs	1	61	201.3
2.5V Regulator	1	805	2656.5
Total 3.3V Power		2876.5	9492.45

2.5V Components	Quantity	Current (mA)	Power (mW)
PM8315	1	368	920
PM73122	1	400	1000
PM4354	1	38	95
Total 2.5V Power		806	2115

6 PHYSICAL AND MECHANICAL DESCRIPTIONS

6.1 Form Factor

The AAL1gator-32/TEMUX Development Kit is a standard length, 32-bit, 5V PCI expansion card. The card has a metal mounting bracket for card location and retention. The mechanical specifications of the card comply to the PCI Local Bus Specification revision 2.2 and for more information refer to [7] of the references.

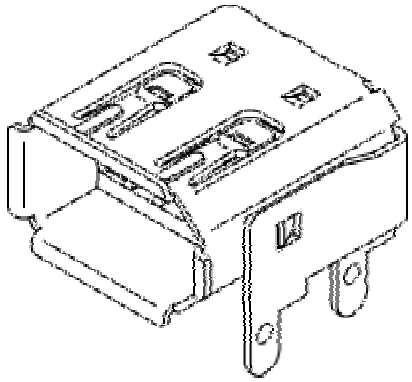
6.2 Connectors

There are three groups of connectors for the AAL1gator-32/TEMUX Development Kit: front-edge connectors, top-edge connectors and the PCI card edge connector. The front edge connectors consist of the LVDS connectors and the DS3 connectors. The top edge connectors are the 8 T1/E1 connectors.

6.2.1 LVDS Connector

The LVDS connector requires a bandwidth of 100 to 200 Mb/s. The IEEE 1394-1995 shielded I/O PCB socket is used to meet this bandwidth requirement. The Molex 53984-0611 socket shown in Figure 5 is use to satisfy the physical limitations of a PCI card connecting to Firewire cables.

Figure 5 Molex 53984-0611 Connector



6.2.2 DS3 Connector

The AAL1gator-32/TEMUX Development Kit uses 50Ω SMB connectors on the front edge of the card. Right angle SMB connectors are used rather than BNC connectors because they are smaller and allow placement on the front edge of

the card. Although the traces and cabling of these signals are 75Ω, 50Ω SMB connectors are used because 75Ω require custom manufacturing and are larger. 50Ω SMB connectors have been found to work adequately in these applications. SMB to BNC adapter cables are available for interfacing with some equipment.

6.2.3 Mini-Bantam Connectors

The 4 T1 and E1 links are connected to the AAL1gator-32/TEMUX Development Kit via mini-bantam connectors.

6.2.4 PCI Card Edge Connector

The PCI edge connector is implemented as a standard length 5V 32-bit PCI connector. For the dimensions and tolerances of this card edge connector refer to the PCI Local Bus Specification [7].

6.2.5 Debug Header

A 0.64 mm Matched Impedance Connector (MICTOR) by AMP (part number 2-767004-2) is used to provide debug access to the board. This connector is used to verify the timing of microprocessor interface and for connection to a logic analyzer.

6.3 LEDs

6.3.1 Card Status LEDs

A basic set of LEDs provide visual information about power and reset on the card. These 4 LEDs are positioned on the front edge of the card so that they can be viewed easily at any time.

- +5 V, green – indicates presence of +5 V
- +3.3 V, green – indicates presence of +3.3 V
- +2.5 V, green – indicates the presence of +2.5 V
- Reset, green – indicates that the reset signals connected to each of the PMC-Sierra devices is low (active).

6.3.2 Auxiliary LEDs

Four auxiliary LEDs are easily visible on the front edge of the expansion card. These yellow LEDs are used to indicate an interrupt from each of the PMC-Sierra devices. By changing the CPLD code these LEDs can indicate other status information.

7 SOFTWARE INTERFACES

7.1 PCI 9050 Configuration

The following tables specify the values that should be programmed into the SEEP. These values will be loaded into the PCI9050 registers on power-up. The checksum of the EEPROM is 0x3388. Please refer to the PCI9050 datasheet for further details.

Table 3 EEPROM Contents

EEPROM Offset (Hex)	Value (Hex)	PLX Register
0	9050	Device ID
2	10B5	Vendor ID
4	0680	Class Code
6	0000	ClassCode
8	2353	Subsystem ID
A	11F8	Subsystem Vendor ID
C	0000	Max Latency and Min Grant (not loadable)
E	00FF	Interrupt Pin
10	0FC0	MSW of Address Space 0 Range
12	0000	LSW of Address Space 0 Range
14	0FFF	MSW of Address Space 1 Range
16	0000	LSW of Address Space 1 Range
18	0FFF	MSW of Address Space 2 Range
1A	E000	LSW of Address Space 2 Range
1C	0FFF	MSW of Address Space 3 Range
1E	FC00	LSW of Address Space 3 Range
20	0000	MSW of Expansion Rom Range
22	0000	LSW of Expansion Rom Range
24	0000	MSW of Address Space 0 Remap
26	0001	LSW of Address Space 0 Remap

EEPROM Offset (Hex)	Value (Hex)	PLX Register
28	0040	MSW of Address Space 1 Remap
2A	0001	LSW of Address Space 1 Remap
2C	0080	MSW of Address Space 2 Remap
2E	0001	LSW of Address Space 2 Remap
30	00C0	MSW of Address Space 3 Remap
32	0001	LSW of Address Space 3 Remap
34	0000	MSW of Expansion Rom Remap
36	0000	LSW of Expansion Rom Remap
38	5681	MSW of Space 0 Bus Descriptor
3A	A1A2	LSW of Space 0 Bus Descriptor
3C	5681	MSW of Space 1 Bus Descriptor
3E	A1A0	LSW of Space 1 Bus Descriptor
40	5681	MSW of Space 2 Bus Descriptor
42	A1A0	LSW of Space 2 Bus Descriptor
44	5681	MSW of Space 3 Bus Descriptor
46	A1A0	LSW of Space 3 Bus Descriptor
48	0000	MSW of Expansion Rom Bus Descriptor
4A	0000	LSW of Expansion Rom Bus Descriptor
4C	0020	MSW of CS0 Register
4E	0001	LSW of CS0 Register
50	0040	MSW of CS1 Register
52	8001	LSW of CS1 Register
54	0080	MSW of CS2 Register
56	1001	LSW of CS2 Register
58	00C0	MSW of CS3 Register
5A	0201	LSW of CS3 Register
5C	0000	MSW of Interrupt Control/Status
5E	0000	LSW of Interrupt Control/Status

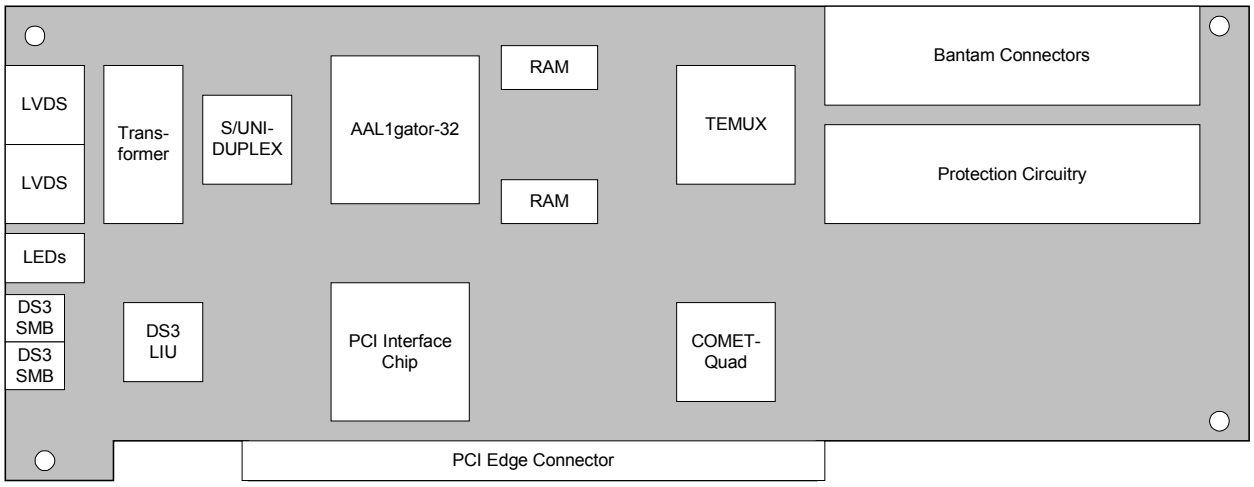
EEPROM Offset (Hex)	Value (Hex)	PLX Register
60	0002	MSW of EEPROM and Misc. Control
62	46C2	LSW of EEPROM and Misc. Control
64 – 7F	FFFF	Unused

8 LAYOUT DESCRIPTIONS

8.1 Component Placement

Figure 6 shows the approximate placement of the major components of the AAL1gator-32/TEMUX Development Kit. Components are located to minimize trace lengths while taking into account the priority of traces.

Figure 6 Major Component Placement



8.2 Power and Ground

Four power and ground planes are used on the AAL1gator-32/TEMUX Development Kit PCI expansion board. There are two ground planes, one +2.5V plane and one +3.3 V plane. In addition there is a small +5 V power plane around the PCI9050 and the PCI card edge connector for the +5 V devices. This plane is on one of the inner signal layers of the board and does not have any critical traces routed over it unless they are on an outside layer where a ground plane is in-between. A chassis ground signal is routed around the outside of the board that connects to each mounting hole and connector shielding.

8.3 Routing

- All power and ground traces are as wide and short as possible to minimize trace inductance.

- All high speed traces are routed over continuous image planes (power or ground planes).
- All traces carrying transmit and receive line rate data are transmission lines with controlled impedances. These traces should be routed on the same side and kept as short as possible.
- Both signals of a differential pair are of equal length and routed close to each other.
- All PCI signal traces are 75 Ω impedance.
- All UTOPIA interface signals are also 75 Ω impedance. For each of the UTOPIA interface signal, a series termination resistor is added at each output.
- All LVDS signals are 50Ω controlled impedance.

8.4 PCI Bus Signal Specification

This layout follows the PCI Rev. 2.2 Specification layout restrictions. The PCI Special Interest Group specification has stringent and detailed rules on decoupling, power consumption, trace lengths, routing, trace impedance, and signal loading. It is therefore essential to check the latest PCI specification before proceeding with new designs and layouts.

The AAL1gator-32/TEMUX Development Kit PCI expansion board conforms to the following PCI Specifications/Recommendations:

- Component height on the component side does not exceed 0.570 inches, and on the solder side does not exceed 0.105 inches.
- PCI CLK signal trace is 2.5 inches +/- 0.1 inches and is connected to only one load.
- All 32-bit interface signals have the maximum trace length of 1.5 inches.
- Trace impedance for shared PCI signals are within 60-100 Ω range, and trace velocity is between 150 and 190 ps/inch.
- 20 mil wide traces are used to connect the power and ground pins on PCI connector to their respective planes and the trace lengths are limited to 250 mil.
- Route all traces over continuous image planes.

9 MANUFACTURING ISSUES

9.1 Board Assembly

The AAL1gator-32/TEMUX Development Kit has one assembly option. The S/UNI-DUPLEX LVDS line interface can be populated as capacitively coupled or transformer coupled. For capacitive coupling, transformer T1 should not be populated on the board. For transformer coupling, capacitors C204 to C211 and resistors R126 to R133 should not be populated on the board. The development kit boards are originally populated with the transformer-coupled option. The above modifications must be made to the hardware to achieve a capacitvely-coupled board.

10 GLOSSARY

ATM	Asynchronous Transfer Mode
AAL1	ATM Adaptation Layer Type 1
AAL1gator-32	PMC-Sierra's mnemonic for the PM73122 32 Link CES/DBCES ATM AAL1 SAR
COMET-QUAD	PMC-Sierra's mnemonic for the PM4354 Combined Four-channel E1/T1 Framer/Transceiver
DSLAM	Digital Subscriber Line Access Multiplexer
LAN	Local Area Network
LVDS	Low Voltage Differential Signal
PBGA	Plastic Ball Grid Array
POTS	Plain Old Telephone Service
PSTN	Public Switched Telephone Network
SAR	Segmentation and Reassembly
S/UNI	SATURN User Network Interface
S/UNI-DUPLEX	PMC-Sierra's mnemonic for the PM7350 Dual Port Serialized UTOPIA Multiplexer
SCI-PHY	PMC-Sierra's enhanced UTOPIA bus
TDM	Time Division Multiplexing
TEMUX	PMC-Sierra's mnemonic for the PM8315 High Density T1/E1 Framer with Integrated VT/TU Mapper and M13 Multiplexer
WAN	Wide Area Network

11 REFERENCES

1. PMC-Sierra, Inc., PMC-2001068, “AAL1gator-32/TEMUX Development Kit Platform”, July 2000, Issue 1.

2. PLX Technology, “PCI9050-1 Databook”, April 17, 1997, Version 1.01

3. PMC-Sierra, Inc., PMC-1981419, “32 Link CES/DBCES AAL1 SAR Processor (AAL1gator-32) Telecom Standard Product Data Sheet”, May 2000, Issue 5.

4. PMC-Sierra, Inc., PMC-1981125, “High Density T1/E1 Framer with Integrated VT/TU Mapper and M13 Multiplexer Telecom Standard Product Data Sheet”, April 2001, Issue 6.

5. PMC-Sierra, Inc., PMC-1990315, “COMET-QUAD Datasheet”, May 2001, Issue 6.

6. PMC-Sierra, Inc., PMC-1980581, “S/UNI-DUPLEX Dual Serial Link PHY Multiplexer Data Sheet”, April 2000, Issue 5.

7. PCI Special Interest Group,”PCI Local Bus Specification”, December 1998, Revision 2.2.

8. PMC-Sierra, Inc., PMC-1991820, “AAL1gator-32/8/4 Programmer’s Guide”, January 2000, Issue 1.

9. ATM Forum, “Circuit Emulation Service Interoperability Specification”, January 1997, Version 2.0.

12 APPENDIX A: BILL OF MATERIALS

Table 4 Major Component List

Ref Des	Part Name – Value	Part Number	Manufacturer	Qty
J12, J14-J20	BANTAM Connector	ELECTROSONIC – PC-834-J-(BLACK)	ADC TELECOM	8
Y4	EPSON 12.288MHZ CRYSTAL	MA-505-12.288M-C2	EPSON ELECTRONICS	1
U23, U24, U26, U27, U29, U30, U32, U33	LC01-6	SEMTECH – LC01-6	SEMTECH	8
U28	1.544 HCMOS OSCILLATOR	M-TRON MB3050H-1.544MHZ	MMD	1
U1	38.880 HCMOS OSCILLATOR	M-TRON MB3050H-38.880MHZ	MMD	1
U11	PCI9050_PQFP-BASE	PCI9050-1	PLX TECHNOLOGY	1
TR1-TR16	THERMISTOR	TR250-180	RAYCHEM	16
Y1	OSCILLATOR, 25MHZ, 3.3V, 50PPM	CB3LV-3C-25.0000- T	CTS REEVES	1
U12, U14	CY7C1352-80MHZ SRAM PIPELINED 256KX18 TQFP100	CY7C1352	CYPRESS	2
J9	SMB_VERTICAL-BASE	ARF1244-ND	DIGI-KEY	1
Y6	OSCILLATOR, 19.44MHZ, 3.3V, 50PPM	H5M943-19.440M	CONNOR WINFIELD	1
Y3	OSCILLATOR, 37.056MHZ, 3.3V, 32PPM	H5M943-37.056M	CONNOR WINFIELD	1
Y5	OSCILLATOR, 44.736MHZ, 3.3V, 50PPM	H5M943-44.736M	CONNOR WINFIELD	1
Y7	OSCILLATOR, 49.152MHZ, 3.3V, 32PPM	H5M943-49.152M	CONNOR WINFIELD	1
Y2	OSCILLATOR, 25.00MHZ, 3.3V, 50PPM	H5M943-25.000M	CONNOR WINFIELD	1

U9	NM93CS46_DIP8_SOCKET –BASE	NM93CS46EN	FAIRCHILD SEMI	1
U16	MK2049 IC Clock PLL	MK2049-01S	ICS MICROCLOCK	1
J3, J4	SMB RIGHT ANGLE	131-3701-341	JOHNSON COMPONENTS	2
J1, J2	MOLEX 53984-0611 2MM	53984-0611	MOLEX	2
U13	PI3B16233 TSSOP56-BASE	PI3B16233	PERICOM	1
U10	AAL1GATOR-32_SBGA-BA SE	PM73122	PMC-SIERRA	1
U25	COMET-QUAD_REVA3_PBG A-BASE	PM4354	PMC-SIERRA	1
U17	TEMUX_REVC5_PBGA-BAS E	PM8315-PI	PMC-SIERRA	1
U4	SUNIDUPLEX_SCIPHY_1_ PBGA-BASE	PM7350-PI	PMC-SIERRA	1
T2	PE65967_LS-1-BASE	PE-65967	PULSE	1
U2	PE65968_LS-1-BASE	PE-65968	PULSE	1
T1	H1026_SMD-BASE	H1026	PULSE ENGINEERING	1
U6	78P2241_PLCC-BASE	78P2241	TDK SEMICONDUCTOR	1
U31	T9021 Transformer	T9021	PULSE	1
U19	XC95144XL-TQ100_TQFP –7NS	XC95144XL-7TQ100C	XILINX	1

Table 5 Miscellaneous Parts

Ref Des	Part Name – Value	Part Number	Manufacturer	Qty
U5, U8, U21, U22	QUAD BUFFER WITH THREE STATE OUTPUTS	74ACT125SC	FAIRCHILD SEMI	4
U20	74HC04_SOIC-VCC=3_3V			1
C6, C9-C12, C14,	CAPACITOR-0.01UF,	DIGIKEY		139

C16, C19-C22, C26, C30, C35-C39, C42, C44, C46, C47, C49, C50, C53, C56, C62, C66-C71, C73, C74, C76-C79, C81, C82, C84-C90, C92-C119, C121, C122, C124-C127, C129-C147, C149, C151-C168, C170-C174, C176, C177, C179, C185, C186, C189, C191-C193, C197, C199, C203, C213, C216	50V, X7R_603	PCC103BVCT-ND		
C201	CAPACITOR-0.047UF, 25V, X7R_0603	NEWARK – 85F219		1
C27	CAPACITOR-0.047UF, 50V, PPS_1913	ECH-U1H473GB9		1
C1, C2, C5, C7, C28, C29, C41, C55, C61, C64, C91, C187, C188, C190, C194, C195, C198, C200, C212, C215	CAPACITOR-0.1UF, 16V, X7R_603	PANASONIC – ECJ-1VB1C104K		20
C45, C48, C54, C65	CAPACITOR-0.47UF, 6.3V, X5R_603	ECJ-1VB0J474K	PANASONIC	4
C204-C211	CAPACITOR-0.22UF, 16V, Y5V_805	NEWARK -- 52F022		8
C148	CAPACITOR-0.33UF, 16V, X7R_1206	ECJ-3VB1C334K	PANASONIC	1
C3, C4	CAPACITOR-10UF, 16V, TANT TEH	DIGI-KEY -- PCT3106CT-ND		2
C184, C196	CAPACITOR-10UF, 6.3V, TANT TE	DIGI-KEY -- PCS1106CT-ND		2
C31	CAPACITOR-22UF, 16V, TANT TEH	DIGI-KEY -- PCT3226CT-ND		1
C13, C17, C18, C63, C72, C75, C80, C83, C120, C123, C128,	CAPACITOR-22UF, 6.3V, TANT TE			19

C150, C169, C175, C178, C180-C183				
C15, C57-C60, C202, C214	CAPACITOR-4.7UF, 10V, TANT TEH	DIGI-KEY -- PCT2475CT-ND		7
C8, C23-C25, C32-C34, C40, C43, C51, C52	CAPACITOR-47UF, 10V, TANT TEH	DIGI-KEY -- PCT2476CT-ND		11
U7	CLOCK_BUFFER_QS 53805 -BASE	QS53805	QUALITY SEMI	1
J10	CON_MICTOR_38PIN _2-7 67004-2-BAA	2-767004-2	AMP	1
D4	5% 1W SMD ZENER DIODE	DIGI-KEY -- ZM4735ACT-ND		1
D5, D6	DIODE_SCHOTTKY_ SMB_2 -2A, 20V	DIGI-KEY -- B220DICT-ND		2
SW2	DIPSW4-BASE			1
F2	FUSE__SMD_SOCKE T-2.5 00A, NANO	DIGIKEY -- F1225CT-ND		1
F1	FUSE__SMD_SOCKE T-5.0 00A, NANO	DIGIKEY -- F1228CT-ND		1
J8	HEADER2_100MIL-BASE	PZC36SAAN	SULLINS ELECTRONICS	1
J5-J7	HEADER3S_100MIL-BASE			3
J13	HEADER6_100MIL-BASE	PZC36SAAN	SULLINS ELECTRONICS	1
J11	HEADER_4X2_100MI L-BASE			1
L1-L3	INDUCTOR-4.7UH, , INDUCTOR_FC	DIGI-KEY DN10472CT-ND		3
D3	LED-SUPER_RED, SURFACE MOUNT	SIEMENS -- LST670-HK		1
U15	7A LOW DROPOUT 100MV TO 540MV REGULATOR	LT1580CQ	LINEAR TECHNOLOGY	1
U3	4.6A LOW DROPOUT FIXED 3.3V	LT1585CT-3.3	LINEAR	1

	REGULATOR		TECHNOLOGY	
U18	POWER-SUPPLY MONITOR WITH RESET	MAXIM MAX700CSA		1
SW1	VERT PCB MOUNT SPST PUSH BUTTOM	DIGIKEY -- P8009S-ND		1
U13	Bus Switch	PI3B16233	PERICOM	1
R3, R47, R95	RESISTOR-0, 5%, 603			3
R1, R37, R39, R40, R43-R45, R50, R51, R73, R75, R78, R79, R135, R137	RESISTOR-1, 5%, 603			15
R126-R133	RESISTOR-1.00M, 1%, 603	DIGI-KEY -- P<VALUE>MHCT-ND		8
R6, R83, R136, R138	RESISTOR-1.0K, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND		4
R65-R71, R76	RESISTOR-100, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND		8
R41, R52, R72, R80, R123	RESISTOR-100K, 1%, 603			5
R16-R21, R84, R122, R124, R125	RESISTOR-10K, 1%, 603	DIGI-KEY -- P<VALUE>GCT-ND		10
R91, R92	RESISTOR-110, 1%, 805	DIGI-KEY -- P<VALUE>CCT-ND		2
R53, R54, R56, R57, R59, R60, R62, R63	RESISTOR-12.7, 1%, 603	DIGI-KEY -- P12.7HCT-ND		8
R55, R58, R61, R64	RESISTOR-18.2, 1%, 603	DIGI-KEY -- P18.2HCT-ND		4
R7, R8	RESISTOR-20, 5%, 603	?		2
R14	RESISTOR-270, 5%, 603	DIGI-KEY -- P<VALUE>GCT-		1

		ND		
R5	RESISTOR-3.3, 5%, 805	DIGI-KEY -- P<VALUE>BCT-ND		1
R2	RESISTOR-301, 1%, 805	DIGI-KEY -- P301CCT-ND		1
R24, R25, R94, R100, R106, R116	RESISTOR-330, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND		6
R42, R48, R49	RESISTOR-4.7, 5%, 603			3
R112	RESISTOR-4.75K, 1%, 603	DIGI-KEY -- P<VALUE>GCT-ND		1
R22, R23, R26, R29, R30, R46, R81, R82, R87-R90, R93, R96, R102, R107-R109, R117, R118	RESISTOR-4.7K, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND		20
R110, R113	RESISTOR-430, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND		2
R9-R12	RESISTOR-49.9, 1%, 603	?		4
R27	RESISTOR-5.1M, 5%, 805	DIGI-KEY -- P<VALUE>ACT-ND		1
R134	RESISTOR-5.23K, 1%, 805	DIGI-KEY -- P<VALUE>CCT-ND		1
R4, R13, R28, R31-R36, R38, R74, R77, R86, R97-R99, R101, R103-R105, R115, R119-R121, R139, R140	RESISTOR-56, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND		26
R15	RESISTOR-75, 1%, 805	DIGI-KEY -- P75.0CCT-ND		1

R111, R114	RESISTOR-750, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND		2
R85	RESISTOR-931, 1%, 805	DIGI-KEY -- P<VALUE>CCT-ND		1
RN24, RN25, RN30, RN31	RES_ARRAY_4_SMD-10K	DIGI-KEY -- Y4<VALUE CODE>-ND		4
RN1, RN2	RES_ARRAY_4_SMD-270	DIGI-KEY -- Y4<VALUE CODE>-ND		2
RN19, RN21, RN33-RN37, RN40-RN47	RES_ARRAY_4_SMD-330	DIGI-KEY -- Y4<VALUE CODE>-ND		15
RN3-RN17, RN20, RN26, RN32, RN38, RN39, RN61, RN64, RN65	RES_ARRAY_4_SMD-4.7K	DIGI-KEY -- Y4<VALUE CODE>-ND		23
RN18, RN22, RN23, RN27-RN29, RN48-RN60, RN62, RN63, RN66	RES_ARRAY_4_SMD-56	DIGI-KEY -- Y4<VALUE CODE>-ND		22
D2	QUAD GREEN LED.	SSF-LXH5147LGD	LUMEX	1
D1	QUAD YELLOW LED.	SSF-LXH5147LYD	LUMEX	1

13 APPENDIX B: SCHEMATICS

The schematics for the development kit are revision 2.0. The schematics contain 13 pages as follows:

Sheet 1: Root Drawing

This sheet provides a block view of the interface signals between each block of the AAL1gator-32/TEMUX Development Kit.

Sheet 2: DS3 Line Interface

This sheet shows the connection surrounding the TDK Semiconductor 78P2241 Transceiver and the SMB connectors.

Sheet 3-4: TEMUX Block

These sheets shows the connections required for PMC-Sierra's PM8315 TEMUX.

Sheet 5-6: COMET Line Interface

These sheets contain the connectors and line protection circuitry required by the COMET-QUAD.

Sheet 7: COMET-QUAD Block

This sheet contains PMC-Sierra's PM4354 COMET-QUAD and its important power pin filtering circuitry.

Sheet 8-10: AAL1gator-32 Block

These sheets show the PM73122 AAL1gator-32 and the two SRAMs.

Sheet 11: S/UNI-DUPLEX

This sheet shows the PM7350 S/UNI-DUPLEX and the LVDS connectors and line interface circuitry.

Sheet 12-13: PCI and CPLD

These sheets show the PCI9050, CPLD, MK2049 PLL, and power supplies.

REVISIONS				
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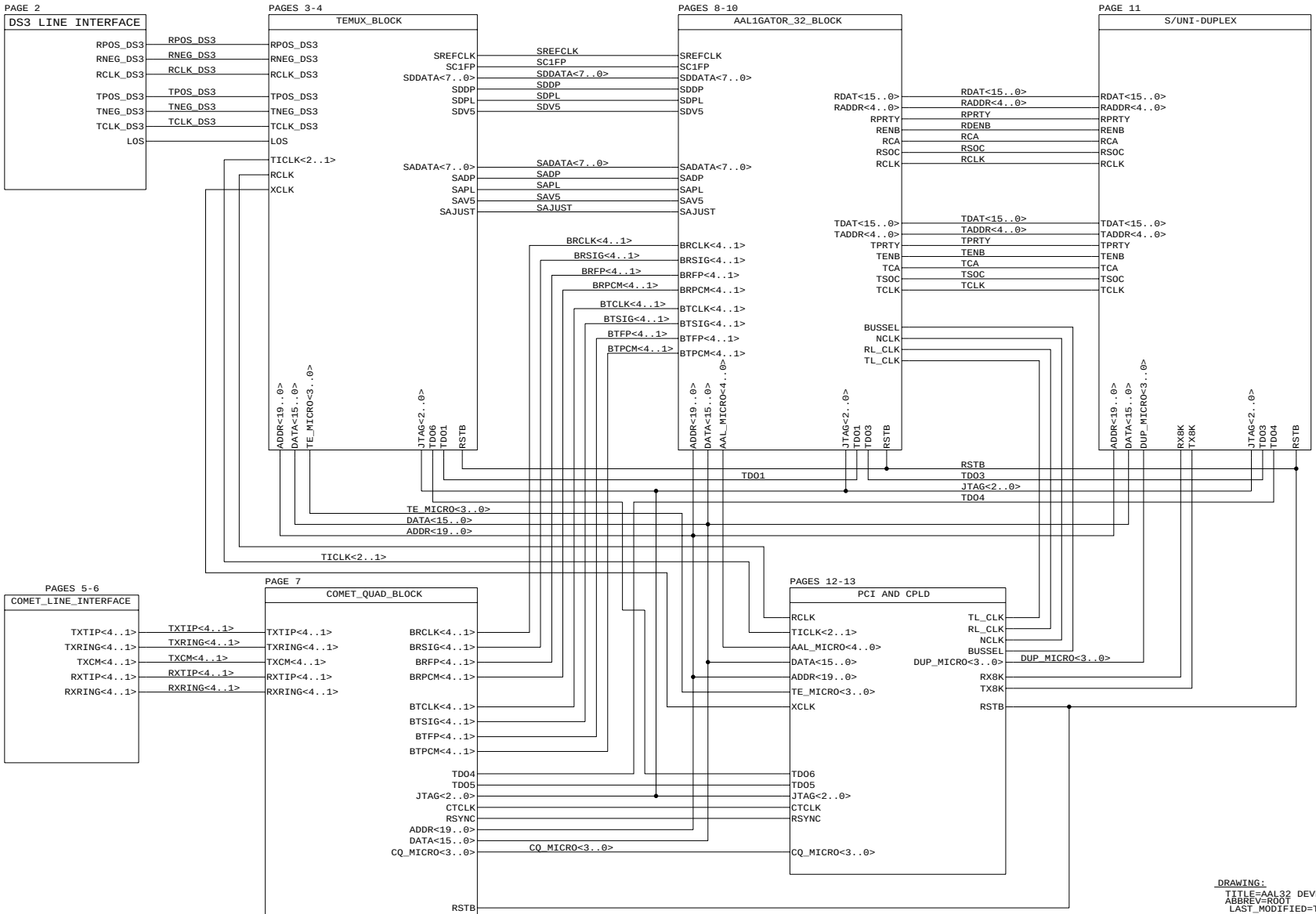

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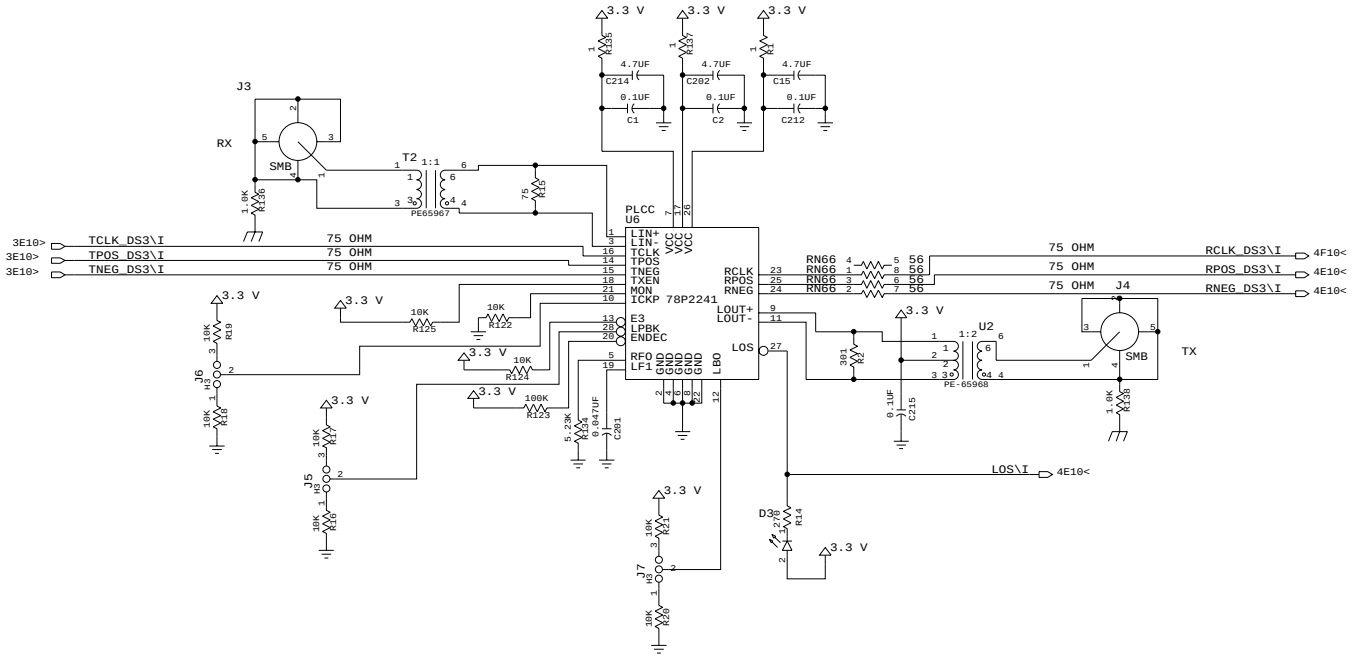
LAST_MODIFIED=Tue Dec 12 09:46:10 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991144 DOCUMENT ISSUE NUMBER: 3	ISSUE DATE: NOVEMBER 2000
TITLE: AAL1GATOR-32/TEMUX DEVELOPMENT KIT ROOT DRAWING	REVISION NUMBER: 2.0
ENGINEER: BW	PAGE:1 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

DS3 LINE INTERFACE



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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991144 DOCUMENT ISSUE NUMBER: 3	ISSUE DATE: NOVEMBER 2000
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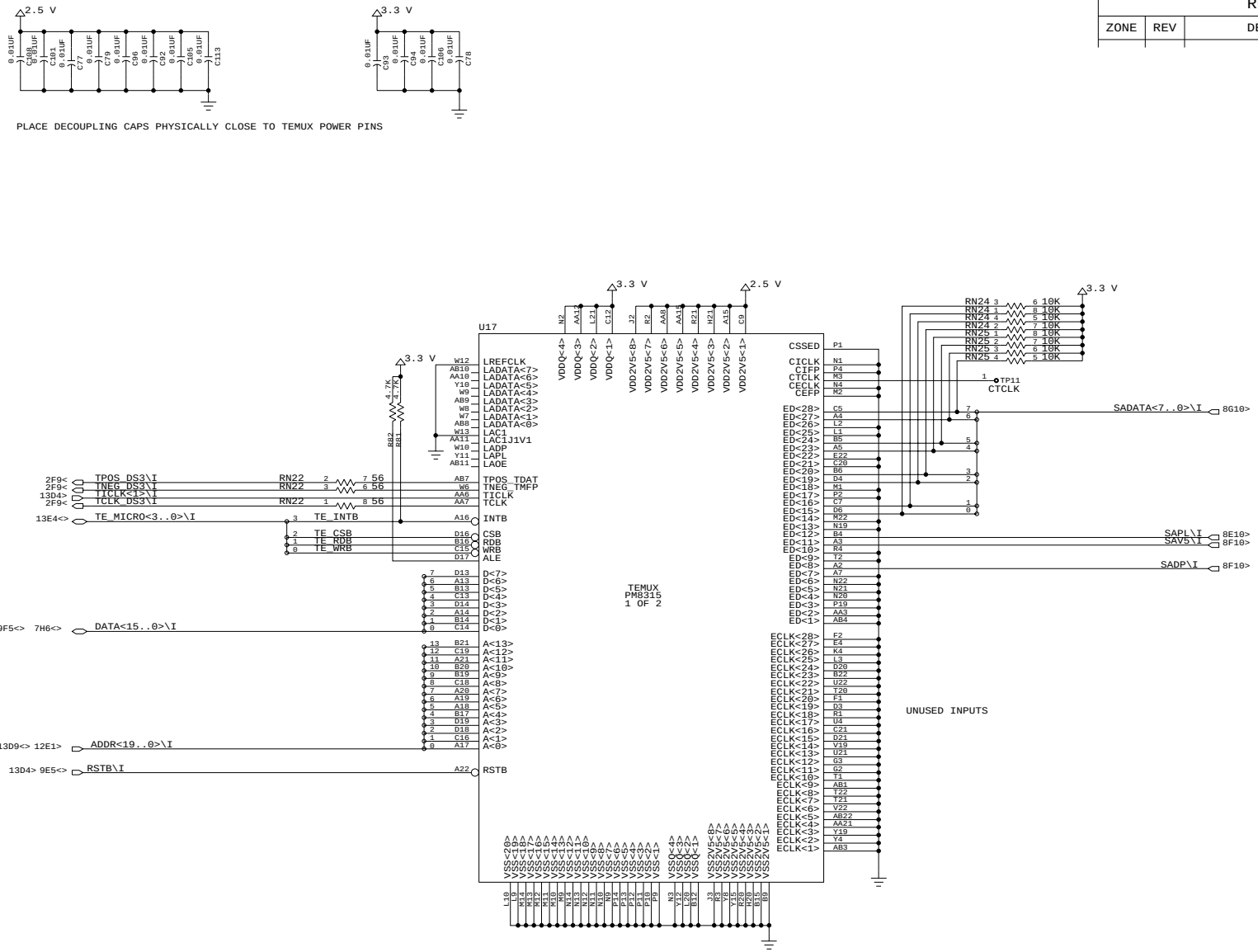
ENGINEER: BW	PAGE:2 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

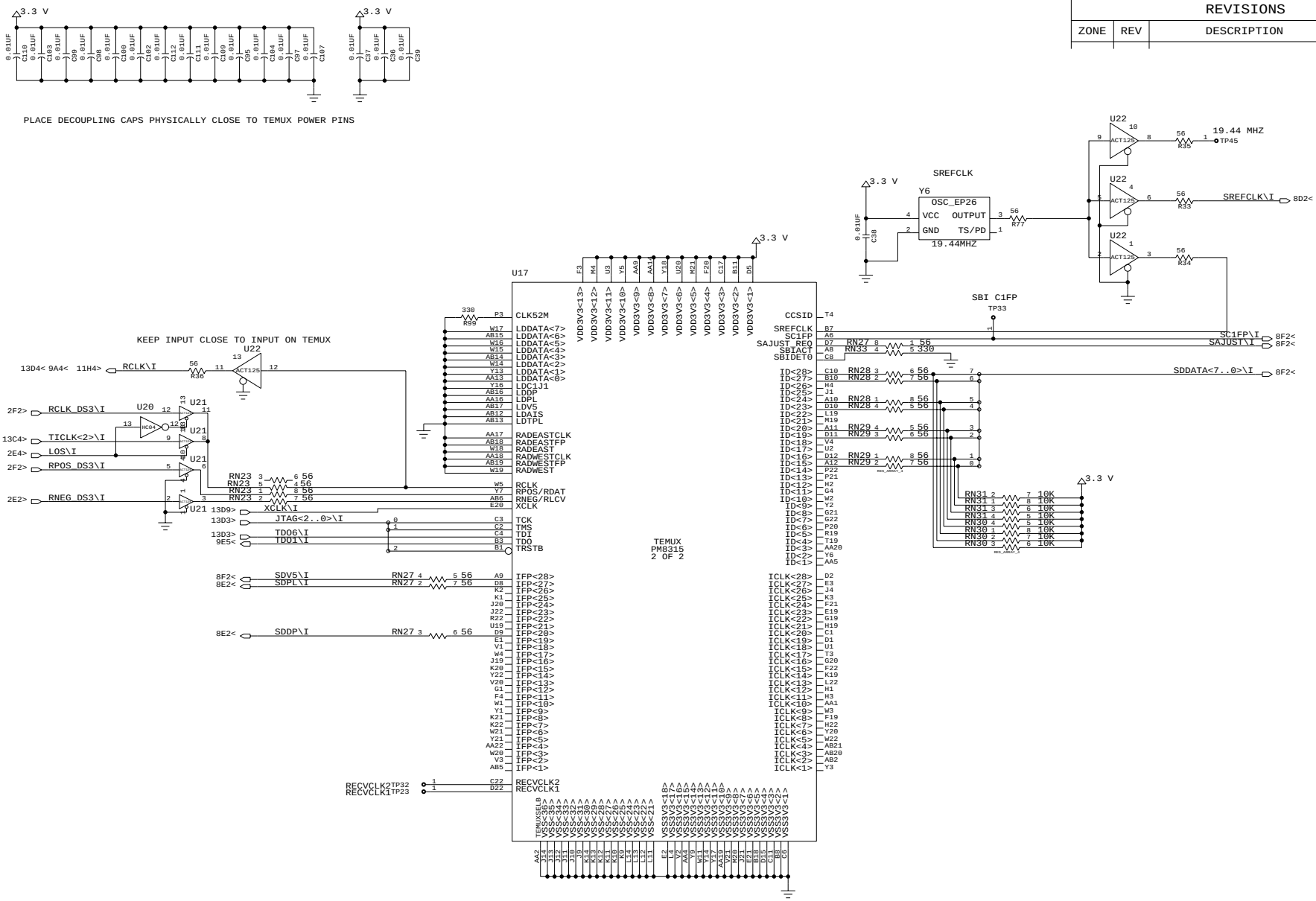


DRAWING:
TEMUX_1.1
TMX1

Thu May 17 10:44:54 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991144 DOCUMENT ISSUE NUMBER: 3	ISSUE DATE: NOVEMBER 2000
TITLE: AAL1GATOR-32/TEMUX DEVELOPMENT KIT TEMUX_BLOCK 1	REVISION NUMBER: 2.0
ENGINEER: BW	PAGE:3 OF 13


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
PLACE DECOUPLING CAPS PHYSICALLY CLOSE TO TEMUX POWER PINS
KEEP INPUT CLOSE TO INPUT ON TEMUX
U17
TEMUX
PM8315
2 OF 2
SREFCLK
OSC_EP26
19.44MHZ
SBI C1FP
SDDATA<7..0>\I
SREFCLK\I
SC1FP\I
SAJUST\I
RCLK\I
RCLK_DS3\I
TICLK<2>\I
LOS\I
RPOS_DS3\I
RNEG_DS3\I
XCLK\I
JTAG<2..0>\I
TDO6\I
TDO1\I
SDV5\I
SDPL\I
SDDP\I
RECVCLK2
RECVCLK1
DRAWING:
TEMUX_1.2
TMX1
Thu May 17 10:44:59 2001
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-1991144
DOCUMENT ISSUE NUMBER: 3
ISSUE DATE: NOVEMBER 2000
TITLE: AAL1GATOR-32/TEMUX DEVELOPMENT KIT TEMUX_BLOCK 2
REVISION NUMBER: 2.0
ENGINEER: BW
PAGE:4 OF 13

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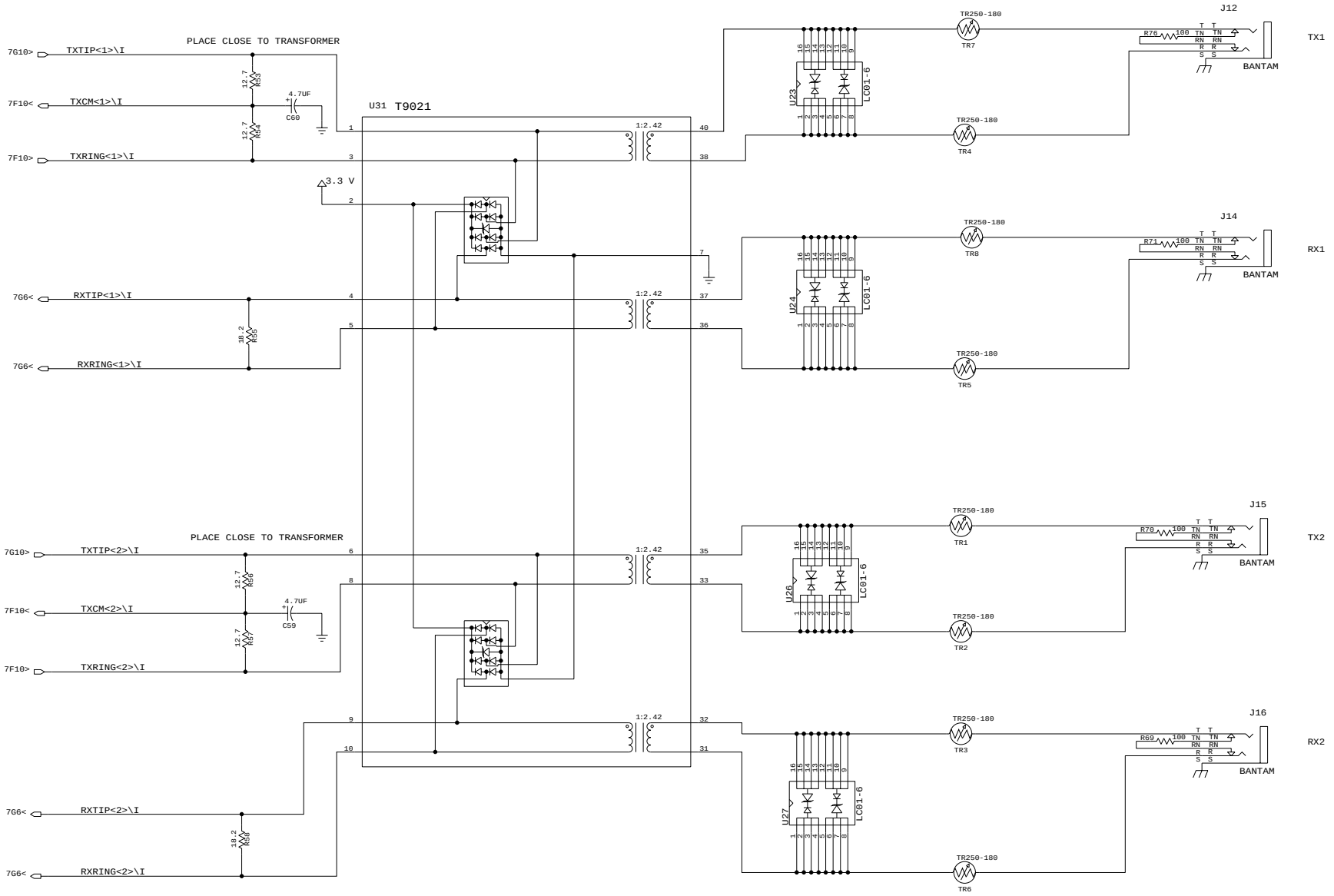

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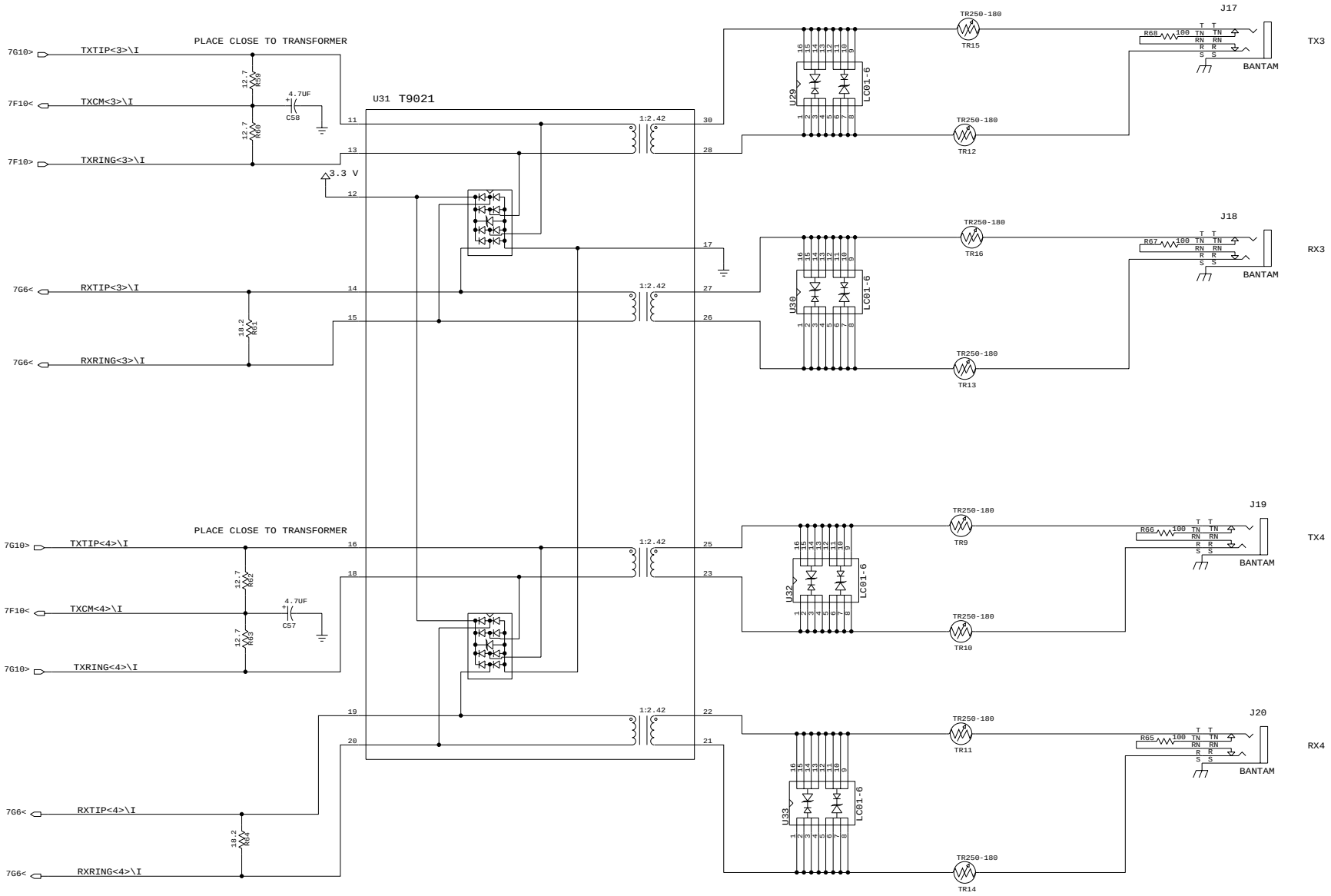
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991144 DOCUMENT ISSUE NUMBER: 3	ISSUE DATE: NOVEMBER 2000
TITLE: AAL1GATOR_32/TEMUX DEVELOPMENT KIT LINE INTERFACE 1	REVISION NUMBER: 2.0
ENGINEER: BW	PAGE:5 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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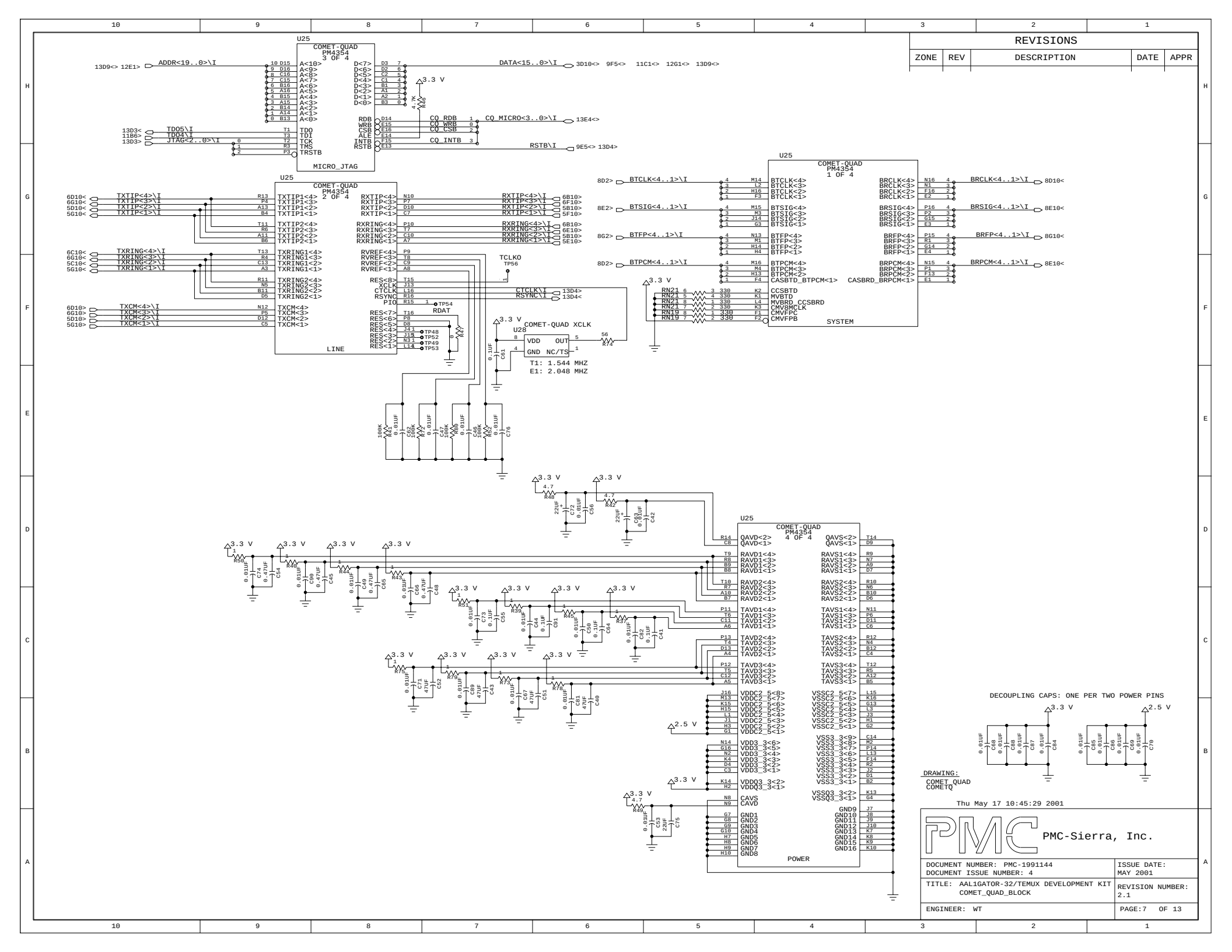
ENGINEER: BW	PAGE:6 OF 13


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
U25
COMET-QUAD
PM4354
3 OF 4
MICRO_JTAG
ADDR<19..0>\I
DATA<15..0>\I
3.3 V
4.7K
CQ RDB
CQ WRB
CQ CSB
CQ INTB
CQ_MICRO<3..0>\I
RSTB\I
TDO5\I
TDO4\I
JTAG<2..0>\I
TDO
TDI
TCK
TMS
TRSTB
U25
COMET-QUAD
PM4354
2 OF 4
LINE
TXTIP<4>\I
TXTIP<3>\I
TXTIP<2>\I
TXTIP<1>\I
RXTIP<4>\I
RXTIP<3>\I
RXTIP<2>\I
RXTIP<1>\I
TXRING<4>\I
TXRING<3>\I
TXRING<2>\I
TXRING<1>\I
RXRING<4>\I
RXRING<3>\I
RXRING<2>\I
RXRING<1>\I
TXCM<4>\I
TXCM<3>\I
TXCM<2>\I
TXCM<1>\I
RXCM<4>\I
RXCM<3>\I
RXCM<2>\I
RXCM<1>\I
TCLKO
TP56
RDAT
CTCLK\I
RSYNC\I
U28
COMET-QUAD XCLK
VDD OUT
GND NC/TS
T1: 1.544 MHZ
E1: 2.048 MHZ
U25
COMET-QUAD
PM4354
1 OF 4
SYSTEM
BTCLK<4..1>\I
BTSIG<4..1>\I
BTFP<4..1>\I
BTPCM<4..1>\I
BRCLK<4..1>\I
BRSIG<4..1>\I
BRFP<4..1>\I
BRPCM<4..1>\I
CASBTD_BTPCM<1>
CASBRD_BRPCM<1>
CCSBTD
MVBTD
MVBRD_CCSBRD
CMV8MCLK
CMVFPC
CMVFPB
U25
COMET-QUAD
PM4354
4 OF 4
POWER
QAVD<2>
QAVD<1>
QAVS<2>
QAVS<1>
RAVD1<4>
RAVD1<3>
RAVD1<2>
RAVD1<1>
RAVS1<4>
RAVS1<3>
RAVS1<2>
RAVS1<1>
RAVD2<4>
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RAVS2<1>
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TAVD1<3>
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TAVS3<2>
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VDDC2_5<6>
VDDC2_5<5>
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VDDC2_5<1>
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VSS3_3<4>
VSS3_3<3>
VSS3_3<2>
VSS3_3<1>
VDDQ3_3<2>
VDDQ3_3<1>
VSSQ3_3<2>
VSSQ3_3<1>
CAVS
CAVD
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
2.5 V
DECOUPLING CAPS: ONE PER TWO POWER PINS
DRAWING:
COMET_QUAD
COMETQ
Thu May 17 10:45:29 2001
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-1991144
DOCUMENT ISSUE NUMBER: 4
ISSUE DATE: MAY 2001
TITLE: AAL1GATOR-32/TEMUX DEVELOPMENT KIT
COMET_QUAD_BLOCK
REVISION NUMBER: 2.1
ENGINEER: WT
PAGE:7 OF 13

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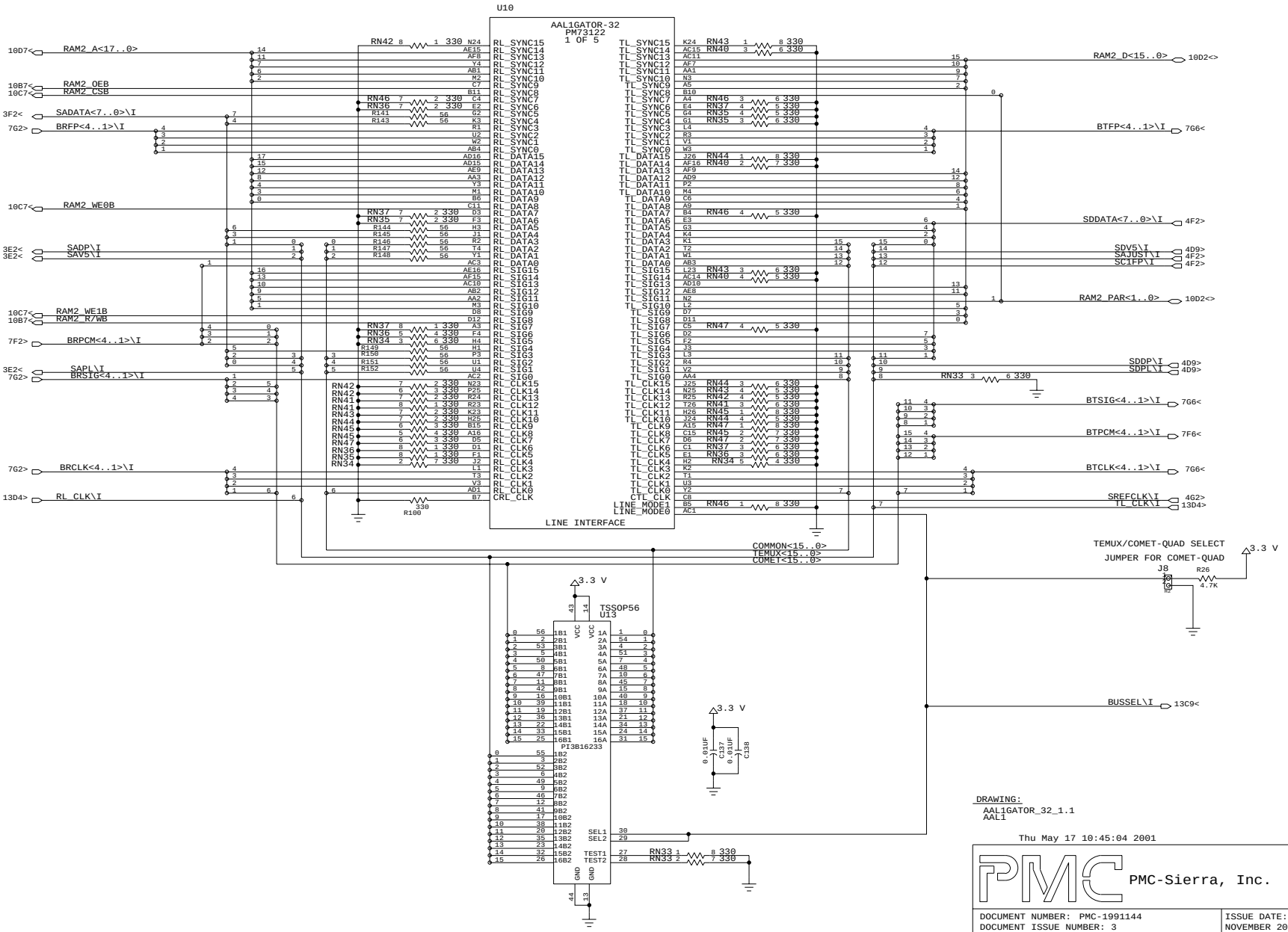

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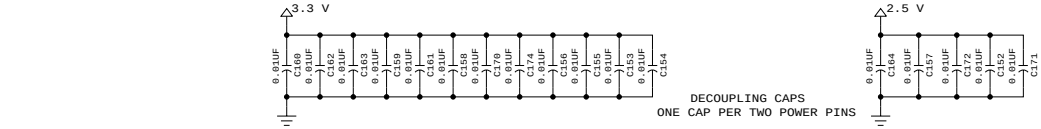
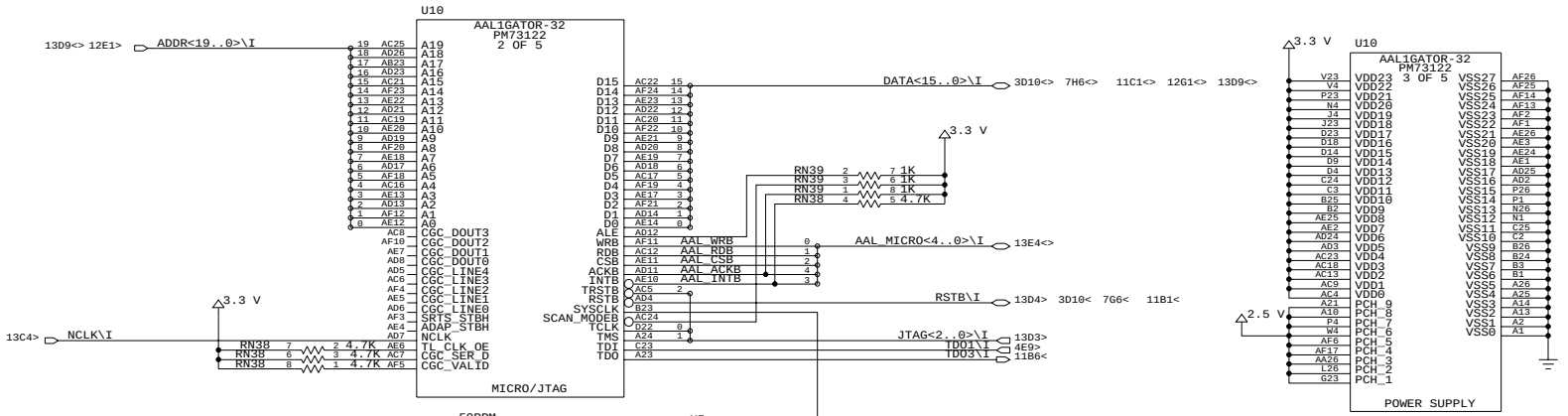
Thu May 17 10:45:04 2001

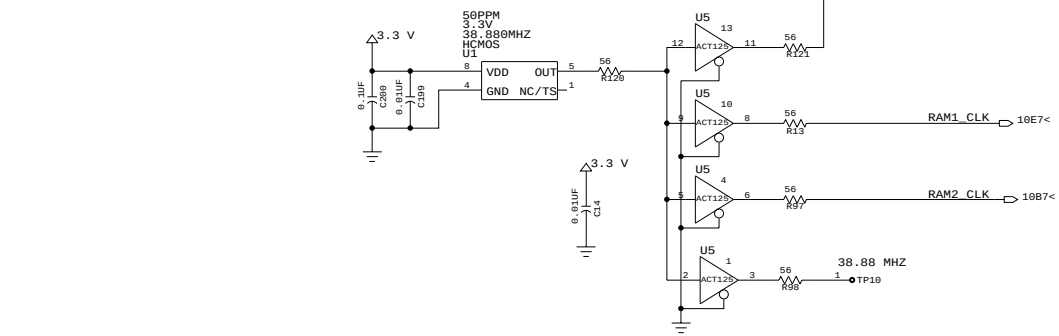
PMC-Sierra, Inc.

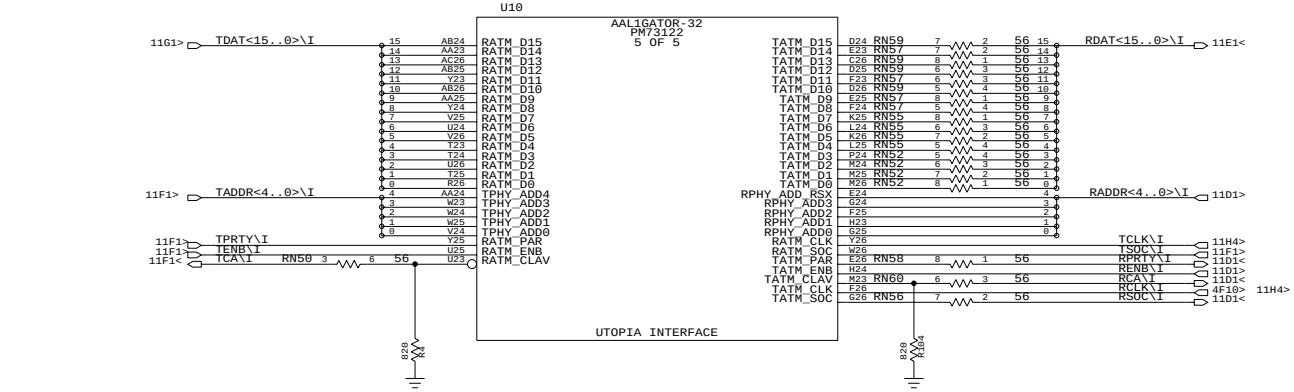
DOCUMENT NUMBER: PMC-1991144 DOCUMENT ISSUE NUMBER: 3	ISSUE DATE: NOVEMBER 2000
TITLE: AAL1GATOR-32/TEMUX DEVELOPMENT KIT AAL1GATOR-32 LINE INTERFACE	REVISION NUMBER: 2.0
ENGINEER: BW	PAGE:8 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR









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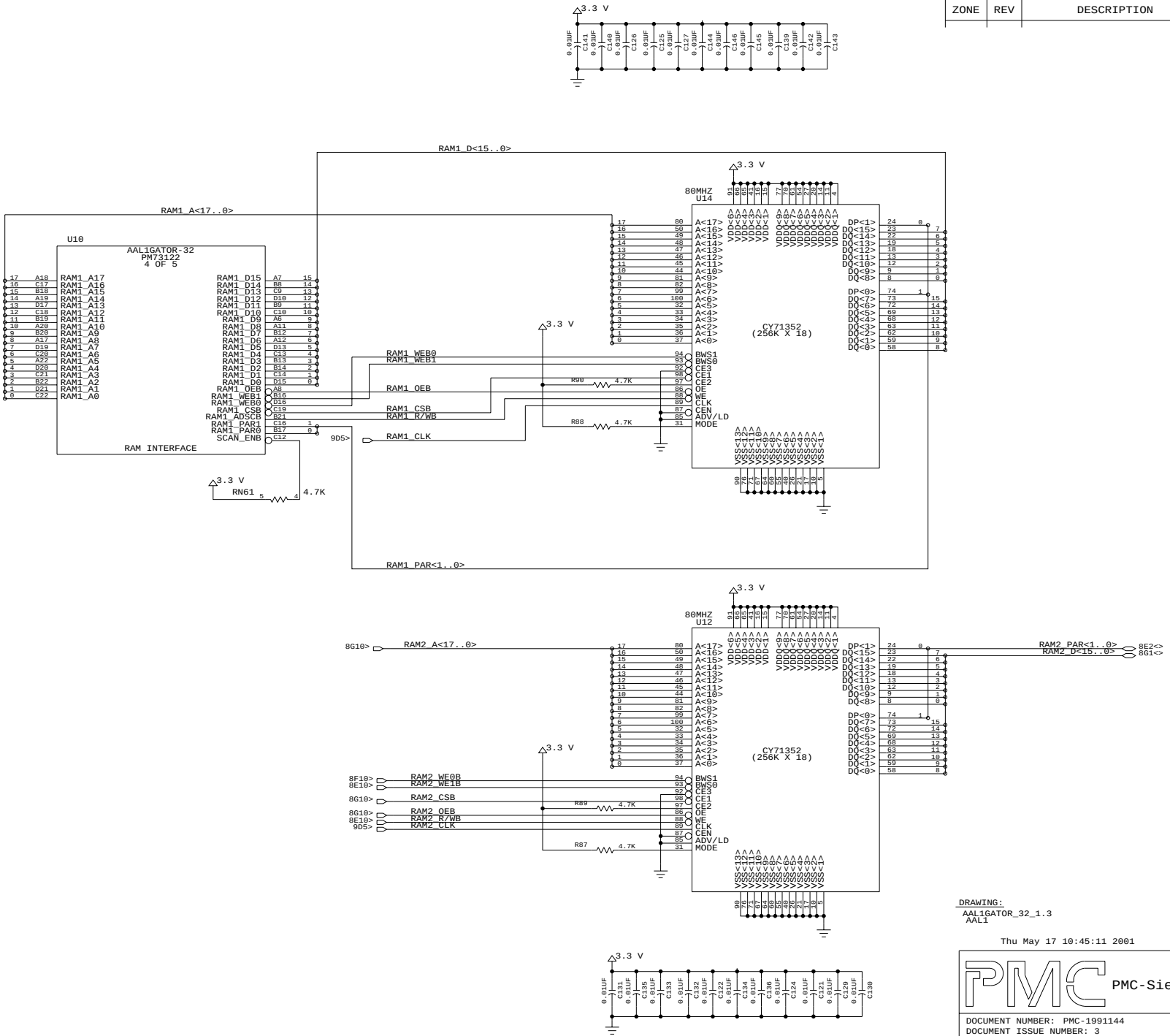
Thu May 17 10:45:07 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991144 DOCUMENT ISSUE NUMBER: 3	ISSUE DATE: NOVEMBER 2000
TITLE: AAL1GATOR-32/TEMUX DEVELOPMENT KIT AAL1GATOR-32_BLOCK 2	REVISION NUMBER: 2.0
ENGINEER: BW	PAGE:9 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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Thu May 17 10:45:11 2001

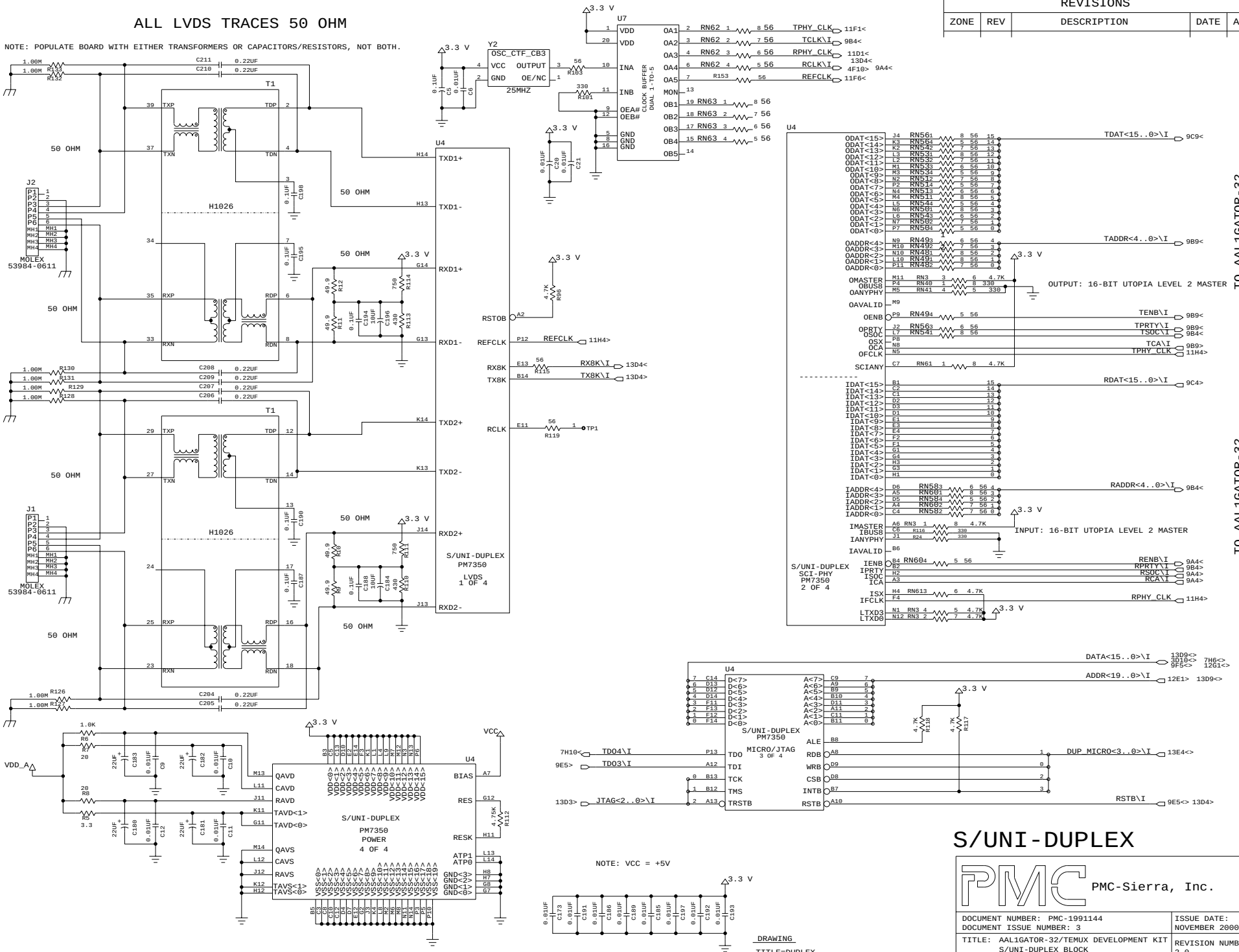
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991144 DOCUMENT ISSUE NUMBER: 3	ISSUE DATE: NOVEMBER 2000
TITLE: AAL1GATOR-32/TEMUX DEVELOPMENT KIT AAL1GATOR-32_BLOCK 3	REVISION NUMBER: 2.0
ENGINEER: BW	PAGE:10 OF 13

ALL LVDS TRACES 50 OHM

NOTE: POPULATE BOARD WITH EITHER TRANSFORMERS OR CAPACITORS/RESISTORS, NOT BOTH.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



NOTE: PLACE FILTER NETWORKS AS PHYSICALLY CLOSE TO THE DEVICE AS POSSIBLE.

ALTERNATE CAPS ON SUNI-DUPLEX VDD PINS

DRAWING

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ABBREV=DUPLEX
LAST_MODIFIED=Thu May 17 10:45:21 2001

S/UNI-DUPLEX

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991144 DOCUMENT ISSUE NUMBER: 3	ISSUE DATE: NOVEMBER 2000
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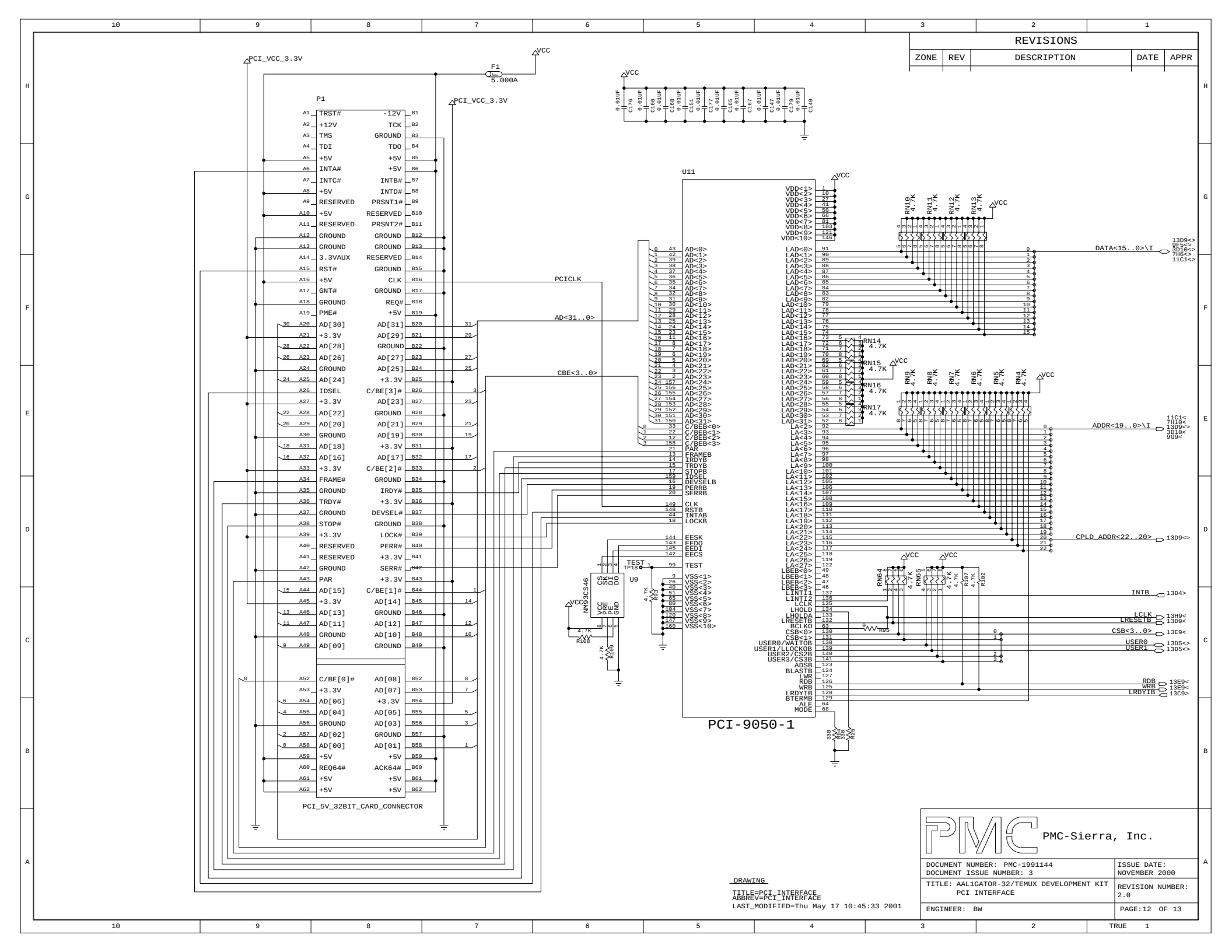
ENGINEER: BW	PAGE:11 OF 13


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
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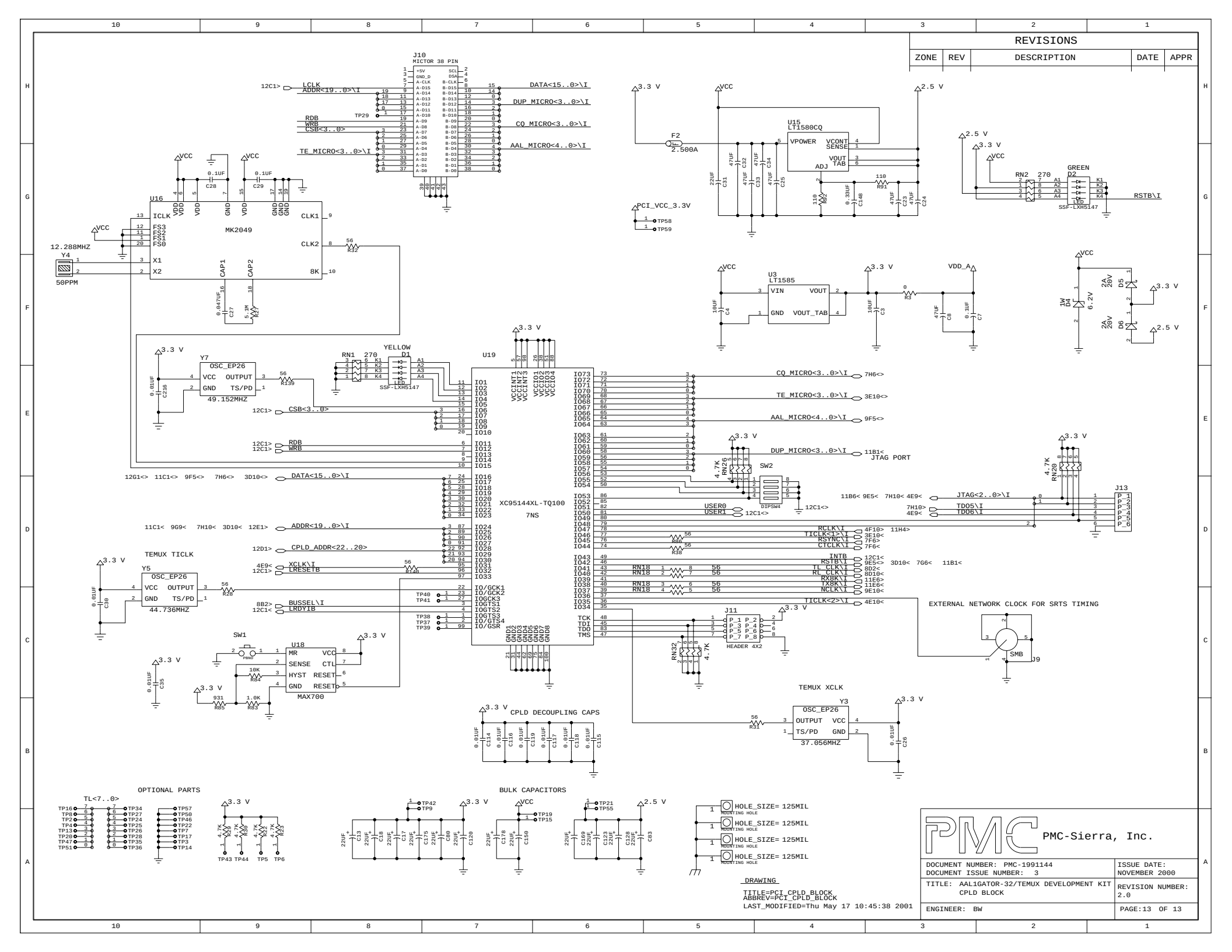
VCC
F1
5.000A
P1
PCI_5V_32BIT_CARD_CONNECTOR
PCICLK
AD<31..0>
CBE<3..0>
U11
PCI-9050-1
U9
NM93CS46
TEST
TP18
DATA<15..0>\I
ADDR<19..0>\I
CPLD_ADDR<22..20>
INTB
LCLK
LRESETB
CSB<3..0>
USER0
USER1
RDB
WRB
LRDYIB
PMC-Sierra, Inc.
DRAWING
TITLE=PCI INTERFACE
ABBREV=PCI_INTERFACE
LAST_MODIFIED=Thu May 17 10:45:33 2001
DOCUMENT NUMBER: PMC-1991144
DOCUMENT ISSUE NUMBER: 3
ISSUE DATE: NOVEMBER 2000
TITLE: AAL1GATOR-32/TEMUX DEVELOPMENT KIT PCI INTERFACE
REVISION NUMBER: 2.0
ENGINEER: BW
PAGE:12 OF 13


REVISIONS
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MICTOR 38 PIN
LCLK
ADDR<19..0>\I
RDB
WRB
CSB<3..0>
TE_MICRO<3..0>\I
DATA<15..0>\I
DUP_MICRO<3..0>\I
CQ_MICRO<3..0>\I
AAL_MICRO<4..0>\I
U16
MK2049
ICLK
FS3
FS2
FS1
FS0
CLK1
CLK2
8K
CAP1
CAP2
12.288MHZ
50PPM
U15
LT1580CQ
VPOWER
VCONT
SENSE
VOUT
TAB
ADJ
F2
2.500A
PCI_VCC_3.3V
U3
LT1585
VIN
VOUT
GND
VOUT_TAB
VDD_A
RSTB\I
GREEN
YELLOW
SSF-LXH5147
U19
XC95144XL-TQ100
7NS
Y7
OSC_EP26
49.152MHZ
Y5
44.736MHZ
TEMUX TICLK
Y3
37.056MHZ
TEMUX XCLK
SW1
SW2
DIPSW4
USER0
USER1
JTAG PORT
J13
J11
HEADER 4X2
J9
SMB
EXTERNAL NETWORK CLOCK FOR SRTS TIMING
U18
MAX700
CPLD_ADDR<22..20>
XCLK\I
LRESETB
BUSSEL\I
LRDYIB
JTAG<2..0>\I
TDO5\I
TDO6\I
RCLK\I
TICLK<1>\I
RSYNC\I
CTCLK\I
INTB
RSTB\I
TL_CLK\I
RL_CLK\I
RX8K\I
TX8K\I
NCLK\I
TICLK<2>\I
CPLD DECOUPLING CAPS
OPTIONAL PARTS
TL<7..0>
BULK CAPACITORS
HOLE_SIZE= 125MIL
MOUNTING HOLE
DRAWING
TITLE=PCI_CPLD_BLOCK
ABBREV=PCI_CPLD_BLOCK
LAST_MODIFIED=Thu May 17 10:45:38 2001
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-1991144
DOCUMENT ISSUE NUMBER: 3
ISSUE DATE: NOVEMBER 2000
TITLE: AAL1GATOR-32/TEMUX DEVELOPMENT KIT CPLD BLOCK
REVISION NUMBER: 2.0
ENGINEER: BW
PAGE:13 OF 13

14 APPENDIX C: VHDL CODE FOR CPLD

```
-- ------------------------------------------------------------------
-- Project  : PMC-991144
-- File Name      : AAL32.vhd
-- Path           :
-- Designer :
--
-- Revision History
-- Issue    Date        Initials    Description
-- 1        02/12/00    BW          Initial Release
--
-- Function
-- Implements the functionality of the AAL1gator-32/TEMUX Development
-- kit CPLD.
-- ------------------------------------------------------------------

library IEEE;
use IEEE.std_logic_1164.all;

entity AAL32_CPLD is

    port (

      LRESETB    : in STD_LOGIC;
      RSTB       : out STD_LOGIC;
      MAXRESET   : in STD_LOGIC;
      TRSTB      : out STD_LOGIC;
      TRSTB_JTAG : in STD_LOGIC;
      NETCLKIN   : in STD_LOGIC;
      NCLK     : out STD_LOGIC;
      OSC44M          : in STD_LOGIC;
      CLK2     : in STD_LOGIC;
      TICLK1          : out STD_LOGIC;
      TICLK2          : out STD_LOGIC;
      CSB0     : in STD_LOGIC;
      CSB1     : in STD_LOGIC;
      CSB2     : in STD_LOGIC;
      CSB3     : in STD_LOGIC;
      CSB_DUPLEX : out STD_LOGIC;
      CSB_AAL32  : out STD_LOGIC;
      CSB_CQ          : out STD_LOGIC;
      CSB_TEMUX  : out STD_LOGIC;
      RDB      : in STD_LOGIC;
      RDB_DUPLEX : out STD_LOGIC;
      RDB_AAL32  : out STD_LOGIC;
```

```
      RDB_CQ          : out STD_LOGIC;
      RDB_TEMUX   : out STD_LOGIC;
      WRB       : in STD_LOGIC;
      WRB_DUPLEX : out STD_LOGIC;
      WRB_AAL32   : out STD_LOGIC;
      WRB_CQ          : out STD_LOGIC;
      WRB_TEMUX   : out STD_LOGIC;
      LRDYIB          : out  STD_LOGIC;
      ACKB_AAL32 : in STD_LOGIC;
      INTB      : out STD_LOGIC;
      INTB_DUPLEX : in STD_LOGIC;
      INTB_AAL32   : in STD_LOGIC;
      INTB_CQ         : in STD_LOGIC;
      INTB_TEMUX : in STD_LOGIC;
      TEMUX_XCLK : out STD_LOGIC;
      OSC49M          : in STD_LOGIC;
      OSC37M          : in STD_LOGIC;
      DIPSW     : in STD_LOGIC_VECTOR (3 downto 1);
      LED       : out STD_LOGIC_VECTOR (3 downto 0);
      TX8K      : out STD_LOGIC;
      RX8K      : in STD_LOGIC;
      ICLK      : out STD_LOGIC;
      CTCLK     : out STD_LOGIC;
      RCLK      : in STD_LOGIC;
      RSYNC     : in STD_LOGIC;
      TL_CLK          : out STD_LOGIC;
      RL_CLK          : out STD_LOGIC

       );
    end AAL32_CPLD;

architecture AAL32_CPLD_arch of AAL32_CPLD is

    component divide_2
       port (
        clk_in     : in STD_LOGIC;
      reset    : in STD_LOGIC;
      clk_out      : out STD_LOGIC
       );
    end component;

    component divide_5592
       port (
        clk_in     : in STD_LOGIC;
      reset    : in STD_LOGIC;
      clk_out      : out STD_LOGIC
       );
```

```
end component;

component Mux_2                  -- Mux: sel = '0' selects Din_A
    port (                         --      sel = '1' selects Din_B
        sel     : in STD_LOGIC;
        Din_A   : in STD_LOGIC;
        Din_B   : in STD_LOGIC;
        Dout    : out STD_LOGIC
    );
end component;

component T_delay
   port (
  clk_in   : in STD_LOGIC;
  reset    : in STD_LOGIC;
  sig_in   : in STD_LOGIC;
  sig_out  : out STD_LOGIC
  );
end component;

signal DS3_8k   : STD_LOGIC;
signal TICLK    : STD_LOGIC;
signal reset    : STD_LOGIC;

begin

  RDB_DUPLEX <= RDB;         -- Provide Read enable to DUPLEX
  RDB_AAL32 <= RDB;    -- Provide Read enable to AAL1gator-32
  RDB_CQ <= RDB;       -- Provide Read enable to COMET-Quad
  RDB_TEMUX <= RDB;          -- Provide Read enable to TEMUX

  WRB_DUPLEX <= WRB;         -- Provide Write Strobe to DUPLEX
  WRB_AAL32 <= WRB;          -- Provide Write Strobe to AAL1gator-32
  WRB_CQ <= WRB;       -- Provide Write Strobe to COMET-Quad
  WRB_TEMUX <= WRB;          -- Provide Write Strobe to TEMUX

  CSB_DUPLEX <= CSB3;        -- Provide Chip Select to DUPLEX
  CSB_AAL32 <= CSB0;         -- Provide Chip Select to AAL1gator-32
  CSB_CQ <= CSB2;      -- Provide Chip Select to COMET-Quad
  CSB_TEMUX <= CSB1;         -- Provide Chip Select to TEMUX

  LRDYIB <= ACKB_AAL32;      -- Provide Chip Select to TEMUX

  LED(0) <= not(INTB_AAL32);       -- Displays a AAL1gator-32 interrupt
  LED(1) <= not(INTB_TEMUX);       -- Displays a TEMUX interrupt
  LED(2) <= not(INTB_CQ);          -- Displays a COMET-Quad interrupt
  LED(3) <= not(INTB_DUPLEX);      -- Displays a DUPLEX interrupt
```

```
      ICLK <= RX8K;               -- 8k reference clk from DUPLEX to PLL and
then AAL1gator-32
      CTCLK <= RX8K;            -- 8k reference clk from DUPLEX to COMET-Quad
for reference

      TICLK1 <= TICLK;    -- First TICLK for TEMUX input
      TICLK2 <= TICLK;    -- Second TICLK for TEMUX when LOS on LIU
      TL_CLK <= TICLK;    -- TL_CLK for AAL1gator-32

      RL_CLK <= RCLK;           -- RL_CLK for AAL1gator-32

      reset <= LRESETB AND MAXRESET;
      RSTB <= reset;
      TRSTB <= reset AND TRSTB_JTAG;

      INTB <= INTB_DUPLEX AND INTB_AAL32 AND INTB_CQ AND INTB_TEMUX;

      -- instantiate the network clock divider

      Network_Clk_Divider : divide_2
        port map(
          clk_in => NETCLKIN,
          reset => reset,
          clk_out => NCLK
      );

      -- instantiate the TEMUX XCLK mux

      TEMUX_XCLK_Mux : Mux_2        -- '0' selects Din_A
      port map(               -- '1' selects Din_B
          sel => not(DIPSW(1)),     -- This allows the selection of clocks
          Din_A => OSC37M,          -- T1 Mode
          Din_B => OSC49M,          -- E1 Mode
          Dout => TEMUX_XCLK
      );

      -- instantiate the RCLK divider

      RClk_Divider : divide_5592
        port map(
          clk_in => RCLK,
          reset => reset,
          clk_out => DS3_8k
      );

      -- instantiate the TX8K_Mux
```

```
      TX8K_Mux : Mux_2        -- '0' selects Din_A
      port map(               -- '1' selects Din_B
          sel => not(DIPSW(2)),     -- This allows the selection of clocks
          Din_A => DS3_8k,          -- TEMUX Reference
          Din_B => RSYNC,           -- COMET-Quad Reference
          Dout => TX8K
      );

      -- instantiate the TICLK mux

      TICLK_Mux : Mux_2       -- '0' selects Din_A
      port map(               -- '1' selects Din_B
          sel => not(DIPSW(3)),     -- This allows the selection of clocks
          Din_A => OSC44M,          -- From oscillator
          Din_B => CLK2,            -- PLL Clock from DUPLEX RX8K
          Dout => TICLK
      );


end AAL32_CPLD_arch;


-- ------------------------------------------------------------------
-- Project  : PMC-1991144
-- File Name      : Mux_2.vhd
-- Path           :
-- Designer :
--
-- Revision History
-- Issue    Date        Initials    Description
-- 1        07/00       BW          Initial Release
--
-- Function
-- This is a Mux with one select line that will select between
-- one input or a second input.
--
-- ------------------------------------------------------------------

library IEEE;
use IEEE.std_logic_1164.all;

entity mux_2 is
    port(
        sel     : in STD_LOGIC;
        Din_A   : in STD_LOGIC;
        Din_B   : in STD_LOGIC;
        Dout    : out STD_LOGIC
        );
end mux_2;

architecture mux_2_arch of mux_2 is
```

```
    begin
    Mux : process(sel, Din_A, Din_B)
        begin
        if sel = '0' then
          Dout <= Din_A;
      elsif sel = '1' then
          Dout <= Din_B;
      end if;
        end process;
end mux_2_arch;


-- ------------------------------------------------------------
-- Project  : PMC-1991144
-- File Name      : Clk_Divide2.vhd
-- Path           :
-- Designer :
--
-- Revision History
-- Issue    Date        Initials    Description
-- 1        07/00       BW          Initial Release
--
-- Function
-- This code implements a clock divider. It will divide the clock by
-- 2.
--
-- ------------------------------------------------------------------

library IEEE;
use IEEE.std_logic_1164.all;

entity divide_2 is
    port(
      clk_in      : in STD_LOGIC := '1';
      reset : in STD_LOGIC := '1';
      clk_out : out STD_LOGIC
      );
    end divide_2;

architecture divide_2_arch of divide_2 is

    constant divide_by : integer := 2;
    signal clk : STD_LOGIC := '1';

    begin

    divide : process(clk_in, reset)       -- this clock divides a clock by 2
    variable count : integer := 0;
    begin
      if reset = '0' then
          count := 0;
          clk_out <= '0';
      elsif (clk_in'event and clk_in = '1') then   -- rising edge
          count := count + 1;

          if count = (divide_by / 2) then
              clk_out <= clk;
```

```
              clk <= not(clk);
                    count := 0;
          end if;
        end if;

    end process;
end divide_2_arch;


-- ------------------------------------------------------------------
-- Project  : PMC-991144
-- File Name      : Clk_Divide5592.vhd
-- Path           :
-- Designer :
--
-- Revision History
-- Issue    Date        Initials    Description
-- 1        07/00       BW          Initial Release
--
-- Function
-- This code implements a clock divider. It will divide the clock by
-- 5592.
--
-- ------------------------------------------------------------------

library IEEE;
use IEEE.std_logic_1164.all;

entity divide_5592 is
    port(
      clk_in      : in STD_LOGIC := '1';
      reset : in STD_LOGIC := '1';
      clk_out : out STD_LOGIC
      );
    end divide_5592;

architecture divide_5592_arch of divide_5592 is

    constant divide_by : integer := 5592;
    signal clk : STD_LOGIC := '1';

    begin

    divide : process(clk_in, reset)       -- this clock divides a clock by
5592
    variable count : integer := 0;
    begin
      if reset = '0' then
          count := 0;
          clk_out <= '0';
      elsif (clk_in'event and clk_in = '1') then   -- rising edge
          count := count + 1;

          if count = (divide_by / 2) then
              clk_out <= clk;
              clk <= not(clk);
                    count := 0;
```

```
          end if;
        end if;

    end process;
end divide_5592_arch;
```

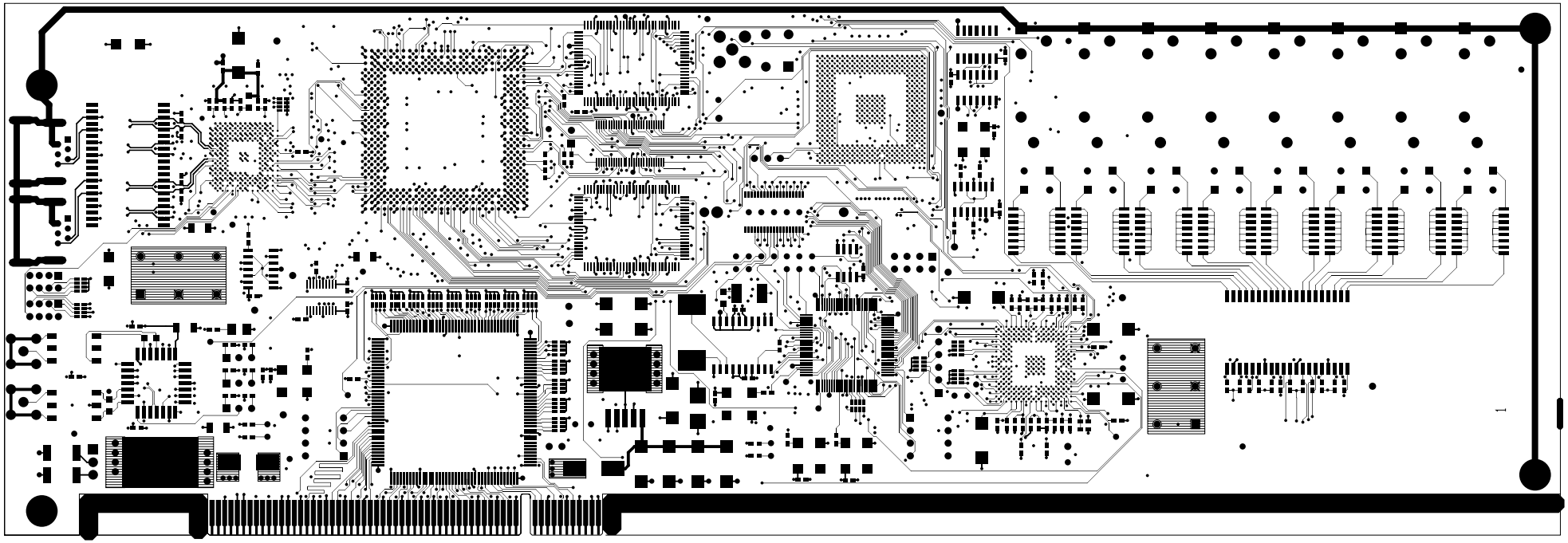
```
      // UCF file -- locking pin names to locations

      #PINLOCK_BEGIN

      NET "rsync"          LOC =  "S:PIN76";

      NET "rclk"           LOC =  "S:PIN78";

      NET "dipsw<1>"       LOC =  "S:PIN53";

      NET "osc37m"         LOC =  "S:PIN35";

      NET "osc49m"         LOC =  "S:PIN15";

      NET "netclkin"       LOC =  "S:PIN37";

      NET "intb_aal32"     LOC =  "S:PIN63";

      NET "intb_temux"     LOC =  "S:PIN68";

      NET "intb_cq"        LOC =  "S:PIN73";

      NET "intb_duplex"    LOC =  "S:PIN58";

      NET "csb0"           LOC =  "S:PIN19";

      NET "csb2"           LOC =  "S:PIN17";

      NET "csb3"           LOC =  "S:PIN16";

      NET "csb1"           LOC =  "S:PIN18";

      NET "rx8k"           LOC =  "S:PIN41";

      NET "rdb"            LOC =  "S:PIN6";

      NET "maxreset"       LOC =  "S:PIN97";

      NET "lresetb"        LOC =  "S:PIN96";

      NET "trstb_jtag"     LOC =  "S:PIN80";
```

```
NET "wrb"            LOC =  "S:PIN7";

NET "dipsw<3>"       LOC =  "S:PIN50";

NET "osc44m"         LOC =  "S:PIN22";

NET "clk2"           LOC =  "S:PIN9";

NET "dipsw<2>"       LOC =  "S:PIN52";

NET "led<0>"         LOC =  "S:PIN11";

NET "led<1>"         LOC =  "S:PIN12";

NET "led<2>"         LOC =  "S:PIN13";

NET "led<3>"         LOC =  "S:PIN14";

NET "csb_aal32"      LOC =  "S:PIN61";

NET "csb_cq"         LOC =  "S:PIN72";

NET "csb_duplex"     LOC =  "S:PIN56";

NET "csb_temux"      LOC =  "S:PIN67";

NET "ctclk"          LOC =  "S:PIN74";

NET "iclk"           LOC =  "S:PIN10";

NET "intb"           LOC =  "S:PIN49";

NET "nclk"           LOC =  "S:PIN39";

NET "rdb_aal32"      LOC =  "S:PIN60";

NET "rdb_cq"         LOC =  "S:PIN71";

NET "rdb_duplex"     LOC =  "S:PIN55";

NET "rdb_temux"      LOC =  "S:PIN66";

NET "rstb"           LOC =  "S:PIN46";

NET "temux_xclk"     LOC =  "S:PIN95";

NET "ticlk1"         LOC =  "S:PIN77";

NET "ticlk2"         LOC =  "S:PIN36";
```

```
NET "wrb_aal32"      LOC =  "S:PIN59";

NET "wrb_cq"         LOC =  "S:PIN70";

NET "wrb_duplex"     LOC =  "S:PIN54";

NET "wrb_temux"      LOC =  "S:PIN65";

NET "trstb"          LOC =  "S:PIN79";

NET "lrdyib"         LOC =  "S:PIN4";

NET "ackb_aal32"     LOC =  "S:PIN64";

NET "tx8k"           LOC =  "S:PIN40";

NET "tl_clk"           LOC =  "S:PIN43";

NET "rl_clk"           LOC =  "S:PIN42";


#PINLOCK_END
```

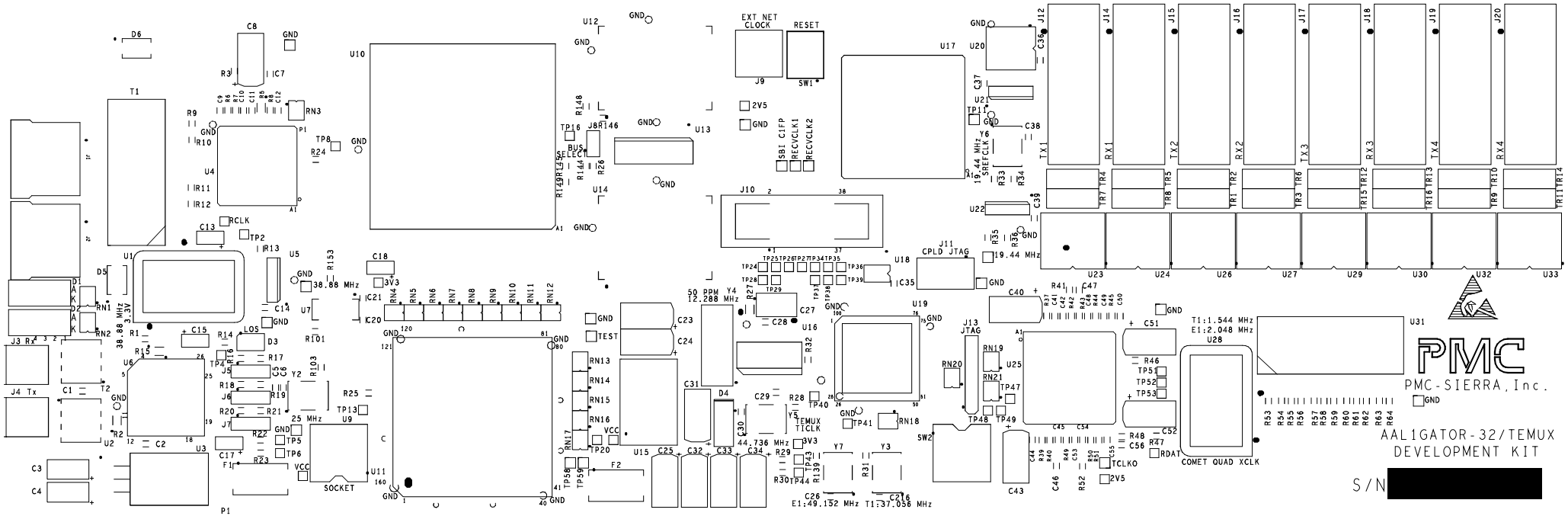
15 APPENDIX D: LAYOUT

TOP LAYER



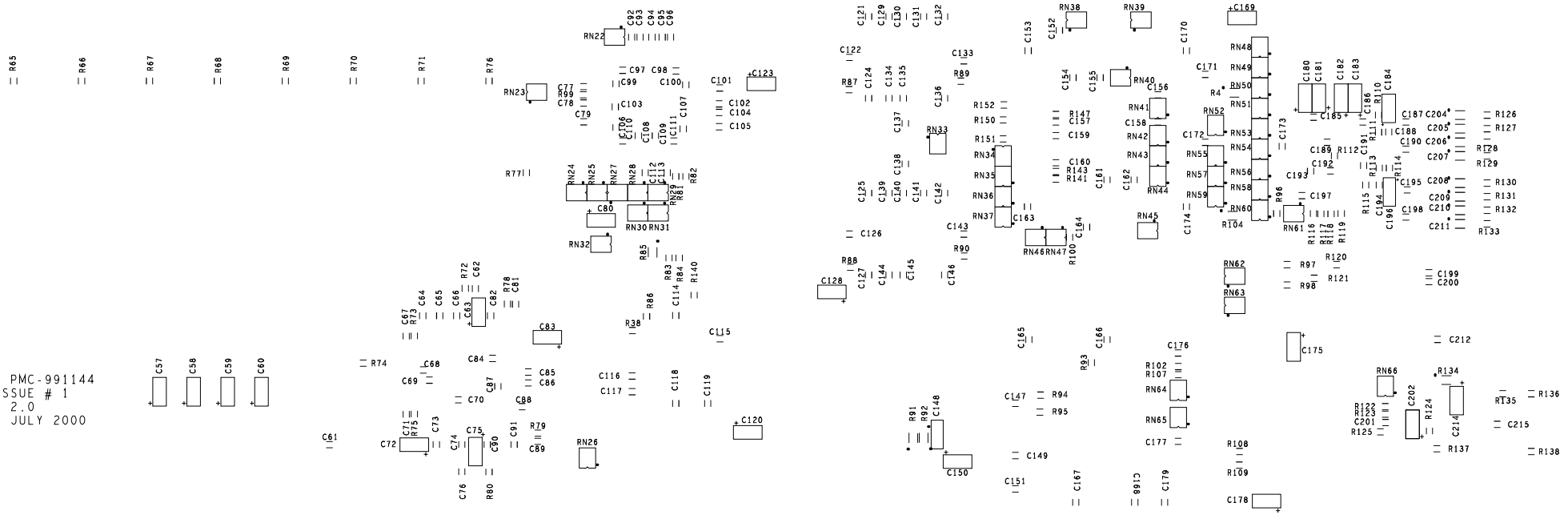
PMC-SIERRA AAL1GATOR-32/TEMUX DEV KIT 2000 REV2

SILK SCREEN TOP



PMC-SIERRA AAL1GATOR-32/TEMUX DEV KIT 2000 REV2

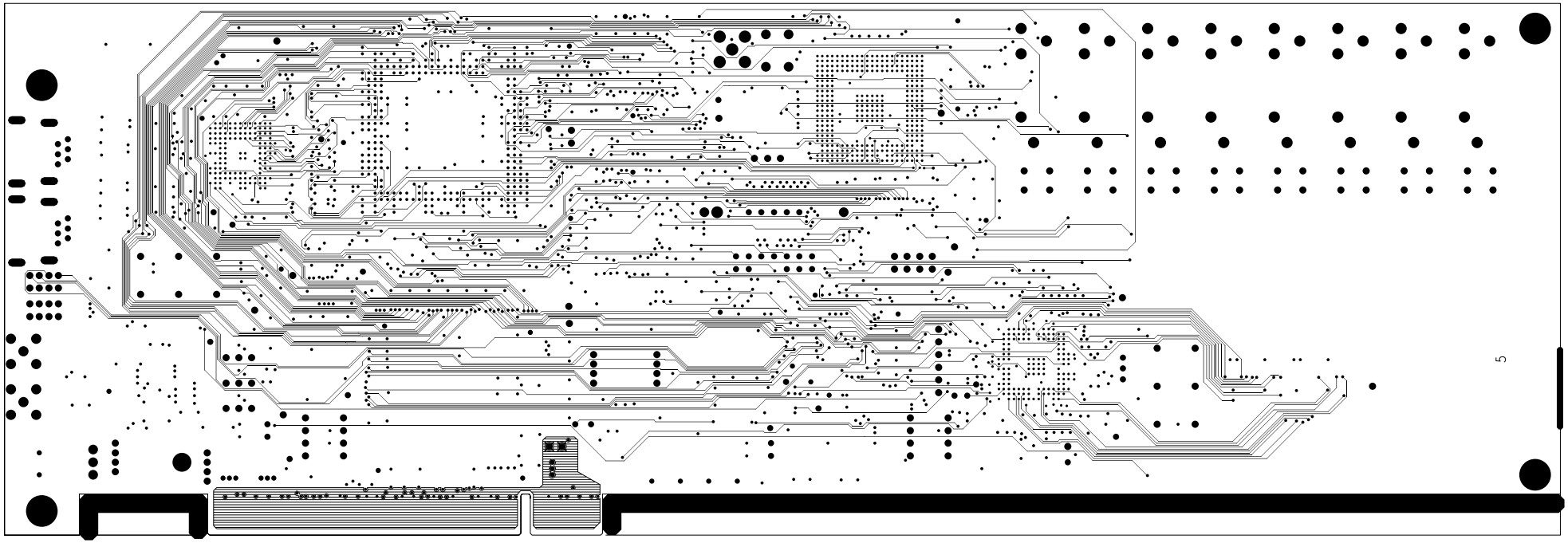
SILK SCREEN BOTTOM



DOC # PMC-991144
DOC ISSUE # 1
REV # 2.0
DATE: JULY 2000

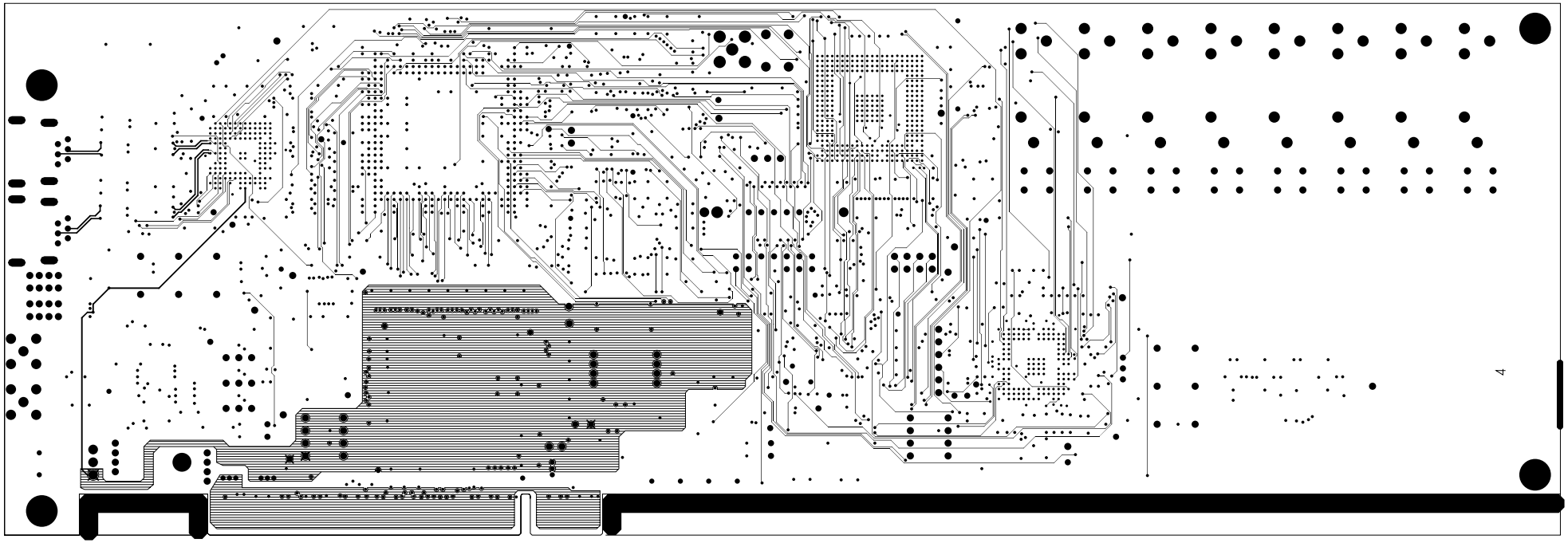
PMC-SIERRA AAL1GATOR-32/TEMUX DEV KIT 2000 REV2

SIG2



PMC-SIERRA AAL1GATOR-32/TEMUX DEV KIT 2000 REV2

SIG1



REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED

FINISHED HOLES SIZE			
All Units are in mils			
FIGURE	SIZE	PLATED	QTY
·	12.0	PLATED	623
·	13.0	PLATED	1607
·	25.0	PLATED	39
·	32.0	PLATED	87
·	36.0	PLATED	59
·	39.0	PLATED	8
·	42.0	PLATED	48
·	50.0	PLATED	40
·	52.0	PLATED	10
·	55.0	PLATED	5
·	79.0	PLATED	5
⊕	125.0	PLATED	4
⊕	150.0	PLATED	1
·	94.0	NOT PLATED	1

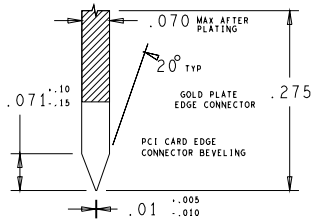
Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	-------
FR-4	DIELECTRIC	-------	-------	6 mil	4.5
COPPER	CONDUCTOR	GND_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	3.0 mil	4.5
COPPER	CONDUCTOR	2_5V_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	8.0 mil	4.5
COPPER	CONDUCTOR	SIG1	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	18 mil	4.5
COPPER	CONDUCTOR	SIG2	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	8.0 mil	4.5
COPPER	CONDUCTOR	3_3V_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	3 mil	4.5
COPPER	CONDUCTOR	GND2_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	6 mil	4.5
COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	-------

Note: All 11 mils traces are 50 Ohm controlled impedance.
All 5 mils traces are 75 Oms controlled impedance.

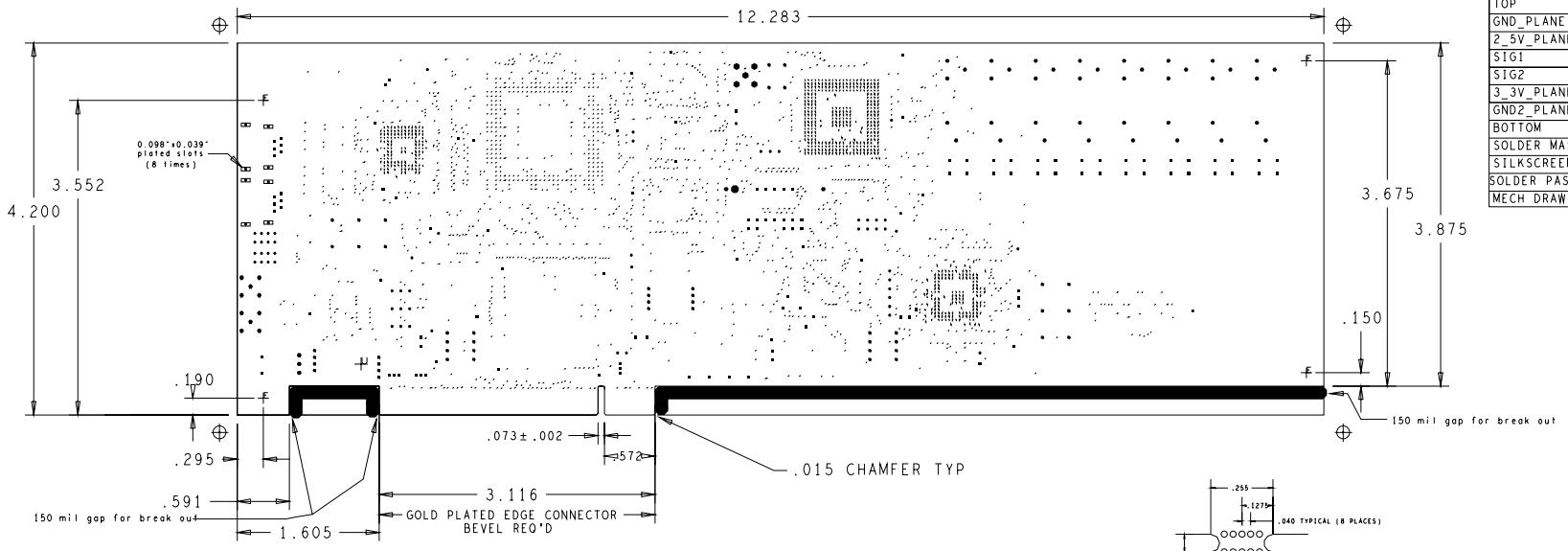
CAUTION !!

Notes:

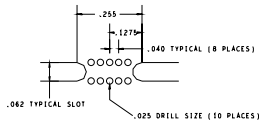
1. Copper thickness is 1/2 oz. on outer layers and 1 oz. on internal layers.
2. Total thickness of board shall be 62 mil +/- 7 mil.
3. The outline dimension are spedified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.
10. Plated holes marked with SQUARE R - 0.026" - should be within -0/+0.004" tolerance.
11. Add teardrops - if needed - to compensate for manufacturing process.



ARTWORK FILM
SOLDER PASTE TOP
SILKSCREEN TOP
SOLDER MASK TOP
TOP
GND_PLANE
2_5V_PLANE
SIG1
SIG2
3_3V_PLANE
GND2_PLANE
BOTTOM
SOLDER MASK BOTTOM
SILKSCREEN BOTTOM
SOLDER PASTE BOTTOM
MECH DRAWING



VIEW FROM COMPONENT SIDE B



PMC-SIERRA AAL1GATOR-32/TEMUX DEV KIT 2000 REV2

UNLESS OTHERWISE SPECIFIED		DATE YY	MM	DD
DIMENSIONS ARE IN INCHES	DRAWN			
TOLERANCES ON:				
2 PL DECIMALS ±	CHECKED			
3 PL DECIMALS ±	ENGRG			
ANGLES ±	ISSUED			
FRACTIONS ±				

DOC #: PMC-991144
DOC ISSUE #: 1
REV #: 2.0
DATE: JULY 2000

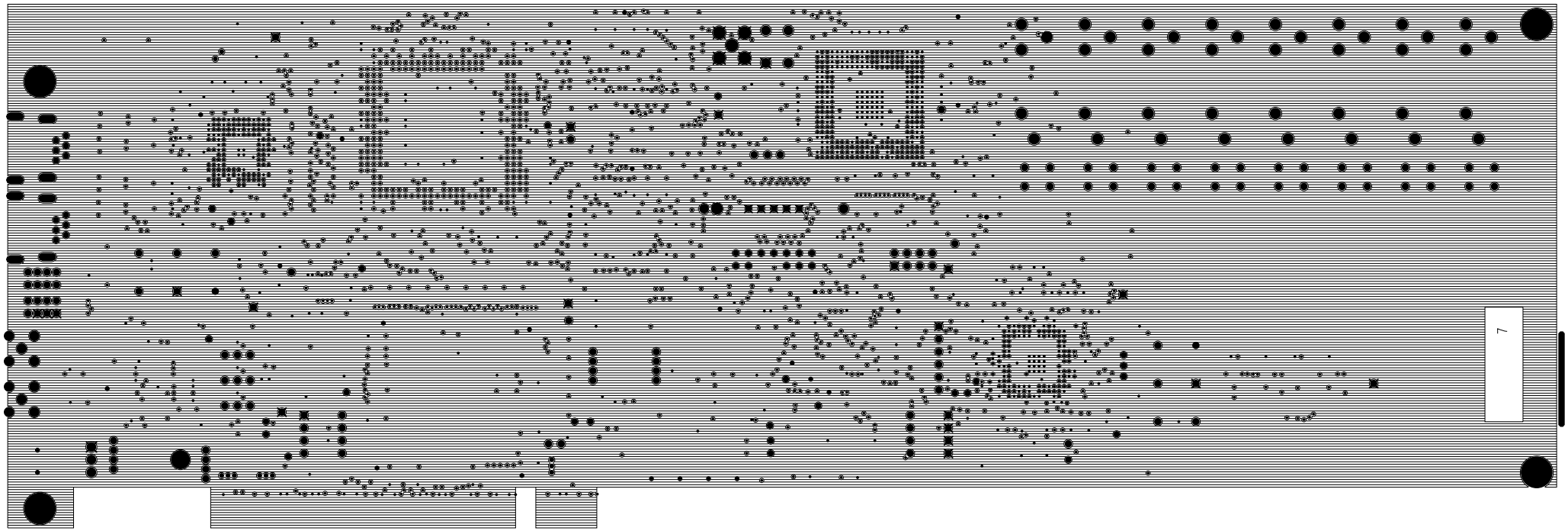
PMC-Sierra, Inc.

105-8555 Baxter Place, Burnaby B.C. Canada, V5A 4V7

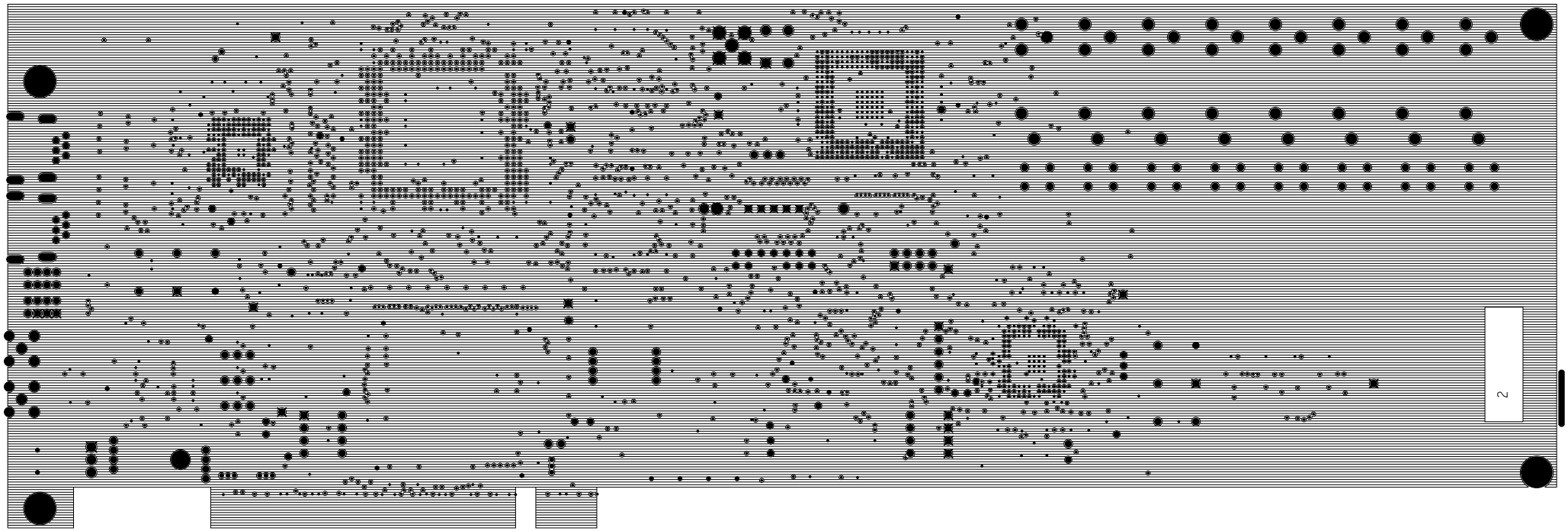
Tel: 604 415-6000 Fax: 604 415-6200

SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET OF

GND2_PLANE

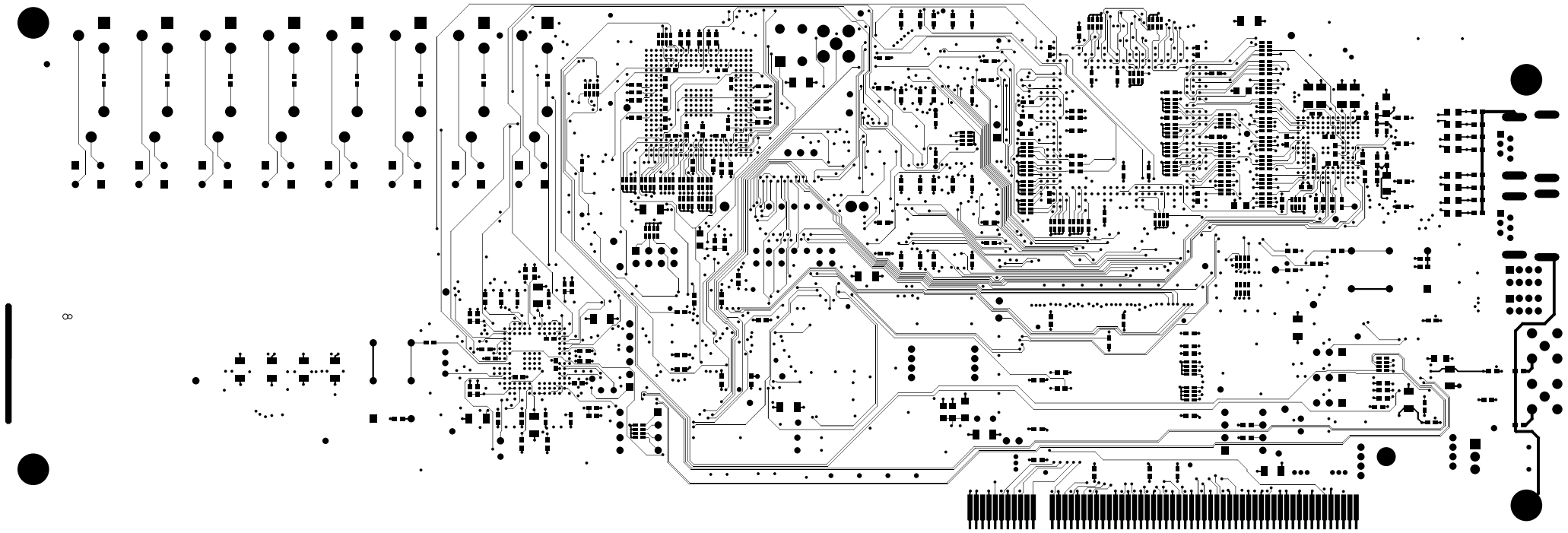


GND_PLANE



PMC-SIERRA AAL1GATOR-32/TEMUX DEV KIT 2000 REV2

BOTTOM LAYER



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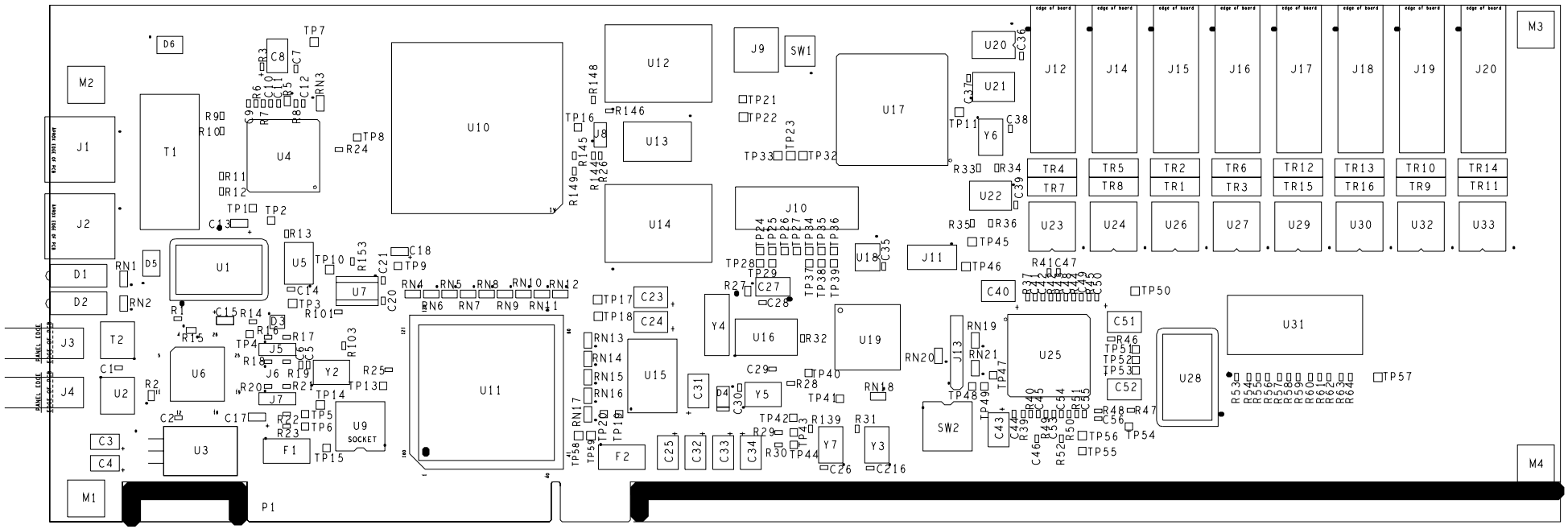
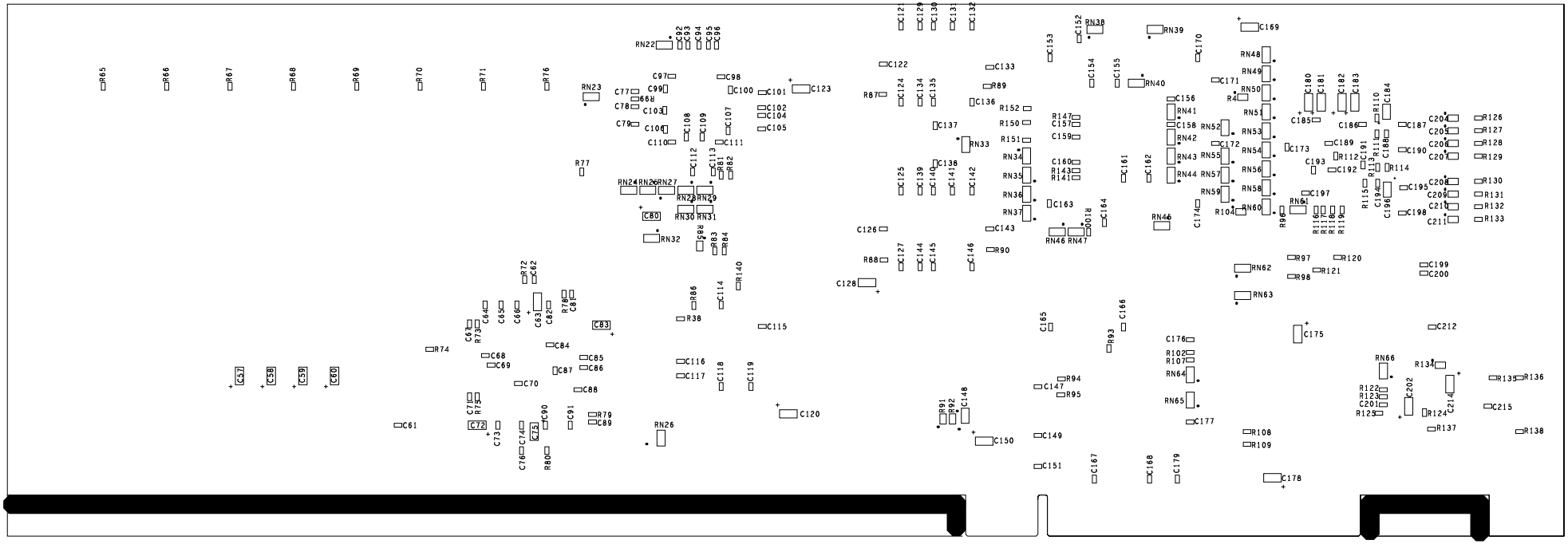
PMC-SIERRA AAL1GATOR-32/TEMUX DEV KIT 2000 REV2

ASSY TOP



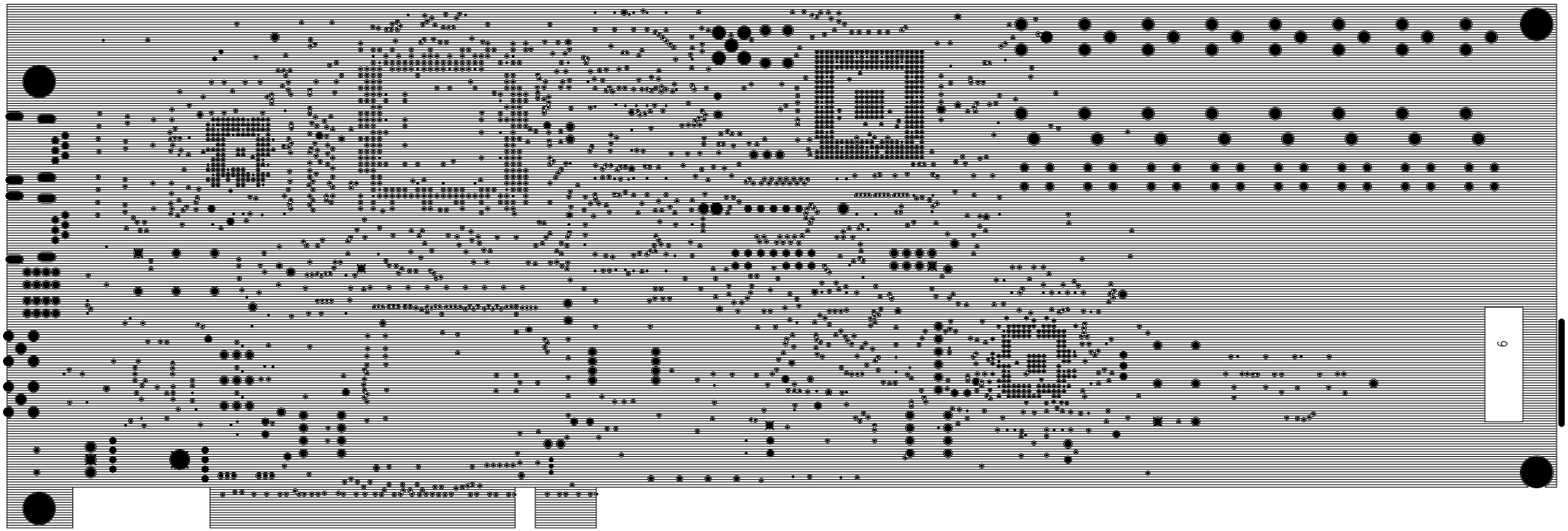
PMC-SIERRA AAL1GATOR-32/TEMUX DEV KIT 2000 REV2

ASSY BOTTOM

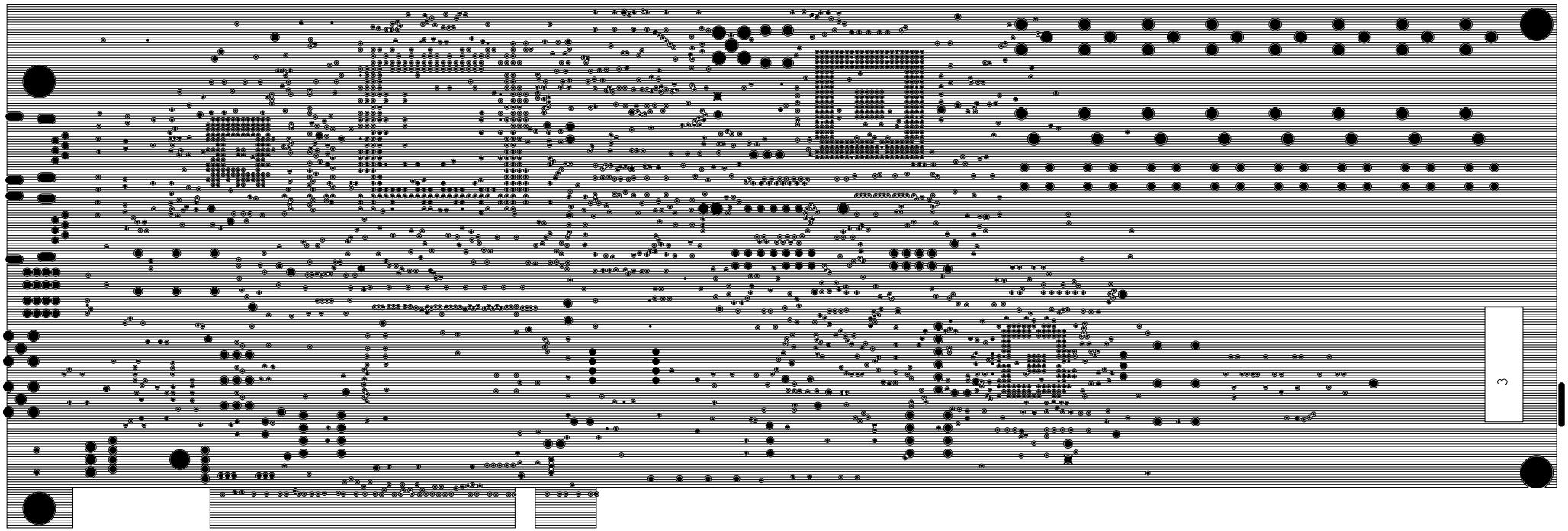


PMC-SIERRA AAL1GATOR-32/TEMUX DEV KIT 2000 REV2

3_3V_PLANE



2.5V PLANE



NOTES

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
(604) 415-4533
Web Site: http://www.pmc-sierra.com

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