NEC

MOS INTEGRATED CIRCUIT

# μPD7554A, 7554A(A)

## 4-BIT SINGLE-CHIP MICROCOMPUTER

### DESCRIPTION

The μPD7554A is a product of the μPD7554, 7564 sub-series which is a 4-bit single-chip microcomputer with a small number of ports in a small package, which is enabled to operate even at the super-low voltage of 2.0 V so that it is optimized for handy-type systems operating with dry cells. The μPD7554A is a low-order model in the μPD7500 series (μPD7554A only).

This device incorporates a serial interface, and serves as the sub-CPU for a high-order model of that series or the 8-bit microcomputer. It is optimized for distributed processing of the system.

The μPD7554A has outputs to directly drive a triac and LEDs and allows selection among many types of input/output circuits using their respective mask options, sharply reducing the number of external circuits required.

**Details of functions are described in the User's Manual shown below. Be sure to read in design.**
**μPD7554, 7564 User's Manual: IEM-1111D**

### FEATURES

- Range of supply voltage 7554A : 2.0 to 6.0 V
  7554A(A) : 2.7 to 6.0 V
- Drive with two 1.5 V manganese cells
- 47 types of instructions
  (Subset of μPD7500H SET B)
- Instruction cycle
  External clock : 2.86 μs (in operation at 700 kHz, 5 V)
  RC oscillation : 4 μs (in operation at 500 kHz, 5 V)
- Program memory (ROM) capacity: 1024 × 8 bits
- Data memory (RAM) capacity: 64 × 4 bits
- Test source: One external source and two internal sources
- 8-bit timer/event counter ★
- 16 I/O lines (Total output current of all pins: 100 mA)
  - Can directly drive a triac and a LED: P80 to P83
  - Can directly drive LEDs: P100 to P103 and P110 to P113
  - Mask option function provided for every port
- 8-bit serial interface
- Standby (STOP/HALT) function
- Low supply voltage data retaining function for data memory
- Built-in ceramic oscillator for system clock RC Oscillation with an external resistor R (Incorporating capacitor C)

### APPLICATION ★

μPD7554A : Sub-CPU including handy-type system, PPC, printer, VCR, audio equipments, etc.
μPD7554A(A) : Automotive and transportation equipments, etc.

**The quality level and absolute maximum ratings of the μPD7554A and the μPD7554A(A) differ.**
**Except where specifically noted, explanations here concern the μPD7554A as a representative product.**
**If you are using the μPD7554A(A), use the information presented here after checking the functional differences.**



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The mark ★ shows major revised points.

## ORDERING INFORMATION

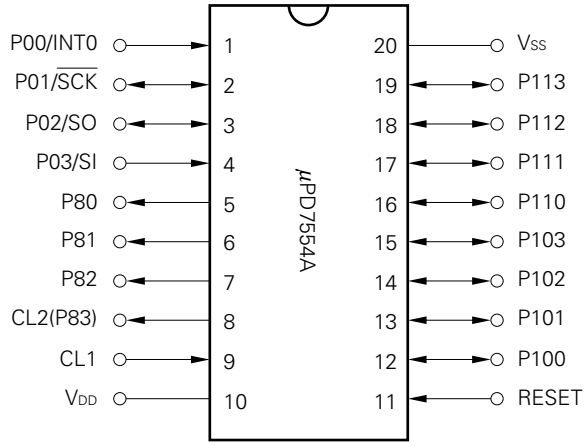
| | Ordering Code | Package | Quality Grade |
|---|---|---|---|
| | μPD7554ACS-×××| 20-pin plastic shrink DIP (300 mil) | Standard |
| | μPD7554AG-××× | 20-pin plastic SOP (300 mil) | Standard |
| ★ | μPD7554ACS(A)-××× | 20-pin plastic shrink DIP (300 mil) | Special |
| ★ | μPD7554AG(A)-××× | 20-pin plastic SOP (300 mil) | Special |

**Caution Be sure to specify a mask option when ordering this device.**

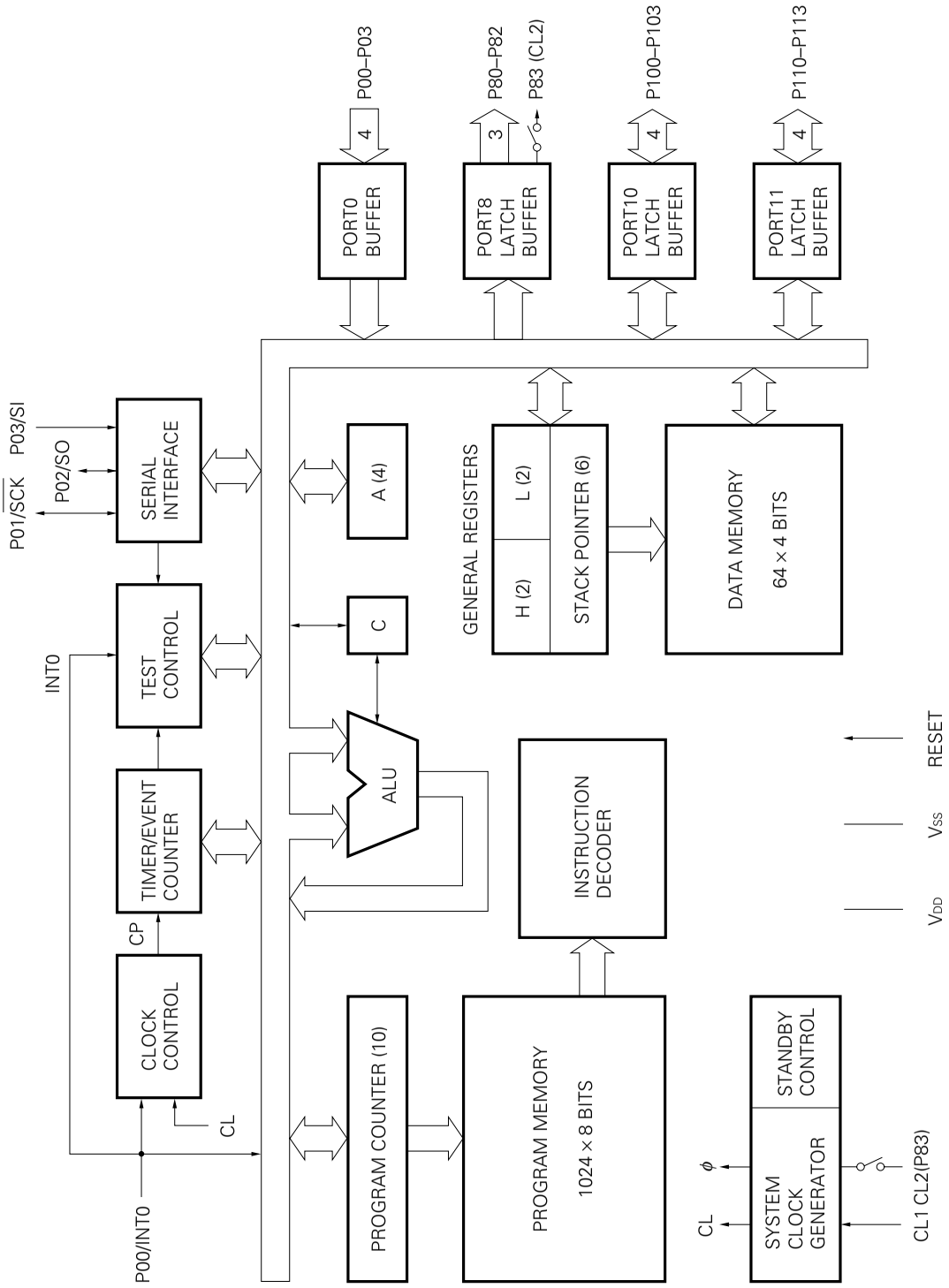
**Remarks** "×××" is a ROM code number.

Please rfer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

### PIN CONFIGURATION (TOP VIEW)



## BLOCK DIAGRAM OF μPD7554A



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# 1. PIN FUNCTIONS

## 1.1 PORT FUNCTIONS

| Pin Name | Input/Output | Dual-Function Pin | Function | After RESET | Input/Output Circuit |
|---|---|---|---|---|---|
| P00 | Input | INT0 | 4-bit input port (Port 0)<br>P00 serves also as a count clock (event pulse) input. | Input | S |
| P01 | Input/output | $\overline{SCK}$ | | | X |
| P02 | | SO | | | W |
| P03 | Input | SI | | | S |
| P80 to P82 | Output | — | 4-bit output port (Port 8)<br>High current (15 mA), middle-high voltage (9 V) output | High impedance | O |
| P83 Note | Output | CL2 | | | |
| P100 to P103 | Input/output | — | 4-bit I/O port (Port 10)<br>Middle-high current (10 mA), middle-high voltage (9 V) input/output | High impedance or high-level output | P |
| P110 to P113 | Input/output | — | 4-bit I/O port (Port 11)<br>Middle-high current (10 mA), middle-high voltage (9 V) input/output | | |

**Note** Mask options are available to specify port functions only when the external clock (CL1) is used.

## 1.2 OTHER THAN PORTS

| Pin Name | Input/Output | Dual-Function Pin | Function | After RESET | Input/Output Circuit |
|---|---|---|---|---|---|
| INT0 | Input | P00 | Edge detection testable input pin (Rising edge) | | S |
| $\overline{SCK}$ | Input/output | P01 | Serial clock Input/output pin | Input | X |
| SO | Output | P02 | Serial data output pin | Input | W |
| SI | Input | P03 | Serial data input pin | Input | S |
| CL1 | | | Connection pin for resistor R for RC oscillator<br>When an external clock is used, its input must be connected to CL1, and CL2 can be used as P83 using the mask option. | | Q |
| CL2 | | P83 | | | |
| RESET | | | System reset input pin (high-level active)<br>A pull-down resistor can be incorporated using the mask option. | | R |
| $V_{DD}$ | | | Positive power supply pin | | |
| $V_{SS}$ | | | GND potential pin | | |

### 1.3 PIN MASK OPTION

Each pin is provided with the following mask options which can be selected for each bit according to the purpose:

| Pin Name | Mask Options | |
|---|---|---|
| P00 | ① No internally provided resistor<br>③ Pull-up resistor internally provided | ② Pull-down resistor internally provided |
| P01 | ① No internally provided resistor<br>③ Pull-up resistor internally provided | ② Pull-down resistor internally provided |
| P02 | ① No internally provided resistor<br>③ Pull-up resistor internally provided | ② Pull-down resistor internally provided |
| P03 | ① No internally provided resistor<br>③ Pull-up resistor internally provided | ② Pull-down resistor internally provided |
| P80 | ① N-channel open-drain output | ② CMOS (push-pull) output |
| P81 | ① N-channel open-drain output | ② CMOS (push-pull) output |
| P82 | ① N-channel open-drain output | ② CMOS (push-pull) output |
| P83/CL2 | ① Used as CL2 or P83N-ch open-drain output pin. | ② Used as P83 pin (push-pull output). |
| P100 | ① N-channel open-drain I/O<br>③ N-channel open-drain + I/O with pull-up resistor internally provided | ② Push-pull I/O |
| P101 | ① N-channel open-drain I/O<br>③ N-channel open-drain + I/O with pull-up resistor internally provided | ② Push-pull I/O |
| P102 | ① N-channel open-drain I/O<br>③ N-channel open-drain + I/O with pull-up resistor internally provided | ② Push-pull I/O |
| P103 | ① N-channel open-drain I/O<br>③ N-channel open-drain + I/O with pull-up resistor internally provided | ② Push-pull I/O |
| P110 | ① N-channel open-drain I/O<br>③ N-channel open-drain + I/O with pull-up resistor internally provided | ② Push-pull I/O |
| P111 | ① N-channel open-drain I/O<br>③ N-channel open-drain + I/O with pull-up resistor internally provided | ② Push-pull I/O |
| P112 | ① N-channel open-drain I/O<br>③ N-channel open-drain + I/O with pull-up resistor internally provided | ② Push-pull I/O |
| P113 | ① N-channel open-drain I/O<br>③ N-channel open-drain + I/O with pull-up resistor internally provided | ② Push-pull I/O |
| System clock[Note] | ① RC oscillation | ② External clock |
| RESET | ① Pull-down resistor is not internally provided | ② Pull-down resistor is internally provided |

★

**Note** When using RC oscillation, switch the P83/CL2 pin to the CL2 pin.

There is no mask option for PROM products. For more information, see the μPD75P54 Data Sheet (IC-2830).

### 1.4 CAUTION ON USE OF P00/INT0 PIN AND RESET PIN

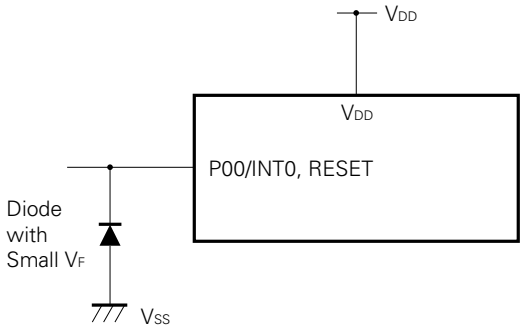
In addition to the functions shown in 1.1, 1.2 and 1.3, the P00/INT0 pin and RESET pin have a function for setting the test mode in which the internal operation of the μPD7554A is tested (IC test only).

When a potential greater than $V_{SS}$ is applied to either of these pins, the test mode is set. As a result, if noise exceeding $V_{SS}$ is applied during normal operation, the test mode will be entered and normal operation may be impeded.

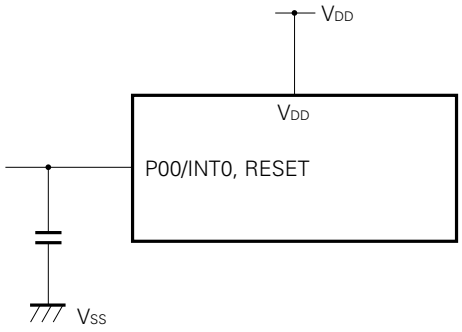
If, for example, the routing of the wiring between the P00/INT0 pin and RESET pin is long, the above problem may occur as the result of inter-wiring noise between these pins.

Therefore, wiring should be carried out so as to suppress inter-wiring noise as far as possible. If it is not possible to suppress noise, anti-noise measures should be taken using external parts as shown in the figures below.

- **Connection of diode with small $V_F$ between P00/INT4/RESET pin and $V_{SS}$**



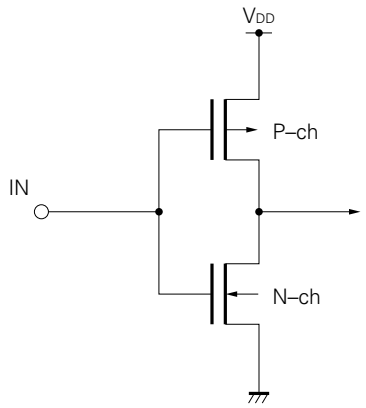

- **Connection of capacitor between P00/INT0/RESET pin and $V_{SS}$**



### 1.5 PIN INPUT/OUTPUT CIRCUITS

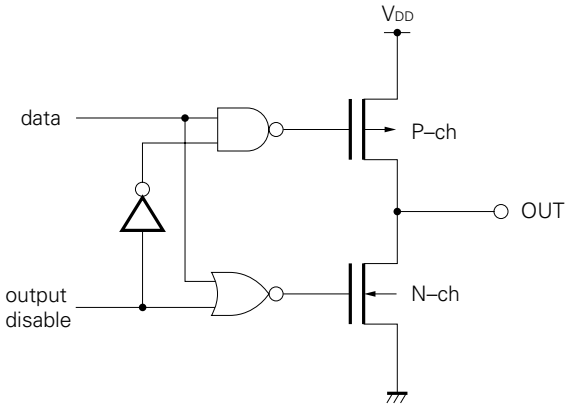
This section presents the input/output circuit for each pin of the μPD7554A in a partly simplified format:

(1) Type A (for Type W)



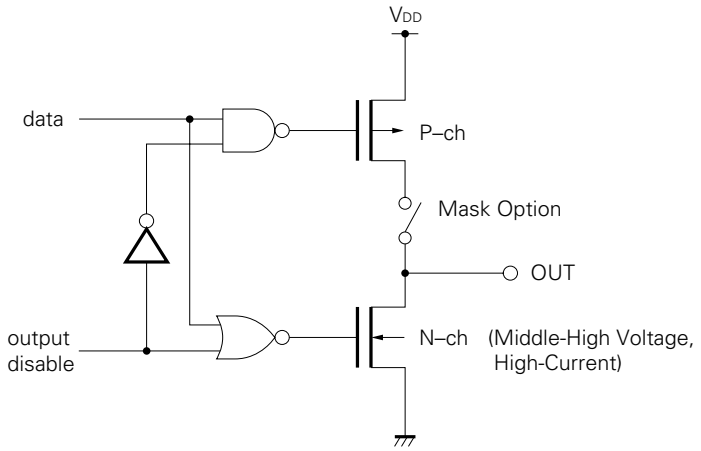

Forming an input buffer conformable to the CMOS specification

(2) Type D (for Types W and X)

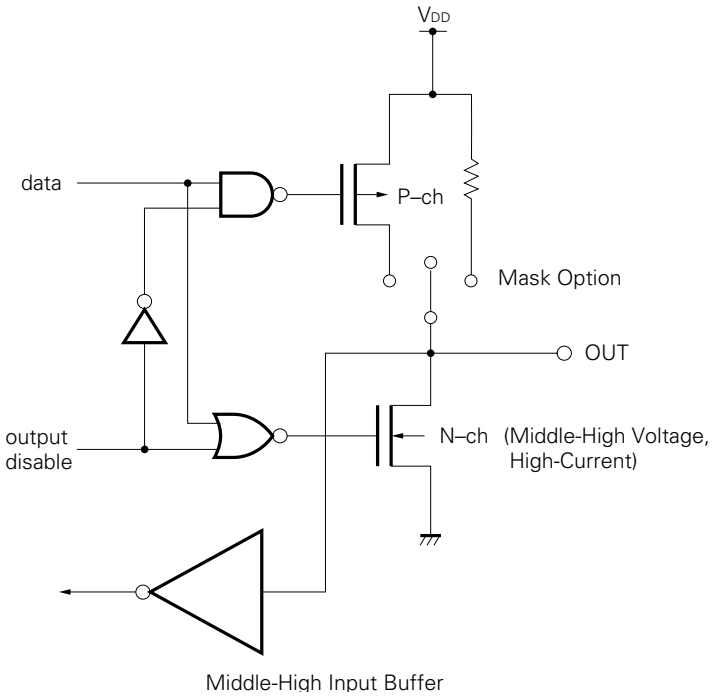



Forming a push-pull output which becomes high impedance (with both P-ch and N-ch off) in response to RESET input

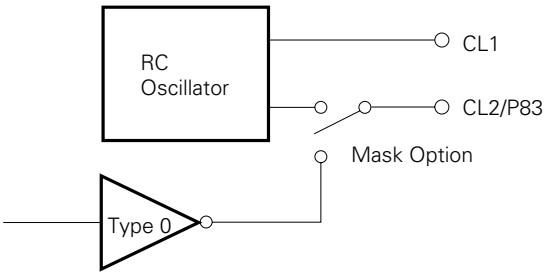
(3) Type O



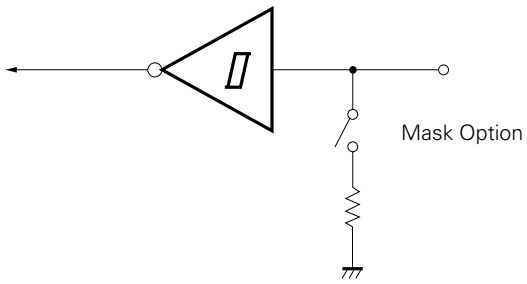

(4) Type P



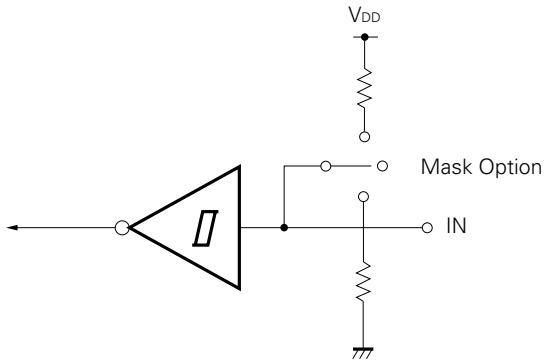

(5) Type Q



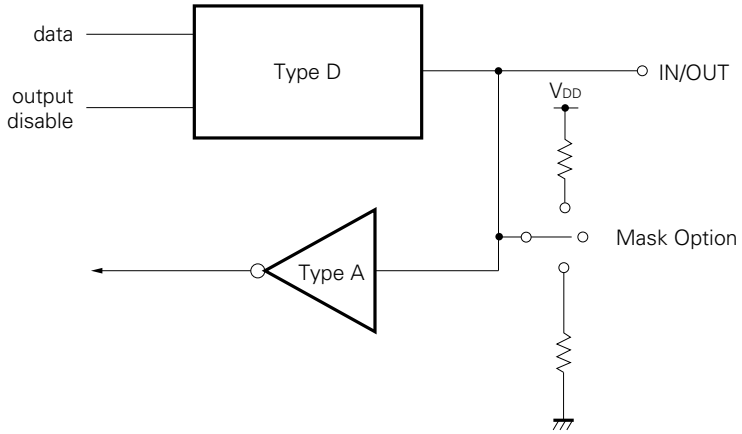
(6) Type R



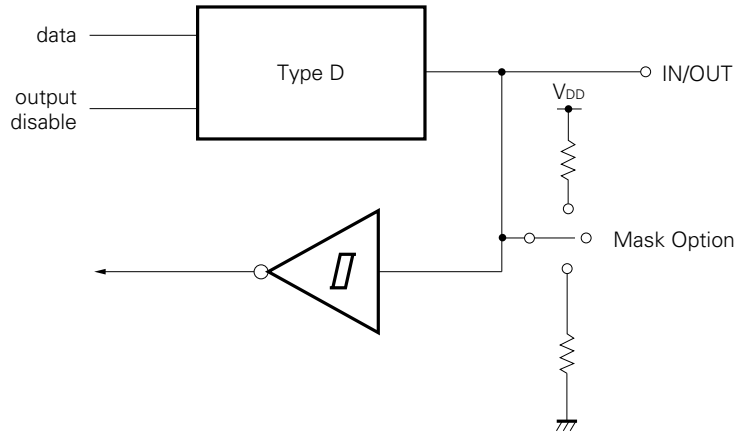

(7) Type S




(8) Type W



(9) Type X




## 1.6 RECOMMENDED CONNECTION OF UNUSED μPD7554A PINS

| Pin | Recommended Connection |
|---|---|
| P00/INT0 | Connect to $V_{SS}$. |
| P01 to P03 | Connect to $V_{SS}$ or $V_{DD}$. |
| P80 to P82 | Leave open. |
| P100 to P103 | Input state : Connect to $V_{SS}$ or $V_{DD}$. Output state: Leave open. |
| P110 to P113 | |

### 1.7 OPERATION OF INPUT/OUTPUT PORTS

**(1) P00 to P03 (Port 0)**

The port 0 is a 4-bit input port consisting of 4-bit input pins P00 to P03. In addition to being used for port input, P00 serves as a count clock input or testable input (INT0), each of P01 to P03 serves as a serial interface input/output.

To use P00 as a count clock input, set bits 2 (CM2) and 1 (CM1) of the clock mode register to 01. (See **2.10 "CLOCK CONTROL CIRCUIT"** for details.)

To use P00 as a INT0, set bit 3 (SM3) of the shift mode register to 1.

The serial interface function to use P01 to P03 as a serial interface I/O port is determined by bits 2 and 1 (SM2 and SM1) of the shift mode register. See **2.12 "SERIAL INTERFACE"** for details.

Even though this port operates using any function other than the port function, execution of the port input instruction (IPL) permits loading data on the P00 to P03 line to the accumulator (A0 to A3) at any time.

**(2) P80 to P83 (Port 8)**

The port 8 is a 4-bit output port with an output latch, which consists of 4-bit output pin.

The port output instruction (OPL) latches the content of the accumulator (A0 to A3) to the output latch and outputs it to pins P80 to P83.

The SPBL and RPBL instructions[Note] allow bit-by-bit setting and resetting of pins P80 to P83.

Note that P83 is to be selected using a mask option, to serve as one of the connection pins of the resistor R for RC oscillation (CL2) or as the bit 3 output of the port 8. Thus, the port 8 is a 3-bit output port (P80 to p82) if RC oscillation is performed, and provides a 4-bit output (P80 to P83) only when an external clock is used.

For these ports, mask options for the output format are available to select CMOS (push-pull) output or N-ch open-drain output.

The port specified as a N-ch open-drain output and provides an efficient interface to the circuit operating at a different supply voltage because the output buffer has a dielectric strength of 9 V.

Contents of the output latch become undefined when the RESET signal is input, then the output becomes high impedance.

**Note** RPBL and SPBL are bit-by-bit setting and resetting instructions. During setting and resetting operations, the RPBL and SPBL instructionrs allow outputting with each (4-bit) port which contains the specified bits. (The content of the output latch is output to any pin other than the specified pins.) The content of the output latch must be initialized with the OPL instruction before executing the RPBL and SPBL instructions.

**(3) P100 to P103 (Port 10) and P110-P113 (Port 11): Quasi-bidirectional input/output**

P100 to P103 are 4-bit I/O pins which form the port 10 (4-bit I/O port with an output latch). P110 to P113 are 4-bit I/O pins which form the port 11 (4-bit I/O port with an output latch).

The port output instruction (OPL) latches the content of the accumulator to the output latch and outputs it to the 4-bit pins.

The data written once in the output latch and the output buffer state are retained until the output instruction to operate the port 10 or 11 is executed or the RESET signal is input. Even though an input instruction is executed for the port 10 or 11, the states of both the output latch and output buffer do not change.

The SPBL and RPBL instructions allow bit-by-bit setting and resetting of pins P100 to P103 and P110 to P113.

The input/output format of each of the ports 10 and 11 can be selected from among the N-ch open-drain input/output, N-ch open-drain + pull-up resistor built-in input/output, and CMOS (push-pull) input/output by their respective mask options.

The ports 10 and 11 offers the middle withstand voltage of 9 V for the N-ch open-drain input/output, so that they are convenient for interface between circuits which has different supply voltages.

When the CMOS (push-pull) input/output is selected, the port cannot return to the input mode once the output instruction is executed. However, the states of the pins of the port can be checked by reading via the port input instruction (IPL).

When one of the other two formats is selected, the port can enter the input mode to load the data on the 4-bit line to the accumulator (as a quasi-bidirectional port) when the port receives high level output. Select each type of the input/output format to meet the use of the port:

① **CMOS input/output**
   i) Uses all 4 bits of the port as input ports.
   ii) Uses pins of the port as output pins not requiring middle withstand voltage output.

② **N-ch open-drain input/output**
   i) Uses pins of the port as I/O pins requiring a middle withstand voltage dielectric strength.
   ii) Uses input pins of the port which also has output pins.
   iii) Uses each pin of the port for both input and output by switching them over.

③ **N-ch open-drain + pull-up resistor built-in input/output**
   i) Uses input pins of the port which also has output pins, that require a pull-up resistor.
   ii) Uses each pin of the port for both input and output by switching them over. This requires a pull-up resistor.

**Caution Before using input pins in the case of ② or ③ , write 1 in the output latch to turn the N-ch transistor off.**

The content of the output latch becomes undefined when the RESET signal is input. In such a case, the output becomes high level with the N-ch open-drain + pull-up resistor built-in, and becomes high impedance without the resistor.

## 2. INTERNAL BLOCK FUNCTIONS

### 2.1 PROGRAM COUNTER (PC): 10 BITS

The program counter is a 10-bit binaryc ounter to retain program memory (ROM) address information.

**Fig. 2-1 Program Counter Configuration**

| PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 | PC |
|---|---|---|---|---|---|---|---|---|---|---|

When one instruction is executed, usually the program counter is incremented by the number of bytes of the instruction.

When the call instruction is executed, the PC is loaded with a nkew call address after the stack memory saves the current contents (return address) of the PC. When the return instruction is executed, the content (return address) of the stack memory is loaded onto the PC. When the jump instruction is executed, the immediate data identifying the destination of the jump is loaded to all or some of bits of the PC.

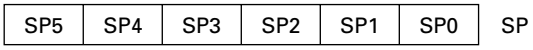
When a skip occurs, the PC is incremented by 2 or 3 during the machine cycle depending on the number of bytes in the next instruction.

When the RESET signal is input, all the bits of the PC are cleared to zero.

### 2.2 STACK POINTER (SP): 6 BITS

The stack pointer is a 6-bit register which retains head address information of the stack memory (LIFO type) which is a part of the data memory.

**Fig. 2-2 Stack Pointer Configuration**

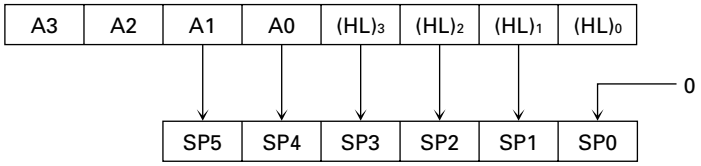



The stack pointer is decremented when the call instruction is executed. It is incremented when the return instruction is executed.

To determine the stack area, initialize the SP using the TAMSP instruction. Note that bit SP0 is loaded with 0 unconditionally when the TAMSP instruction is executed. Set the SP to the value of "the highest address of the stack area + 1" because the stack operation starts with decrementation of the SP.

**When the highest address of the stack area is 3FH which is the highest address of the data memory, the initial value of SP5-0 must be 00H. For emulation using the μPD7500H (EVAKIT-7500B), set the data to be used for AM when executing the TAMSP instruction.**

**Fig. 2-3 In Execution of TAMSP Instruction**




Note that the contents of the SP cannot be read.

**Caution Be sure to set the SP at the initial stage of the program execution because the SP becomes undefined when the RESET signal is input.**

```
Example  LHLI    00H
         LAI     0
         ST
         LAI     4
         TAMSP           ;SP = 40H
```

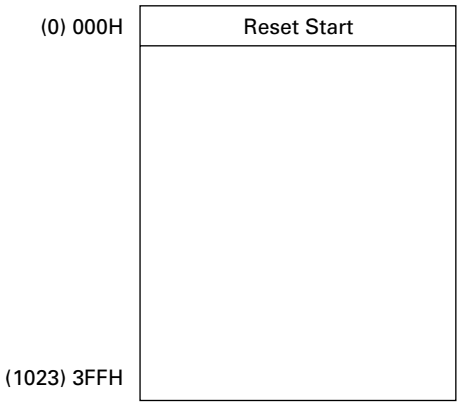
### 2.3 PROGRAM MEMORY (ROM): 1024 WORDS × 8BITS

The program memory is a mask programmable ROM of 1024 word × 8 bits configuration. It is addressed by the program counter.

The program memory stores programs.

Address 000H is the reset start address.

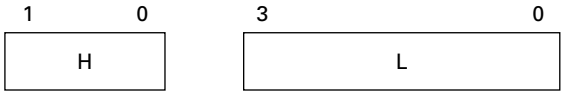
**Fig. 2-4 Program Memory Map**




### 2.4 GENERAL REGISTER

General registers H (with two bits) and L (with four bits) operate individually. They also form a pair register HL (H: high order and L: low order) to serve as a data pointer for addressing the data memory.

**Fig. 2-5 General Register Configuration**

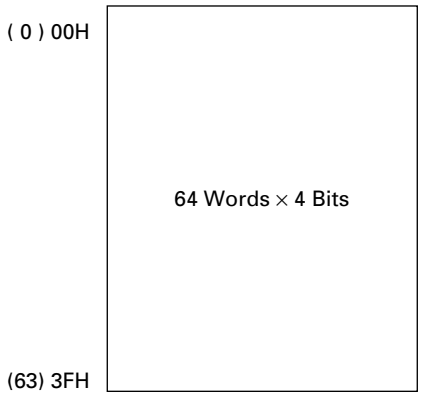



The L register is also used to specify I/O ports and the mode register when an input/output instruction (IPL or OPL) is executed. It also used to specify the bits of a port when the SPBL or RPBL instruction is executed.

### 2.5 DATA MEMORY (RAM): 64 × 4 BITS

The data memory is a static RAM of 64 word × 4 bits configuration. It is used as the area to store or stack processed data. The data memory may be processed in 8-bit units when paired with the accumulator.

**Fig. 2-6 Data Memory Map**




The data memory is addressed in the following three ways:

- Direct: Direct addressing based on immediate data of an instruction
- Register indirect: Indirect addressing according to the contents of the pair register HL (including automatic incrementation and decrementation)
- Stack: Indirect addressing according to the contents of the stack pointer (SP)

An arbitrary space of the data memory is available as stack memory. The boundary of the stack area is specified when the TAMSP instruction initializes the SP. After that, the stack area is accessed automatically by the call or return instruction.

After the call instruction is executed, the content of the PC and PSW is stored in the order shown in the following diagram:

Stack Area

| | 3 | | | 0 |
|---|---|---|---|---|
| SP – 4 | 0 | 0 | PC9 | PC8 |
| SP – 3 | PSW[Note] | | | |
| SP – 2 | PC3 – PC0 | | | |
| SP – 1 | PC7 – PC4 | | | |
| | | | | |

**Note** Bit 1 is fixed at 0.

When the return instruction is executed, the content of the PSW is not restored while those of the PC are restored. Data in the data memory is retained at a low supply voltage in the STOP mode.

### 2.6 ACCUMULATOR (A): 4 BITS

The accumulator is a 4-bit register which plays a major role in many types of arithmetic operations. The accumulator may be processed in 8-bit units when paired with the data memory addressed by the pair register HL.

**Fig. 2-7 Accumulator Configuration**

| A3 | A2 | A1 | A0 | A |
|---|---|---|---|---|

### 2.7 ARITHMETIC LOGIC UNIT (ALU): 4 BITS

The arithmetic logic unit is a 4-bit arithmetic circuit to perform arithmetic and bit processing such as binary addition, logical operation, incrementation, decrementation, and comparison.

### 2.8 PROGRAM STATUS WORD (PSW): 4 BITS

The program status word consists of skip flags (SK1 and SK0) and a carry flag (C). Bit 1 of the PSW is fixed at 0.

**Fig. 2-8 Program Status Word Configuration**

| 3 | 2 | 1 | 0 | |
|---|---|---|---|---|
| SK1 | SK0 | 0 | C | PSW |

**(1) Skip flags (SK1 and SK0)**

Skip flags store the following skip status:

- Stacking by the LAI instruction
- Stacking by the LHLI instruction
- Skip condition establishment by any instruction other than stack instructions

The skip flags are set and reset automatically when respective instructions are executed.

**(2) Carry flag (C)**

The carry flag is set to 1 when a carry from bit 3 of the ALU occurs when the add instruction (ACSC) is executed. The flag is reset to 0 when the carry does not occur. The SC and RC instructions respectively set and reset the carry flag. The SKC instruction tests the contents of the flag.

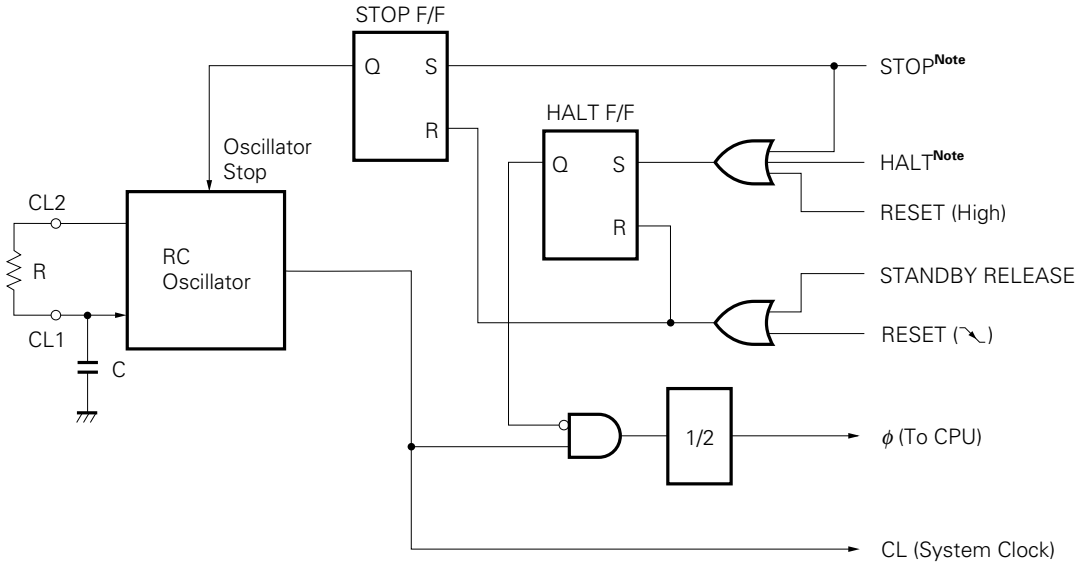
The content of the PSW are automatically stored in the stack area when the call instruction is executed. It cannot be restored by the return inhstruction.

When the RESET signal is input, SK1 and SK0 are both cleared to zero and C becomes undefined.

## 2.9 SYSTEM CLOCK GENERATOR

The system clock generator contains an RC oscillator, 1/2 divider, and standby (STOP/HALT) mode control circuit.

**Fig. 2-9 System Clock Generator**




**Note** Instruction execution

The RC oscillator oscillates with an external resistor R connected to pins CL1 and CL2. (A capacitor C is incorporated.)

The RC oscillator serves merely as a reverse buffer if inputs an external clock through the CL1 input.

The RC oscillator outputs the system clock (CL) which is 1/2 divided to the CPU clock ($\phi$).

The control circuit in the standby mode consists mainly of STOP F/F and HALT F/F.

The STOP F/F is set by the STOP instruction, blocking any clock from being supplied. The STOP F/F stops RC oscillation during operation of the RC oscillator (STOP mode).

The STOP F/F is reset by the STANDBY RELEASE signal (which goes active when even one test request flag is input) or at the fall of the RESET input, to cause the RC oscillator to start oscillation and supplying each clock.

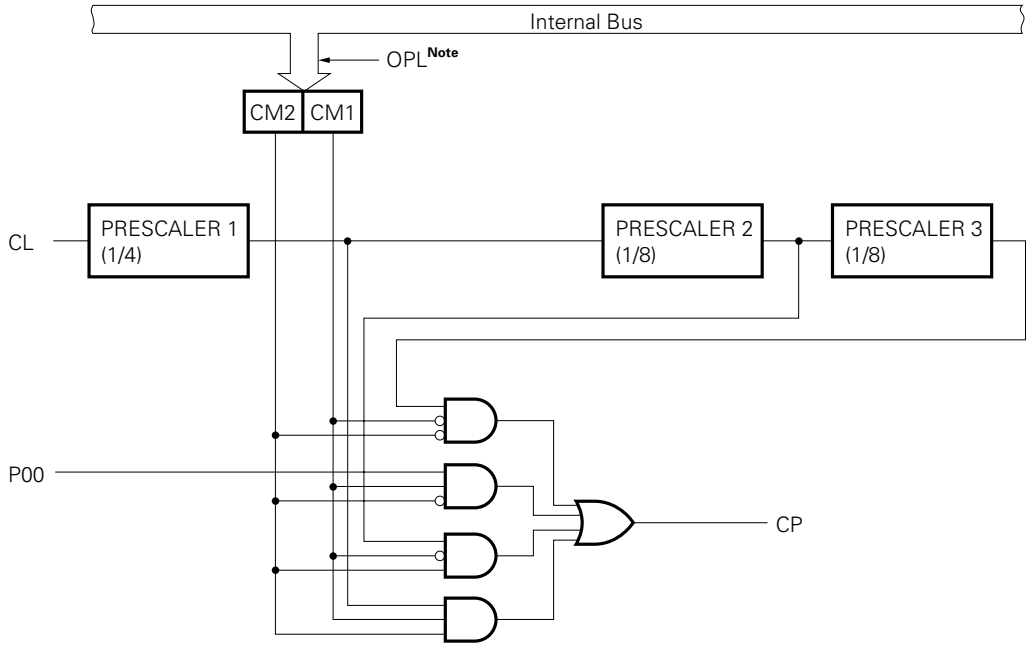
The HALT F/F is set by the HALT instruction to disable the input to the 1/2 divider which generates the CPU clock $\phi$, stopping only the CPU clock $\phi$ (HALT mode).

The HALT F/F is set and reset as in the case of the STOP F/F. Resetting the HALT F/F cause the RC oscillator to start supplying the CPU clock $\phi$.

### 2.10 CLOCK CONTROL CIRCUIT

The clock control circuit consists of 2-bit clock mode registers (CM2 and CM1), prescalers 1, 2 and 3, and a multiplexer. The circuit inputs the system clock generator output (CL) and the event pulse (P00). It also selects a clock source and a prescaler according to the specifications of clock mode register and supplies a count pulse (CP) to the timer/event counter.

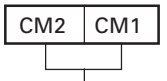
**Fig. 2-10 Clock Control Circuit**




**Note** Instruction execution

Use the OPL instruction to set codes in the clock mode registers.

**Fig. 2-11 Clock Mode Register Format**



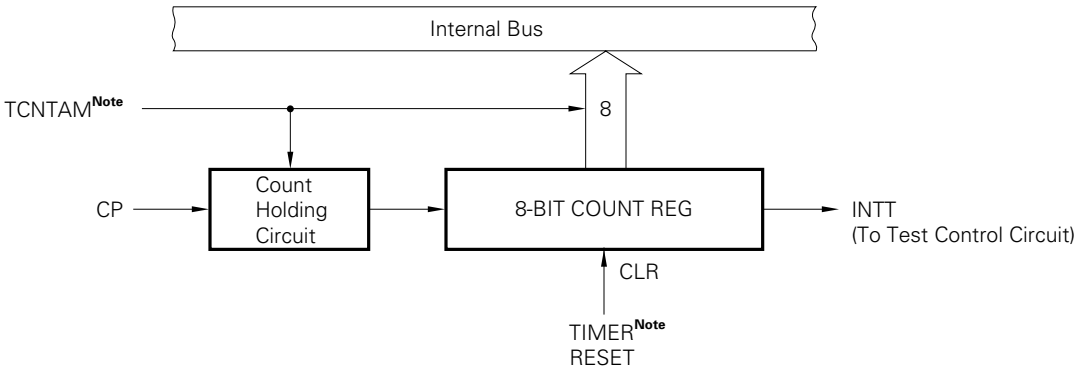

| CM2 | CM1 | Count Pulse Frequency (CP) |
|---|---|---|
| 0 | 0 | CL × $\frac{1}{256}$ |
| 0 | 1 | P00 |
| 1 | 0 | CL × $\frac{1}{32}$ |
| 1 | 1 | CL × $\frac{1}{4}$ |

**Caution When setting codes in the clock mode registers using the OPL instruction, be sure to set bit 0 of the accumulator to 0. (Bit 0 corresponds to CM0 of the μPD7500 of EVAKIT-7500B in emulation.)**

### 2.11 TIMER/EVENT COUNTER

The timer/event counter is based on an 8-bit count register as shown in Fig. 2-12.

**Fig. 2-12 Timer/Event Counter**




**Note** Instruction execution

The 8-bit count register is a binary 8-bit up-counter which is incremented whenever a count pulse (CP) is input. The register is cleared to 00H when the TIMER instruction is executed, RESET signal is input, or an overflow occurs (FFH to 00H).

As the count pulse, the clock mode register can select one of the following four. See **2.10 "CLOCK CONTROL CIRCUIT"**.

$$CP : CL \times \frac{1}{4},\ CL \times \frac{1}{32},\ CL \times \frac{1}{256},\ P00$$

The count register continues to be incremented as long as count pulses are input. The TIMER instruction clears the count register to 00H and triggers the timer operation.

The count register is incremented in synchronization with the CP (or the rise of the P00 input when an external clock is used). On the count reaches 256, the register returns the count value to 00H from FFH, generates the overflow signal INTT, and sets the INTT test flag INTT RQF.

In this way, the count register counts over from 00H.

To recognize the overflow, test the flag INTT RQF using the SKI instruction.

When the timer/event counter serves as a timer, the reference tiome is determined by the CP frequency. The precision is determined by the RC oscillation or CL1 external input frequency when the system clock system is selected and by the P00 input frequency when the P00 input is selected.

The content of the count register can be read at any time by the TCNTAM instruction. This function allows checking the current time of the timer and counting event pulses input to the P00 input. This enables the number of even pulses that have been generated so far (event counter function).

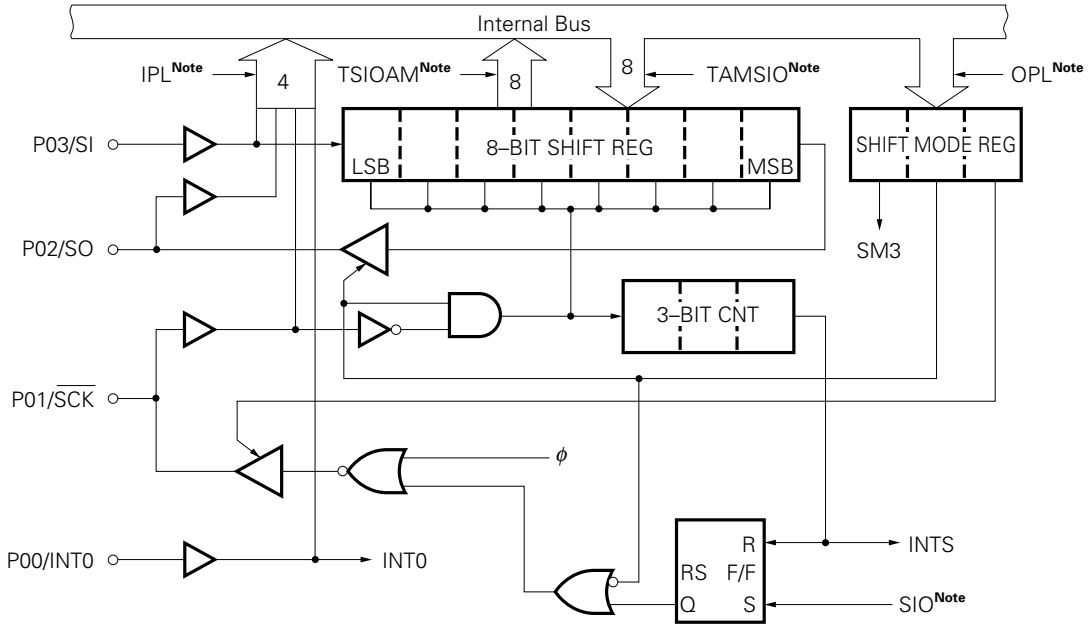
The count holding circuit ignores the change of the count pulse (CP) during execution of the TCNTAM instruction. This is to prevent reading undefined data in the count register using the TCNTAM instruction while the counter is being updated.

Since the timer/event counter operates the system clock system (CL) or the P00 input for count pulses, it is used to cancel the HALT mode which stops the CPU clock $\phi$ as well as the STOP mode which stops the system clock CL. (See **3 "STANDBY FUNCTIONS"**.)

## 2.12 SERIAL INTERFACE

The serial interface consists of an 8-bit shift register, 3-bit shift mode register, and 3-bit counter. It is used for input/output of serial data.

**Fig. 2-13 Serial Interface Block Diagram**



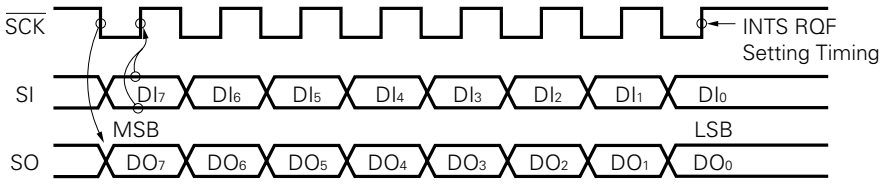

**Note** Instruction execution

**Remarks** **1.** $\phi$ indicates the internal clock signal (system clock).
**2.** SM3 and INT0 go to the test control circuit.

Input/output of serial data is controlled by the serial clock. The highest bit (bit 7) of the shift register is output from the SO line at rise of the serial clock ($\overline{SCK}$ pin signal). At its fall, the contents of the shift register is shifted by one bit (bit n -> bit n+1) and data on the SI line is loaded to the lowest bit (bit 0) of the shift register.

The 3-bit counter (octal counter) counts serial clock pulses. Wthenever it counts eight clock pulses (on completion of 1-byte serial data transfer), the counter generates an internal test request signal INTS to set the test request flag (INT0/S RQF).

**Fig. 2-14 Shift Timing**




**Remarks** **1.** DI: Serial data input
**2.** DO: Serial data output

The serial interface sets serial data for transmission in the shift register using the TAMSIO instruction and starts the transfer using the SIO instruction. To recognize the termination of one-byte transfer, check the test request flag INT0/S RQF using the corresponding instruction.

The serial interface starts serial data reception, using the SIO instruction, checks the termination of one-byte transfer using the instruction, and then receives data from the shift register by executing the TSIOAM instruction.

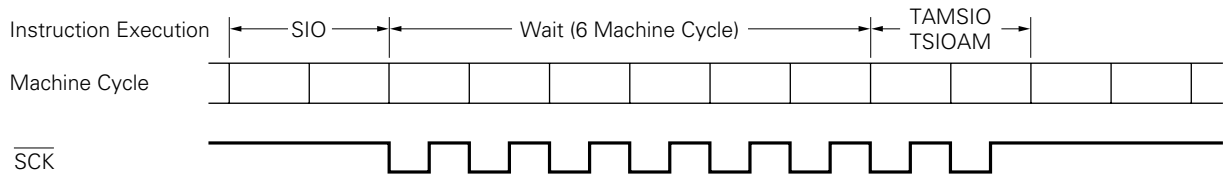
Two types of serial clock sources are available: one is the system clock $\phi$ and the other is the external clock ($\overline{SCK}$ input). They are selected respectively by bits 2 and 1 (SM2 and SM1) of the shift mode register.

When the system clock $\phi$ is selected and the SIO instruction is executed, the clock pulse is supplied to the serial interface as a serial clock to control serial data input/output and is output from the $\overline{SCK}$ pin.

When the system clock $\phi$ pulse is supplied eight times, the supply to the serial interface is automatically stopped and the $\overline{SCK}$ output remains high. Since serial data input/output stops automatically after transfer of one byte. The programmer does not need to control the serial clock. In this case, the transfer speed is determined by the system clock frequency.

In this mode, it is possible to read receive data (by the TSIOAM instruction) and write data (by the TAMSIO instruction) from and to the shift register only by waiting for 6 machine cycles after execution of the SIO instrucction on the program without waiting until the INT0/S RQF is set.

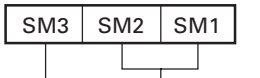
**Fig. 2-15 TAMSIO/TSIOAM Instruction Execution Timing**




When the external clock ($\overline{SCK}$ input) is selected, the interface inputs serial clock pulses from the $\overline{SCK}$ input. When an external serial clock pulse is input eight times, the INT0/S RQF is set and the termination of one-byte transfer can be recognized. However, the eight serial clocks to be input must be counted on the side of the external clock source because serial clock disable control is not performed internally. The transfer speed is determined by the external serial clock within the range from DC to the maximum value limited by the standard.

When the external clock is used, the SIO, TAMSIO, or TSIOAM instruction the execution must be executed while the serial clock pulse $\overline{SCK}$ is high. If such an instruction is executed while the $\overline{SCK}$ is rising or falling or is low, the function of the instruction is not guaranteed.

**Fig. 2-16 Shift Mode Register Format**




Shift Mode Register

Settings for serial interface operation and the associated mode of the port 0

| SM2 | SM1 | P03/SI | P02/SO | P01/$\overline{SCK}$ | Serial Operation |
|---|---|---|---|---|---|
| 0 | 0 | Port input | Port input | Port input | Stop |
| 0 | 1 | | | $\phi$ continuous output | |
| 1 | 0 | SI input | SO output | $\overline{SCK}$ input | Operation based on external clock |
| 1 | 1 | | | $\overline{SCK}$ output ($\phi \times 8$) | Operation based on $\phi$ |

INT0/INTS selection

| SM3 | Test Sources |
|---|---|
| 0 | INTS |
| 1 | INT0 |

**Caution When setting a code in the shift mode register using the OPL instruction, be sure to set bit 0 of the accumulator to 0 (Bit 0 corresponds to CM0 of the μPD7500H of EVAKIT-7500B in emulation).**

In the system which does not require serial interface, the 8-bit shift register can be used as a simple register and data can be read or writtene by the TSIOAM or TAMSIO instruction when serial operation is off.

### 2.13 TEST CONTROL CIRCUIT

The μPD7554A is provided with the following three types of test sources (one external source and two internal sources):

| Test Sources | Internal/External | Request Flag |
|---|---|---|
| INTT (Overflow from timer/event counter) | Internal | INTT RQF |
| INT0 (Test request signal from P00 pin) | External | INT 0/S RQF |
| INTS (Transfer end signal from serial interface) | Internal | |

The test control circuit checks consist mainly of test request flags (INTT RQF and INT0/S RQF) which are set by three different test sources and the test request flag control circuit which checks the content of test request flags using the SKI instruction and controls resetting the checked flags.

The INT0 and INTS are common in the request flag. Which one is selected is determined by bit 3 (SM3) of the shift mode register.

| SM3 | Test Sources |
|---|---|
| 0 | INTS |
| 1 | INT0 |

The INTT RQF is set when a timer overflow occurs and is reset by the SKI or TIMER instruction.

The INT0/S request flag functions in the following two ways according to the setting of the SM3:

**(1) SM3 = 0**

The INTS is validated. The request flag INT0/S RQF is set when the INTS signal to indicate the termination of 8-bit serial data transfer is issued. The flag is reset when the SKI or SIO instruction is executed.

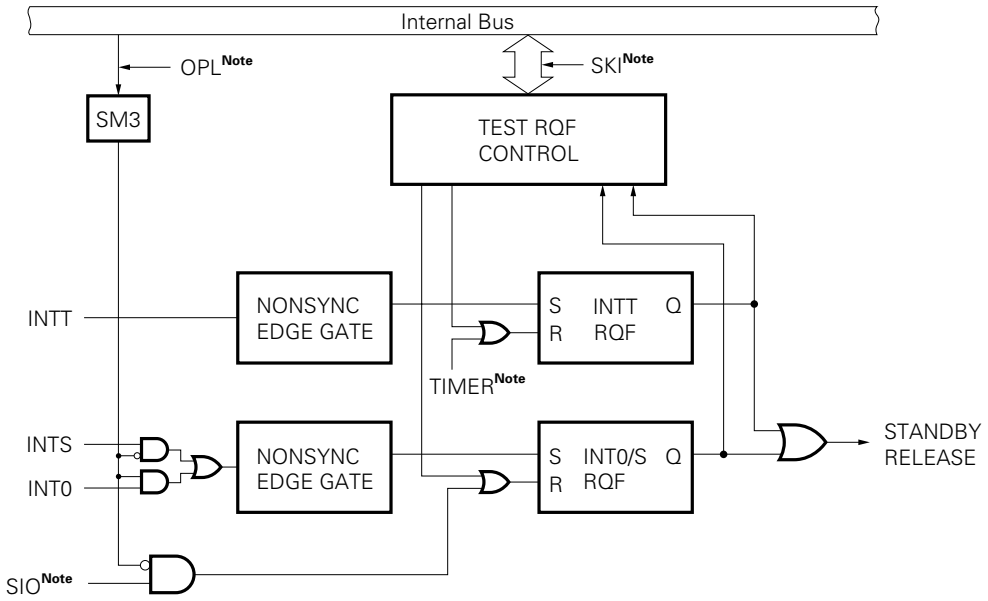
**(2) SM3 = 1**

The IN0 is validated. The request flag INT0/S RQF is set when the leading edge signal enters the INT0/P00 pin. The flag is reset when the SKI instruction is executed.

The OR output of each test request flag is used to cancel the standby mode (STOP/HALT mode). If one or more request flags are set in the standby mode, the standby mode is cancelled.

The RESET signal cancels every request flag and the SM3. In the reset initial status, the INTS is selected and the INT0 input is disabled.

**Fig. 2-17 Test Control Circuit Block Diagram**




**Note** Instruction execution

**Remark** SM3 is bit 3 of the shift mode register.

## 3. STANDBY FUNCTIONS

The μPD7554A provides two types of standby modes (STOP and HALT modes) to save power while the program is on standby. The STOP and HALT modes are set by the STOP and HALT instructions, respectively. The standby mode halts program execution, however, it holds the contents of all the internal registers and data memory that have been stored.

The timer can operate even in the standby mode.

The standby mode is canceled when the test request flag (INTT RQF or INT0/S RQF) is set or by RESET input.

Note that if even one test request flag is set, the device cannot enter either the STOP or HALT mode even though the STOP or HALT instruction is executed. Before setting the standby mode at a point where a test request flag may be set, execute the SKI instruction to reset the test request flag.

Table 3-1 relates the STOP mode to the HALT mode. An essential difference between them is found when RC oscillation supplies the system clock: by stopping the oscillation, the CL output stops in the STOP mode and does not stop in the HALT mode. Thus the amount of the power consumption of the RC oscillator equals to the difference in the amounts of the basic power consumption between the STOP mode and HALT mode.

Note that the STOP mode enables the low supply voltage data to be retained in the data memory.

**Table 3-1 The Relation Between STOP and HALT Modes**

| | Setting Instruction | RC Oscillation (CL) | $\phi$ | P00 | CPU | Timer | Cancellation Factor |
|---|---|---|---|---|---|---|---|
| STOP mode | STOP | × | × | ○ | × | △ | INTT RQF<br>INT0/S RQF<br>RESET input |
| HALT mode | HALT | ○ | | | | ○ | |

○ : Operation enabled
△ : Operation enabled depending on mode selection
× : Stop

### 3.1 STOP MODE

The STOP mode stops the RC oscillation and 1/2 divider in the system clock generator. Therefore, the operations of requiring the system clock stubsystem (CL and $\phi$) such as the CPU are stopped. Since the STOP mode allows operation of the clock control circuit, the timer can operate if the P00 input is selected as the count pulse (CP).

Note that the STOP mode stops only the $\phi$ signal, allowing the CL output when system clock generation is not drived by the RC oscillation, but drived by the external CL1 input. In such a case, the STOP mode causes the same state as in the case of the HALT mode described below. Therefore, the STOP instruction is effective for setting the STOP mode only during RC oscillation.

### 3.2 HALT MODE

The HALT mode stops only the 1/2 divider in the system clock generator (allowing operation of the system clock CL and stopping the CPU clock $\phi$). Therefore, the operations of the CPU requiring the $\phi$ signal is stopped in the HALT mode. Since the HALT mode allows operation of the clock control circuit, the circuit inputs the CL signal from the clock generator and the external count clock (P00) to supply the count pulses (CP) for both subsystems selectively to the timer. Thus, the timer can operate depending on the both-system count pulses and continue counting time.

### 3.3 CANCELLING THE STANDBY MODE

**(1) Cancelling the STANDBY mode by test request flag**

As well as the STOP mode and HALT mode, the STANDBY mode is canceled when the test request flag (INTT RQF or INT0/S RQF) is set in the mode. The program starts executing the instruction that follows the HALT instruction that follows the STOP or HALT instruction.

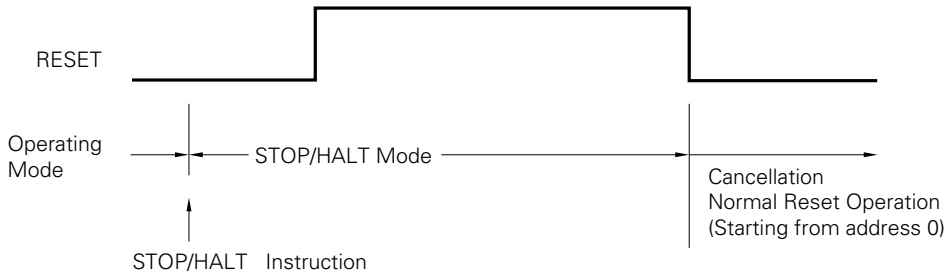
Cancellation of the HALT mode does not affect the content of any register or the data memory, that is retained in the mode.

**(2) Cancelling the STANDBY mode by RESET input**

RESET input unconditionally cancels the STANDBY mode as well as nthe STOP mode and HALT mode.

Fig. 3-1 shows the STANDBY mode cancel timing.

**Fig. 3-1 STANDBY Mode Cancel Timing by RESET Input**




The STANDBY mode is maintained while the RESET input is being active (high). When the RESET input goes low, the STANDBY mode is cancelled and the CPU starts to execute the program from address 0 after a normal reset operation.

Note that RESET input does not affect the content of the data memory that is retained in the STANDBY mode, however, the contents of the other registers become undefined on cancellation of the mode.

## 4. RESET FUNCTIONS

The μPD7554A is reset and initialized when the RESET pin inputs a high or active RESET signal as follows:

### 4.1 DETAILS OF INITIALIZATION

(1) The program counter (PC9-PC0) is cleared to zero.
(2) The skip flags (SK1 and SK0) in the program status word are reset to zero.
(3) The count register in the timer-event counter is cleared to 00H.
(4) The clock control circuit becomes as follows:
• Clock mode registers (CM2 and CM1) = 0

$$\rightarrow CP = CL \times \frac{1}{256}$$

• Prescalers 1, 2, and 3 = 0
(5) The shift mode register (SM3 to SM1) is cleared to zero.
→ Shifting of the serial interface is stopped.
→ The port 0 enters the input mode (high impedance). Note1
→ INT0/S, INTS is selected.
(6) The test request flag (INTT RQF or INT0/S RQF) is reset to zero.
(7) The contents of the data memory and the following registers become undefined:
Stack pointer (SP)
Accumulator (A)
Carry flag (C)
General registers (H and L)
Output latch of each port
(8) The output buffer of every port goes off and has high impedance Note2. The I/O port enters the input mode.

**Note 1.** When the pull-up and pull-down resistors are selected using a mask option, the former has high level and the latter has low level.
**2.** When the pull-up and pull-down resistors are selected in the port 0 using a mask option, the former has high level and the latter has low level.
When the pull-up resistor is selected in the ports 10 and 11 using a mask option, the resistor has high level.

**Caution When the STANDBY mode is cancelled by the RESET signal, the content of the data memory is retained without becoming undefined.**

When the RESET input is cancelled, the program is executed starting with address 000H. The content of each register shall either be initialized in the process of the program or reinitialized depending on conditions.

## 5. μPD7554A INSTRUCTION SET

### (1) Operand representation and description

| | |
|---|---|
| addr | 10-bit immediate data or label |
| caddr<br>caddr1 | 10-bit immediate data or label<br>100H to 107H, 140H to 147H, 180H to 187H,<br>IC0H to IC7H immediate data or label |
| mem | 6-bit immediate data or label |
| n5<br>n4<br>n2 | 5-bit immediate data or label<br>4-bit immediate data or label<br>2-bit immediate data or label |
| bit | 2-bit immediate data or label |
| pr | HL-, HL+, HL |

### (2) Mnemonics for operation descriptions

A : Accumulator
H : H register
L : L register
HL : Pair register HL
pr : Pair register HL-, HL+, or HL
SP : Stack pointer
PC : Program counter
C : Carry flag
PSW : Program status word
SIO : Shift register
CT : Count register
In : Immediate data to n5, n4 or n2
Pn : Immediate data to addr, caddr, or caddr1
Bn : Immediate data to bit
Dn : Immediate data to mem
Rn : Immediate data to pr
(××) : Content addressed by ××
×H : Hexadecimal data

### (3) Port/mode register selection

**IPL Instruction**

| L | Port |
|---|---|
| 0 | Port 0 |
| AH | Port 10 |
| BH | Port 11 |

**OPL Instruction**

| L | Port/mode register |
|---|---|
| 8 | Port 8 |
| AH | Port 10 |
| BH | Port 11 |
| CH | Clock mode register |
| FH | Shift mode register |

**RPBL/SPBL Instruction**

| L | FH | EH | DH | CH | BH | AH | 9 | 8 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 |
| Port | Port 11 | | | | Port 10 | | | | Port 8 | | | |

### (4) Selection of pair register addressing

| pr | $R_1$ | $R_0$ |
|---|---|---|
| HL– | 0 | 0 |
| HL+ | 0 | 1 |
| HL | 1 | 0 |

| Note | Mnemonic | Operands | Operation Code B1 | Operation Code B2 | Operation | | Skip Condition |
|---|---|---|---|---|---|---|---|
| Load/Store Instructions | LAI | n4 | 0 0 0 1 $I_3$ $I_2$ $I_1$ $I_0$ | | A←n4 | Loads n4 to the accumulator. | Stack LAI |
| | LHI | n2 | 0 0 1 0 1 0 $I_1$ $I_0$ | | H←n2 | Loads n2 to H register. | |
| | LAM | pr | 0 1 0 1 0 0 $R_1$ $R_0$ | | A←(pr) pr = HL –, HL +, HL | Loads the contents of the memory address by pr to the accumulator. | L = FH(HL –)<br>L = 0 (HL +) |
| | LHLI | n5 | 1 1 0 $I_4$ $I_3$ $I_2$ $I_1$ $I_0$ | | H←0$I_4$, L←$I_{3-0}$ | Loads n5 to the pair register HL. | Stack LHLI |
| | ST | | 0 1 0 1 0 1 1 1 | | (HL)←A | Stores the contents of the accumulator in the memory addressed by HL. | |
| | STII | n4 | 0 1 0 0 $I_3$ $I_2$ $I_1$ $I_0$ | | (HL)←n4, L←L+1 | Stores n4 in the memory addressed by HL and increments the L register. | |
| | XAL | | 0 1 1 1 1 0 1 1 | | A↔L | Exchanges the contents of the accumulator and the L register. | |
| | XAM | pr | 0 1 0 1 0 1 $R_1$ $R_0$ | | A↔(pr) pr = HL – , HL + , HL | Exchanges the contents of the accumulator and the memory addressed by pr. | L = FH(HL–)<br>L = 0 (HL+) |
| Operation Instructions | AISC | n4 | 0 0 0 0 $I_3$ $I_2$ $I_1$ $I_0$ | | A←A + n4 | Adds the accumulator to n4. | Carry |
| | ASC | | 0 1 1 1 1 1 0 1 | | A←A + (HL) | Adds the contents of the accumulator and the memory addressed by HL. | Carry |
| | ACSC | | 0 1 1 1 1 1 0 0 | | A, C←A + (HL) + C | Adds the contents of the accumulator, the memory addressed by HL, and of the carry flag. | Carry |
| | EXL | | 0 1 1 1 1 1 1 0 | | A←A ∀ (HL) | Calculate the exclusive OR of the contents of the accumulator and the memory addressed by HL. | |
| Accumulator & Carry Flag Manipulation Instructions | CMA | | 0 1 1 1 1 1 1 1 | | A←$\overline{A}$ | Complements the accumulator. | |
| | RC | | 0 1 1 1 1 0 0 0 | | C←0 | Resets the carry flag. | |
| | SC | | 0 1 1 1 1 0 0 1 | | C←1 | Sets the carry flag. | |
| Increment/Decrement Instructions | ILS | | 0 1 0 1 1 0 0 1 | | L←L + 1 | Increments the L register. | L = 0 |
| | IDRS | mem | 0 0 1 1 1 1 0 1 | 0 0 $D_5$ $D_4$ $D_3$ $D_2$ $D_1$ $D_0$ | (mem)←(mem) + 1 | Increments the contents of the memory addressed by mem. | (mem) = 0 |
| | DLS | | 0 1 0 1 1 0 0 0 | | L←L – 1 | Decrements the L register. | L = FH |
| | DDRS | mem | 0 0 1 1 1 1 0 0 | 0 0 $D_5$ $D_4$ $D_3$ $D_2$ $D_1$ $D_0$ | (mem)←(mem) – 1 | Decrements the contents of the memory addressed by mem. | (mem) = FH |
| Memory Bit Manipulation Instructions | RMB | bit | 0 1 1 0 1 0 $B_1$ $B_0$ | | $(HL)_{bit}$←0 | Resets the bits specified by $B_{1-0}$, of the memory addressed by HL. | |
| | SMB | bit | 0 1 1 0 1 1 $B_1$ $B_0$ | | $(HL)_{bit}$←1 | Sets the bits specified by $B_{1-0}$, of the memory addressed by HL. | |

**Note** Instruction Group

| Note | Mnemonic | Operands | Operation Code B1 | | | | | | | | Operation Code B2 | | | | | | | | Operation | | Skip Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Jump Instructions | JMP | addr | 0 | 0 | 1 | 0 | 0 | 0 | $P_9$ | $P_8$ | $P_7$ | $P_6$ | $P_5$ | $P_4$ | $P_3$ | $P_2$ | $P_1$ | $P_0$ | $PC_{9-0} \leftarrow P_{9-0}$ | Jumps to the address specified by $P_{9-0}$. | |
| | JCP | addr | 1 | 0 | $P_5$ | $P_4$ | $P_3$ | $P_2$ | $P_1$ | $P_0$ | | | | | | | | | $PC_{5-0} \leftarrow P_{5-0}$ | Jumps to the address specified by replacing $PC_{5-0}$ with $P_{5-0}$. | |
| Subroutine/stack control instructions | CALL | caddr | 0 | 0 | 1 | 1 | 0 | 0 | $P_9$ | $P_8$ | $P_7$ | $P_6$ | $P_5$ | $P_4$ | $P_3$ | $P_2$ | $P_1$ | $P_0$ | $(SP-1)(SP-2)(SP-4) \leftarrow PC_{9-0}$<br>$(SP-3) \leftarrow PSW$, $SP \leftarrow SP-4$<br>$PC_{9-0} \leftarrow P_{9-0}$ | Saves the contents of PC and PSW to the stacxk memory, decrements SP by 4, and calls the address specified by caddr. | |
| | CAL | caddr1 | 1 | 1 | 1 | $P_4$ | $P_3$ | $P_2$ | $P_1$ | $P_0$ | | | | | | | | | $(SP-1)(SP-2)(SP-4) \leftarrow PC_{9-0}$<br>$(SP-3) \leftarrow PSW$, $SP \leftarrow SP-4$<br>$PC_{9-0} \leftarrow 0\ 1\ P_4\ P_3\ 0\ 0\ 0\ P_2\ P_1\ P_0$ | Saves the contents of PC and PSW to the stacxk memory, decrements SP by 4, and calls the address specified by caddr1. | |
| | RT | | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | | | | | | | | | $PC_{9-0} \leftarrow (SP)(SP+2)(SP+3)$<br>$SP \leftarrow SP+4$ | Restores the contents of the stack memory to PC, and increments SP by 4. | |
| | RTS | | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | | | | | | | | | $PC_{9-0} \leftarrow (SP)(SP+2)(SP+3)$<br>$SP \leftarrow SP+4$<br>then skip unconditionally | Restores the contents of the stack memory to PC, increments SP by 4, and causes unconditional skipping. | Unconditionally |
| | TAMSP | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | $PC_{5-4} \leftarrow A_{1-0}$<br>$SP_{3-1} \leftarrow (HL)_{3-1}$, $SP_0 \leftarrow 0$ | Transfers the two low-order bits of the accumulator to $SP_{5-4}$ and the three high-order bits of the memory addressed by HL to $SP_{3-1}$. | |
| Skip Instructions | SKC | | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | | | | | | | | | Skip if C = 1 | Causes skipping if the carry flag is 1. | C = 1 |
| | SKABT | bit | 0 | 1 | 1 | 1 | 0 | 1 | $B_1$ | $B_0$ | | | | | | | | | Skip if $A_{bit} = 1$ | Causes skipping of the bit of the accumulator, which is specified by $B_{1-0}$ is 1. | $A_{bit} = 1$ |
| | SKMBT | bit | 0 | 1 | 1 | 0 | 0 | 1 | $B_1$ | $B_0$ | | | | | | | | | Skip if $(HL)_{bit} = 1$ | Causes skipping of the bit of the memory addressed by HL, which is specified by $B_{1-0}$ is 1. | $(HL)_{bit} = 1$ |
| | SKMBF | bit | 0 | 1 | 1 | 0 | 0 | 0 | $B_1$ | $B_0$ | | | | | | | | | Skip if $(HL)_{bit} = 0$ | Causes skipping of the bit of the memory addressed by HL, which is specified by $B_{1-0}$ is 0. | $(HL)_{bit} = 0$ |
| | SKAEM | | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | | | | | | | | | Skip if A = (HL) | Causes skipping if the contents are the same between the accumulator and the memory addressed by HL. | A = (HL) |
| | SKAEI | n4 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | $I_3$ | $I_2$ | $I_1$ | $I_0$ | Skip if A = n4 | Skips if the accumulator is equal to n4. | A = n4 |
| | SKI | n2 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | $I_1$ | $I_0$ | Skip if INT RQF = 1<br>Then reset INT RQF | Skips if INT RQF is 1, and then sets INT RQF to 0. | INT RQF = 1 |

**Note** Instruction Group

| Note1 | Mnemonic | Operands | Operation Code B1 | | | | | | | | Operation Code B2 | | | | | | | | Operation | | Skip Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SIO control instructions | TAMSIO | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | $SIO_{7-4} \leftarrow A$<br>$SIO_{3-0} \leftarrow (HL)$ | Transfers the contents of the accumulator to the four high-order bits of the shift register and the contents of the memory addressed by HL to the four low-order bits. | |
| | TSIOAM | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | $A \leftarrow SIO_{7-4}$<br>$(HL) \leftarrow SIO_{3-0}$ | Transfers the four high-order bits of the shift register to the accumulator and the four low-order bits to the memory addressed by HL. | |
| | SIO | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | Start SIO | Starts shifting. | |
| Timer control instructions | TIMER | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | Start Timer | Starts timer operation. | |
| | TCNTAM | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | $A \leftarrow CT_{7-4}$<br>$(HL) \leftarrow CT_{3-0}$ | Transfers the four high-order bits of the count register to the accumulator and the four low-order bits to the memory addressed by HL. | |
| Input/output instructions | IPL | | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | | | | | | | | | A←Port (L) | Loads the contents of the port specified by the L register to the accumulator. | |
| | OPL | | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | | | | | | | | | Port/Mode reg. (L)←A register or the mode register. | Outputs the contents of the accumulator to the port specified by the L | |
| | RPBL Note2 | | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | | | | | | | | | Port bit (L)←0 | Resets the bits of ports 8, 10, and 11, that are specified by the L register. | |
| | SPBL Note2 | | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | | | | | | | | | Port bit (L)←1 | Sets the bits of ports 8, 10, and 11, that are specified by the L register. | |
| CPU control Instructions | HALT | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | Set Halt Mode | Sets the HALT mode. | |
| | STOP | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Set Stop Mode | Sets the STOP mode. | |
| | NOP | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | No operation | Performs no operation for one machine cycle. | |

**Note 1.** Instruction Group

**2.** SPBL and RPBL are bit-wise set/reset instructions. They perform output to each 4-bit port including the specified bits as well as set and reset operation (They output the contents of the output latch to bits other than the specified bits.). Before executing these instructions, intialize the contents of the output latch using the OPL instruction.

## 6. ELECTRICAL SPECIFICATIONS

### μPD7554A: ABSOLUTE MAXIMUM RATINGS ($T_a$ = 25 °C)

| Parameter | Symbol | Test Conditions | | Rating | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | | –0.3 to +7.0 | V |
| Input voltage | $V_I$ | Except ports 10 and 11 | | –0.3 to $V_{DD}$ + 0.3 | V |
| | | Ports 10 and 11 | **Note 1** | –0.3 to $V_{DD}$ + 0.3 | V |
| | | | **Note 2** | –0.3 to +11 | V |
| Output voltage | $V_O$ | Except ports 8, 10, 11 | | –0.3 to $V_{DD}$ + 0.3 | V |
| | | Ports 8, 10 and 11 | **Note 1** | –0.3 to $V_{DD}$ + 0.3 | V |
| | | | **Note 2** | –0.3 to +11 | V |
| Output current high | $I_{OH}$ | 1 pin | | –5 | mA |
| | | All pins in total | | –15 | mA |
| Output current low | $I_{OL}$ | 1 pin | P01, P02 | 5 | mA |
| | | | Port 8 | 30 | mA |
| | | | Others | 15 | mA |
| | | All pins in total | | 100 | mA |
| Operating temperature | $T_{opt}$ | | | –10 to +70 | °C |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |
| Power consumption | $P_d$ | $T_a$ = 70 °C | Shrink DIP | 480 | mW |
| | | | Mini flat | 250 | |

**Note 1.** CMOS input/output or N-ch open-drain output + pull-up resistor built-in input/output

**2.** N-ch open-drain input/output

**Caution Even if one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product.** ★

### μPD7554A(A): ABSOLUTE MAXIMUM RATINGS ($T_a$ = 25 °C)

| Parameter | Symbol | Test Conditions | | Rating | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | | –0.3 to +7.0 | V |
| Input voltage | $V_I$ | Except ports 10 and 11 | | –0.3 to $V_{DD}$ + 0.3 | V |
| | | Ports 10 and 11 | **Note 1** | –0.3 to $V_{DD}$ + 0.3 | V |
| | | | **Note 2** | –0.3 to +11 | V |
| Output voltage | $V_O$ | Except ports 8, 10, 11 | | –0.3 to $V_{DD}$ + 0.3 | V |
| | | Ports 8, 10 and 11 | **Note 1** | –0.3 to $V_{DD}$ + 0.3 | V |
| | | | **Note 2** | –0.3 to +11 | V |
| Output current high | $I_{OH}$ | 1 pin | | –5 | mA |
| | | All pins in total | | –15 | mA |
| Output current low | $I_{OL}$ | 1 pin | P01, P02 | 5 | mA |
| | | | Port 8 | 30 | mA |
| | | | Others | 15 | mA |
| | | All pins in total | | 100 | mA |
| Operating temperature | $T_{opt}$ | | | –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |
| Power consumption | $P_d$ | $T_a$ = 85 °C | Shrink DIP | 350 | mW |
| | | | Mini flat | 195 | |

**Note 1.** CMOS input/output or N-ch open-drain output + pull-up resistor built-in input/output

**2.** N-ch open-drain input/output

**Caution Even if one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product.**

### CAPACITY ($T_a$ = 25 °C, $V_{DD}$ = 0 V)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input capacity | $C_{IN}$ | f = 1 MHz Unmeasured pins returned to 0 V. | P00, P03 | | | 15 | pF |
| Output capacity | $C_{OUT}$ | | Port 8 | | | 35 | pF |
| I/O capacity | $C_{IO}$ | | P01, P02 | | | 15 | pF |
| | | | Ports 10 and 11 | | | 35 | pF |

**RESONATOR CHARACTERISTICS** (**μPD7554A : $T_a$ = –10 to +70 °C, $V_{DD}$ = 2.7 to 6.0 V**; **μPD7554A(A) : $T_a$ = –40 to +85 °C, $V_{DD}$ = 2.7 to 6.0 V**)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| System clock oscillator frequency (CL1 and CL2) | $f_{CC}$ | $V_{DD}$ = 5 V ± 10%<br>R = 56 kΩ ± 2 % | | 400 | 500 | 600 | kHz |
| | | $V_{DD}$ = 3 V ± 10%<br>R = 100 kΩ ± 2% | | 200 | 250 | 300 | kHz |
| System clock input frequency (CL1) | $f_C$ | Duty = 50% | $V_{DD}$ = 4.5 to 6.0 V | 10 | | 710 | kHz |
| | | | | 10 | | 350 | kHz |
| CL1 input rising and falling time | $t_{CR}$, $t_{CF}$ | | | | | 0.2 | μs |
| CL1 input high/low level duration | $t_{CH}$, $t_{CL}$ | $V_{DD}$ = 4.5 to 6.0 V | | 0.7 | | 50 | μs |
| | | | | 1.45 | | 50 | μs |

**RESONATOR CHARACTERISTICS ($T_a$ = –10 to +70 °C, $V_{DD}$ = 2.5 to 3.3 V)[Note]**

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock oscillator frequency (CL1 and CL2) | $f_{CC}$ | R = 150 kΩ ± 2% | 140 | 180 | 220 | kHz |
| | | R = 150 kΩ ± 2%<br>$V_{DD}$ = 2.5 V | 140 | 175 | 210 | kHz |
| System clock input frequency (CL1) | $f_C$ | Duty = 50 % | 10 | | 250 | kHz |
| CL1 input rising and falling time | $t_{CR}$, $t_{CF}$ | | | | 0.2 | μs |
| CL1 input high/low level duration | $t_{CH}$, $t_{CL}$ | | 2 | | 50 | μs |

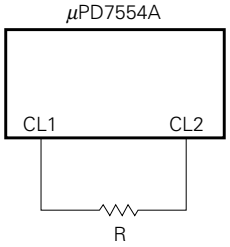
**RESONATOR CHARACTERISTICS ($T_a$ = –10 to +70 °C, $V_{DD}$ = 2.0 to 3.3 V)[Note]**

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock oscillator frequency (CL1 and CL2) | $f_{CC}$ | R = 240 kΩ ± 2% | 65 | 120 | 145 | kHz |
| | | R = 240 kΩ ± 2%<br>$V_{DD}$ = 2.0 V | 65 | 100 | 130 | kHz |
| System clock input frequency (CL1) | $f_C$ | Duty = 50 % | 10 | | 150 | kHz |
| CL1 input rising and falling time | $t_{CR}$, $t_{CF}$ | | | | 0.2 | μs |
| CL1 input high/low level duration | $t_{CH}$, $t_{CL}$ | | 3.3 | | 50 | μs |

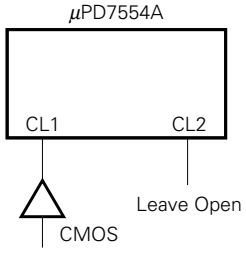
**Note** μPD7554A only

The following circuits are recommended:

① RC oscillation




② External clock



**DC CHARACTERISTICS** ($\mu$PD7554A : $T_a$ = –10 to +70 °C, $V_{DD}$ = 2.7 to 6.0 V; $\mu$PD7554A(A) : $T_a$ = –40 to +85 °C, $V_{DD}$ = 2.7 to 6.0 V)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage high | $V_{IH1}$ | Except CL1 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | CL1 | | $V_{DD}$ – 0.5 | | $V_{DD}$ | V |
| | $V_{IH3}$ | Ports 10 and 11 Note1 | | 0.7$V_{DD}$ | | 9 | V |
| Input voltage low | $V_{IL1}$ | Except CL1 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL2}$ | CL1 | | 0 | | 0.5 | V |
| Output voltage high | $V_{OH}$ | $V_{DD}$ = 4.5 to 6.0 V<br>$I_{OH}$ = –1 mA | | $V_{DD}$ – 2.0 | | | V |
| | | $I_{OH}$ = –100 $\mu$A | | $V_{DD}$ – 1.0 | | | V |
| Output voltage low | $V_{OL}$ | P01, P02 | $V_{DD}$ = 4.5 to 6.0 V<br>$I_{OL}$ = 1.6 mA | | | 0.4 | V |
| | | | $I_{OL}$ = 400 $\mu$A | | | 0.5 | V |
| | | Ports 10 and 11 | $V_{DD}$ = 4.5 to 6.0 V<br>$I_{OL}$ = 1.6 mA | | | 0.4 | V |
| | | | $V_{DD}$ = 4.5 to 6.0 V<br>$I_{OL}$ = 10 mA | | | 2.0 | V |
| | | | $I_{OL}$ = 400 $\mu$A | | | 0.5 | V |
| | | Port 8 | $V_{DD}$ = 4.5 to 6.0 V<br>$I_{OL}$ = 15 mA | | | 2.0 | V |
| | | | $I_{OL}$ = 600 $\mu$A | | | 0.5 | V |
| Input leak current high | $I_{LIH1}$ | $V_{IN}$ = $V_{DD}$ | Except CL1 | | | 3 | $\mu$A |
| | $I_{LIH2}$ | | CL1 | | | 10 | $\mu$A |
| | $I_{LIH3}$ | $V_{IN}$ = 9 V, ports 10 and 11 Note1 | | | | 10 | $\mu$A |
| Input leak current low | $I_{LIL1}$ | $V_{IN}$ = 0 V | Except CL1 | | | –3 | $\mu$A |
| | $I_{LIL2}$ | | CL1 | | | –10 | $\mu$A |
| Output leak current high | $I_{LOH1}$ | $V_{OUT}$ = $V_{DD}$ | | | | 3 | $\mu$A |
| | $I_{LOH2}$ | $V_{OUT}$ = 9 V, ports 8, 10, and 11 Note1 | | | | 10 | $\mu$A |
| Output leak current low | $I_{LOL}$ | $V_{OUT}$ = 0 V | | | | –3 | $\mu$A |
| Input pin built-in resistor (pull-up/down resistor) | | Port 0, RESET | | 23.5 | 47 | 70.5 | KΩ |
| Output pin built-in resistor (pull-up resistor) | | Ports 10 and 11 | | 7.5 | 15 | 22.5 | KΩ |
| Supply current Note2 | $I_{DD1}$ | Operating mode | $V_{DD}$ = 5 V ± 10 %<br>R = 56 kΩ ± 2 % | | 270 | 900 | $\mu$A |
| | | | $V_{DD}$ = 3 V ± 10 %<br>R = 100 kΩ ± 2 % | | 80 | 240 | $\mu$A |
| | $I_{DD2}$ | HALT mode | $V_{DD}$ = 5 V ± 10 %<br>R = 56 kΩ ± 2 % | | 120 | 400 | $\mu$A |
| | | | $V_{DD}$ = 3 V ± 10 %<br>R = 100 kΩ ± 2 % | | 35 | 110 | $\mu$A |
| | $I_{DD3}$ | STOP mode | $V_{DD}$ = 5 V ± 10 % | | 0.1 | 10 | $\mu$A |
| | | | $V_{DD}$ = 3 V ± 10 % | | 0.1 | 5 | $\mu$A |

**Note 1.** For N-ch open-drain input/output selection

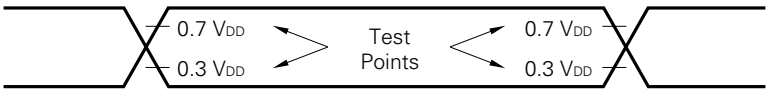
**2.** The current flowing in built-in pull-up and pull-down resistors is excluded.

**AC CHARACTERISTICS** ($\mu$PD7554A : $T_a$ = –10 to +70 °C, $V_{DD}$ = 2.7 to 6.0 V; $\mu$PD7554A(A) : $T_a$ = –40 to +85 °C, $V_{DD}$ = 2.7 to 6.0 V)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Internal clock cycle time | $t_{CY}$ Note | $V_{DD}$ = 4.5 to 6.0 V | | 2.8 | | 200 | μs |
| | | | | 5.7 | | 200 | μs |
| P00 event input frequency | $f_{PO}$ | Duty = 50% | $V_{DD}$ = 4.5 to 6.0 V | 0 | | 710 | kHz |
| | | | | 0 | | 350 | kHz |
| P00 input rise/fall time | $t_{POR}$, $t_{POF}$ | | | | | 0.2 | μs |
| P00 input high/low level width | $t_{POH}$, $t_{POL}$ | $V_{DD}$ = 4.5 to 6.0 V | | 0.7 | | | μs |
| | | | | 1.45 | | | μs |
| $\overline{SCK}$ cycle time | $t_{KCY}$ | Input | $V_{DD}$ = 4.5 to 6.0 V | 2.0 | | | μs |
| | | Output | | 2.5 | | | μs |
| | | Input | | 5.0 | | | μs |
| | | Output | | 5.7 | | | μs |
| $\overline{SCK}$ high/low level width | $t_{KH}$, $t_{KL}$ | Input | $V_{DD}$ = 4.5 to 6.0 V | 1.0 | | | μs |
| | | Output | | 1.25 | | | μs |
| | | Input | | 2.5 | | | μs |
| | | Output | | 2.85 | | | μs |
| SI setup time (to $\overline{SCK}\uparrow$) | $t_{SIK}$ | | | 100 | | | ns |
| SI hold time (from $\overline{SCK}\uparrow$) | $t_{KSI}$ | | | 100 | | | ns |
| $\overline{SCK}\downarrow\rightarrow$ SO output delay time | $t_{KSO}$ | $V_{DD}$ = 4.5 to 6.0 V | | | | 850 | ns |
| | | | | | | 1200 | ns |
| INT0 high/low level width | $t_{IOH}$, $t_{IOL}$ | | | 10 | | | μs |
| RESET high/low level width | $t_{RSH}$, $t_{RSL}$ | | | 10 | | | μs |

**Note** $t_{CY}$ = 2/$f_{CC}$ or 2/$f_C$

**AC Timing Test Point** (Except CL1 Input)



**DC CHARACTERISTICS ($T_a$ = –10 to +70 °C, $V_{DD}$ = 2.5 to 3.3 V)[Note1]**

| Parameter | Symbol | Test Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage high | $V_{IH1}$ | Except CL1 | | | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | CL1 | | | $V_{DD}$ – 0.3 | | $V_{DD}$ | V |
| | $V_{IH3}$ | Ports 10 and 11 [Note2] | | | 0.8 $V_{DD}$ | | 9 | V |
| Input voltage low | $V_{IL1}$ | Except CL1 | | | 0 | | 0.2$V_{DD}$ | V |
| | $V_{IL2}$ | CL1 | | | 0 | | 0.3 | V |
| | $V_{IL3}$ | Ports 10 and 11 | | | 0 | | 0.2$V_{DD}$ | V |
| Output voltage high | $V_{OH}$ | | | $I_{OH}$ = –80 μA | $V_{DD}$ – 1.0 | | | V |
| Output voltage low | $V_{OL}$ | P01, P02 | | $I_{OL}$ = 350 μA | | | 0.5 | V |
| | | Ports 10 and 11 | | $I_{OL}$ = 350 μA | | | 0.5 | V |
| | | Port 8 | | $I_{OL}$ = 500 μA | | | 0.5 | V |
| Input leak current high | $I_{LIH1}$ | $V_{IN}$ = $V_{DD}$ | | Except CL1 | | | 3 | μA |
| | $I_{LIH2}$ | | | CL1 | | | 10 | μA |
| | $I_{LIH3}$ | $V_{IN}$ = 9 V, ports 10 and 11 [Note2] | | | | | 10 | μA |
| Input leak current low | $I_{LIL1}$ | $V_{IN}$ = 0 V | | Except CL1 | | | –3 | μA |
| | $I_{LIL2}$ | | | CL1 | | | –10 | μA |
| Output leak current high | $I_{LOH1}$ | $V_{OUT}$ = $V_{DD}$ | | | | | 3 | μA |
| | $I_{LOH2}$ | $V_{OUT}$ = 9 V, ports 8, 10, and 11 [Note2] | | | | | 10 | μA |
| Output leak current low | $I_{LOL}$ | $V_{OUT}$ = 0 V | | | | | –3 | μA |
| Input pin built-in resistor (pull-up/down resistor) | | Port 0, RESET | | | 23.5 | 47 | 70.5 | KΩ |
| Output pin built-in resistor (pull-up resistor) | | Ports 10 and 11 | | | 7.5 | 15 | 22.5 | KΩ |
| Supply current [Note3] | $I_{DD1}$ | Operating mode | R = 150 kΩ ± 2% | $V_{DD}$ = 3 V ± 10% | | 55 | 180 | μA |
| | | | | $V_{DD}$ = 2.5 V | | 40 | 150 | μA |
| | $I_{DD2}$ | HALT mode | | $V_{DD}$ = 3 V ± 10% | | 25 | 80 | μA |
| | | | | $V_{DD}$ = 2.5 V | | 18 | 60 | μA |
| | $I_{DD3}$ | STOP mode | | | | 0.1 | 5 | μA |

**Note 1.** μPD7554A only

**2.** For N-ch open-drain input/output selection

**3.** The current flowing in built-in pull-up and pull-down resistors is excluded.

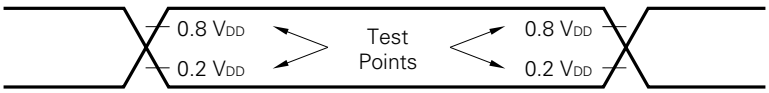
**AC CHARACTERISTICS ($T_a$ = –10 to +70 °C, $V_{DD}$ = 2.5 to 3.3 V)[Note1]**

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Internal clock cycle time | $t_{CY}$[Note2] | | 8.0 | | 200 | μs |
| P00 event input frequency | $f_{PO}$ | | 0 | | 250 | kHz |
| P00 input rise/fall time | $t_{POR}$, $t_{POF}$ | | | | 0.2 | μs |
| P00 input high/low level width | $t_{POH}$, $t_{POL}$ | | 2.0 | | | μs |
| $\overline{SCK}$ cycle time | $t_{KCY}$ | Input | 8.0 | | | μs |
| | | Output | 10.0 | | | μs |
| $\overline{SCK}$ high/low level width | $t_{KH}$, $t_{KL}$ | Input | 4.0 | | | μs |
| | | Output | 5.0 | | | μs |
| SI setup time (to $\overline{SCK}\uparrow$) | $t_{SIK}$ | | 300 | | | ns |
| SI hold time (from $\overline{SCK}\uparrow$) | $t_{KSI}$ | | 300 | | | ns |
| $\overline{SCK}\downarrow\rightarrow$SO output delay time | $t_{KSO}$ | $C_L$ = 100 pF | | | 2000 | ns |
| INT0 high/low level width | $t_{IOH}$, $t_{IOL}$ | | 30 | | | μs |
| RESET high/low level width | $t_{RSH}$, $t_{RSL}$ | | 30 | | | μs |

**Note 1.** μPD7554A only

**2.** $t_{CY}$ = 2/$f_{CC}$ or 2/$f_C$

**AC Timing Test Point** (Except CL1 Input)



**DC CHARACTERISTICS ($T_a$ = –10 to +70 °C, $V_{DD}$ = 2.0 to 3.3 V)[Note1]**

| Parameter | Symbol | Test Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage high | $V_{IH1}$ | Except CL1 | | | 0.85$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | CL1 | | | $V_{DD}$ – 0.2 | | $V_{DD}$ | V |
| | $V_{IH3}$ | Ports 10 and 11 [Note2] | | | 0.85$V_{DD}$ | | 9 | V |
| Input voltage low | $V_{IL1}$ | Except CL1 | | | 0 | | 0.15$V_{DD}$ | V |
| | $V_{IL2}$ | CL1 | | | 0 | | 0.2 | V |
| | $V_{IL3}$ | Ports 10 and 11 | | | 0 | | 0.2$V_{DD}$ | V |
| Output voltage high | $V_{OH}$ | | | $I_{OH}$ = –70 μA | $V_{DD}$ – 1.0 | | | V |
| Output voltage low | $V_{OL}$ | P01, P02 | | $I_{OL}$ = 270 μA | | | 0.5 | V |
| | | Ports 10 and 11 | | $I_{OL}$ = 300 μA | | | 0.5 | V |
| | | Port 8 | | $I_{OL}$ = 400 μA | | | 0.5 | V |
| Input leak current high | $I_{LIH1}$ | $V_{IN}$ = $V_{DD}$ | | Except CL1 | | | 3 | μA |
| | $I_{LIH2}$ | | | CL1 | | | 10 | μA |
| | $I_{LIH3}$ | $V_{IN}$ = 9 V, ports 10 and 11 [Note2] | | | | | 10 | μA |
| Input leak current low | $I_{LIL1}$ | $V_{IN}$ = 0 V | | Except CL1 | | | –3 | μA |
| | $I_{LIL2}$ | | | CL1 | | | –10 | μA |
| Output leak current high | $I_{LOH1}$ | $V_{OUT}$ = $V_{DD}$ | | | | | 3 | μA |
| | $I_{LOH2}$ | $V_{OUT}$ = 9 V, ports 8, 10, and 11 [Note2] | | | | | 10 | μA |
| Output leak current low | $I_{LOL}$ | $V_{OUT}$ = 0 V | | | | | –3 | μA |
| Input pin built-in resistor (pull-up/ down resistor) | | Port 0, RESET | | | 23.5 | 47 | 70.5 | KΩ |
| Output pin built-in resistor (pull-up resistor) | | Ports 10 and 11 | | | 7.5 | 15 | 22.5 | KΩ |
| Supply current [Note3] | $I_{DD1}$ | Operating mode | R = 240 kΩ ± 2% | $V_{DD}$ = 3 V ± 10% | | 38 | 130 | μA |
| | | | | $V_{DD}$ = 2.0 V | | 20 | 70 | μA |
| | $I_{DD2}$ | HALT mode | | $V_{DD}$ = 3 V ± 10% | | 17 | 60 | μA |
| | | | | $V_{DD}$ = 2.0 V | | 8 | 25 | μA |
| | $I_{DD3}$ | STOP mode | | | | 0.1 | 5 | μA |

**Note 1.** μPD7554A only

**2.** For N-ch open-drain input/output selection

**3.** The current flowing in built-in pull-up and pull-down resistors is excluded.

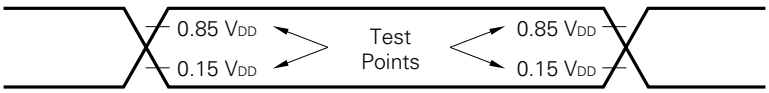
**AC CHARACTERISTICS ($T_a$ = –10 to +70 °C, $V_{DD}$ = 2.0 to 3.3 V)[Note1]**

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Internal clock cycle time | $t_{CY}$ [Note2] | | 13.4 | | 200 | μs |
| P00 event input frequency | $f_{PO}$ | | 0 | | 150 | kHz |
| P00 input rise/fall time | $t_{POR}$, $t_{POF}$ | | | | 0.2 | μs |
| P00 input high/low level width | $t_{POH}$, $t_{POL}$ | | 3.3 | | | μs |
| $\overline{SCK}$ cycle time | $t_{KCY}$ | Input | 13.4 | | | μs |
| | | Output | 16.6 | | | μs |
| $\overline{SCK}$ high/low level width | $t_{KH}$, $t_{KL}$ | Input | 6.7 | | | μs |
| | | Output | 8.3 | | | μs |
| SI setup time (to $\overline{SCK}\uparrow$) | $t_{SIK}$ | | 500 | | | ns |
| SI hold time (to $\overline{SCK}\uparrow$) | $t_{KSI}$ | | 500 | | | ns |
| $\overline{SCK}\downarrow\rightarrow$SO output delay time | $t_{KSO}$ | $C_L$ = 100 pF | | | 3500 | ns |
| INT0 high/low level width | $t_{IOH}$, $t_{IOL}$ | | 50 | | | μs |
| RESET high/low level width | $t_{RSH}$, $t_{RSL}$ | | 50 | | | μs |

**Note 1.** μPD7554A only

**2.** $t_{CY}$ = 2/$f_{CC}$ or 2/$f_C$

**AC Timing Test Point** (Except CL1 Input)

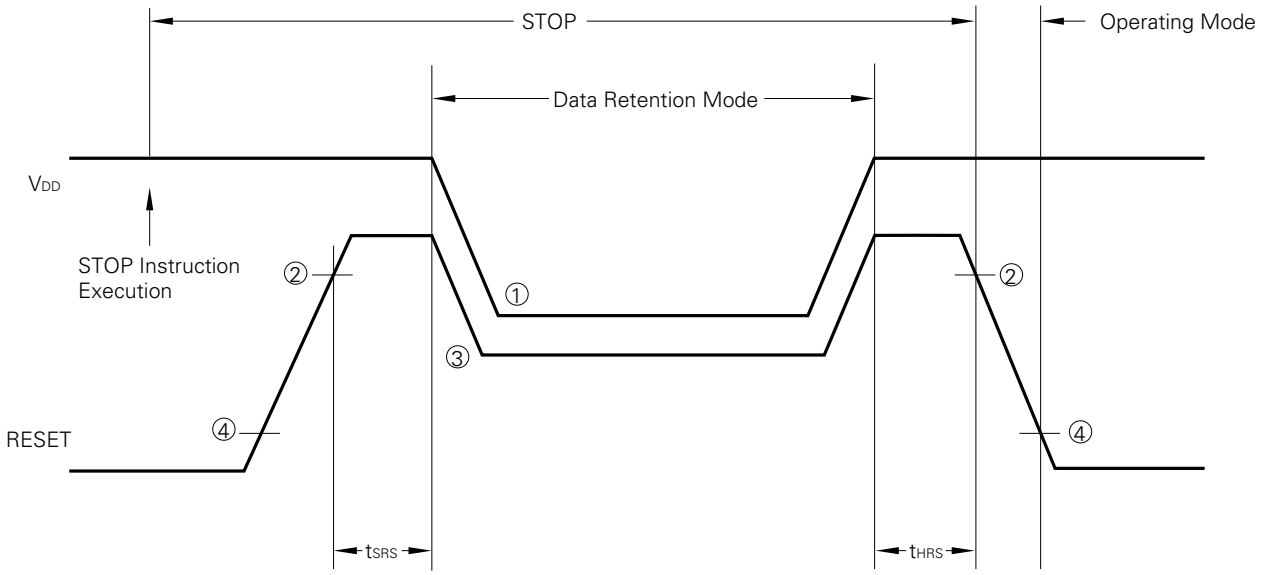


**CHARACTERISTICS OF DATA MEMORY DATA RETENTION AT LOW SUPPLY VOLTAGE IN STOP MODE**

**(μPD7554A : $T_a$ = –10 to +70 °C**
**μPD7554A(A) : $T_a$ = –40 to +85 °C)**

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 2.0 | | 6.0 | V |
| Data retention supply current | $I_{DDDR}$ | $V_{DDDR}$ = 2.0 V | | 0.1 | 5 | μA |
| Data retention high RESET input voltage | $V_{IHDR}$ | | 0.9 $V_{DDDR}$ | | $V_{DDDR}$ +0.2 | V |
| RESET setup time | $t_{SRS}$ | | 0 | | | μs |
| RESET hold time | $t_{HRS}$ | | 0 | | | μs |

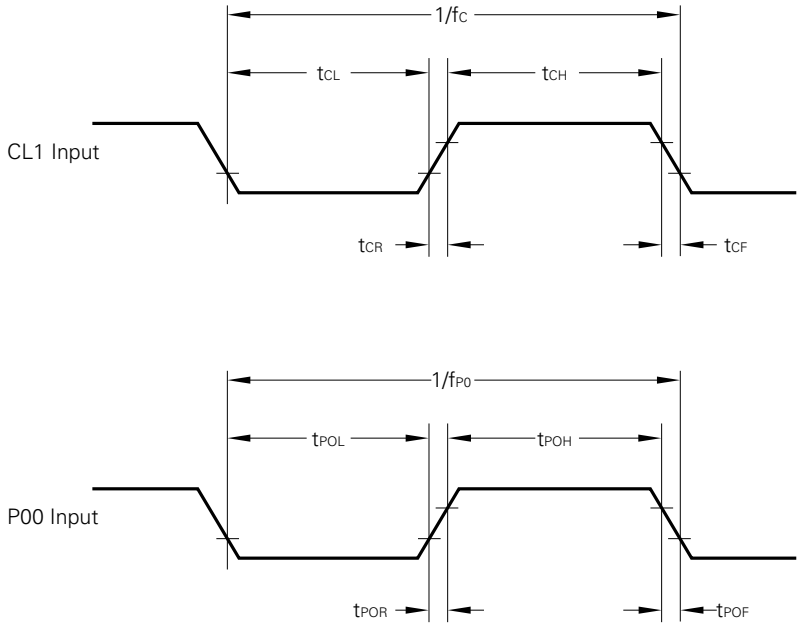
**Data Retention Timing**



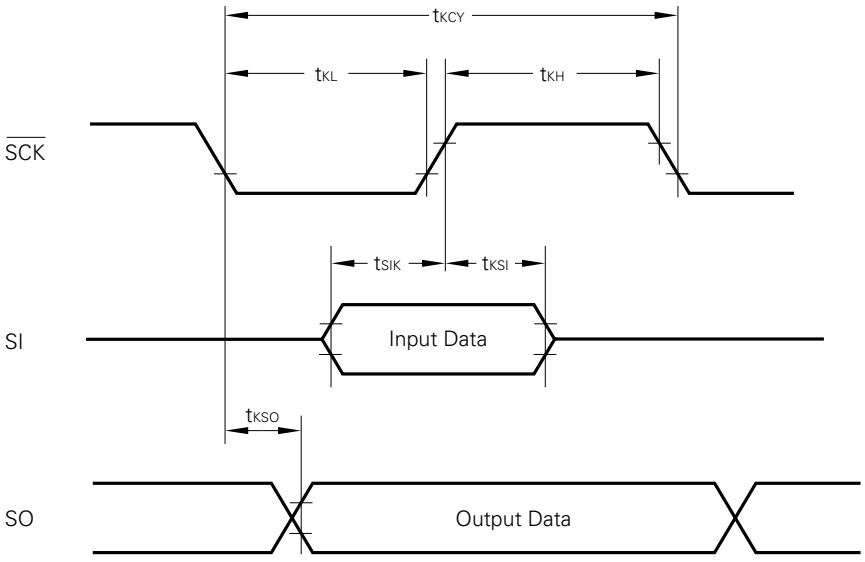

① $V_{DDDR}$
② $V_{IH1}$
③ $V_{IHDR}$
④ $IL_1$

**Caution In the data retention mode, every input must be below $V_{DDDR}$.**

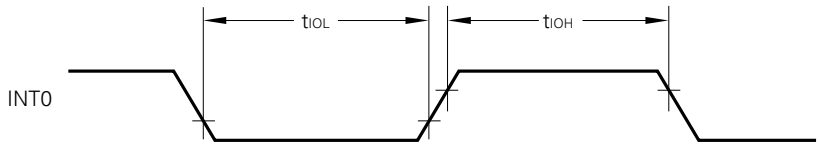
### Clock Timing



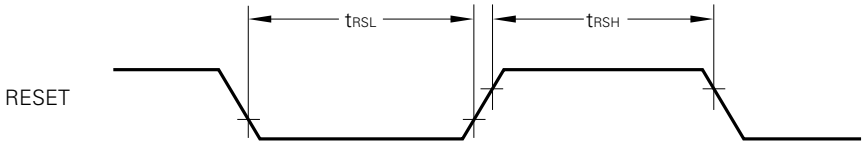

### Serial Transfer Timing



**Test Input Timing**



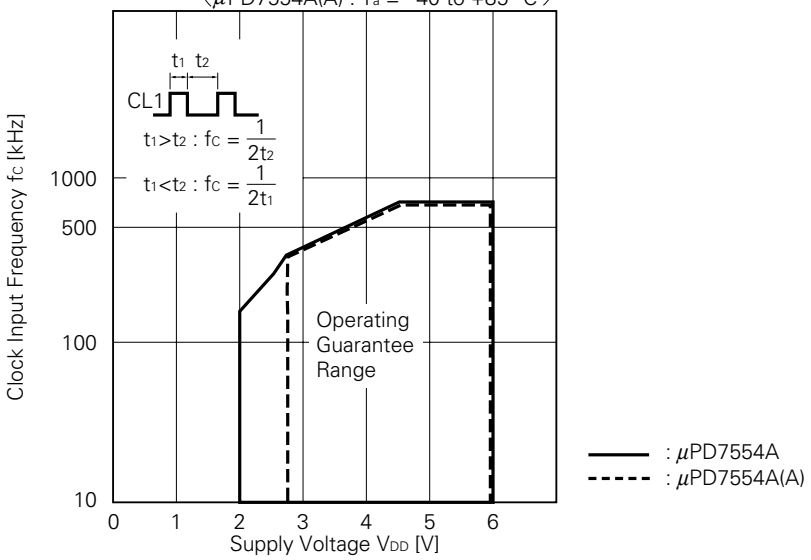

**RESET Input Timing**



## 7. CHARACTERISTIC CURVES

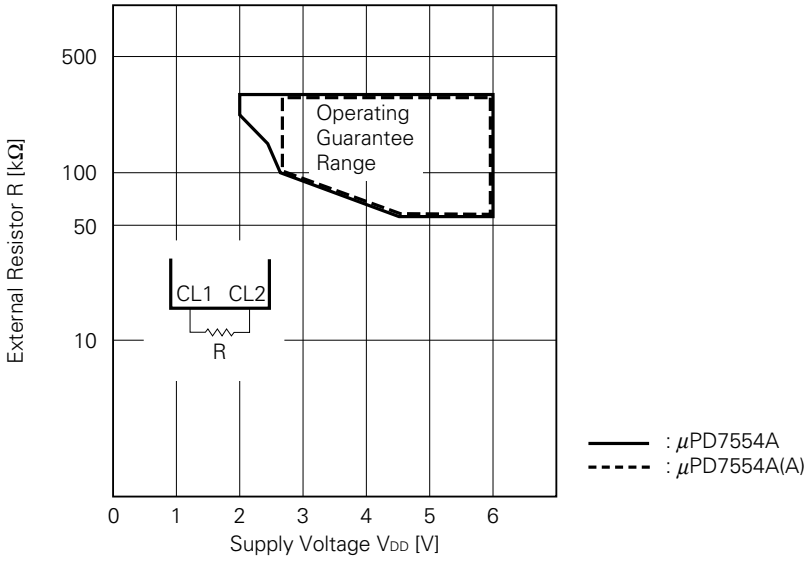
★ $f_C$ vs. $V_{DD}$ Operating Guarantee Range

($\mu$PD7554A : $T_a$ = –10 to +70 °C
$\mu$PD7554A(A) : $T_a$ = –40 to +85 °C)



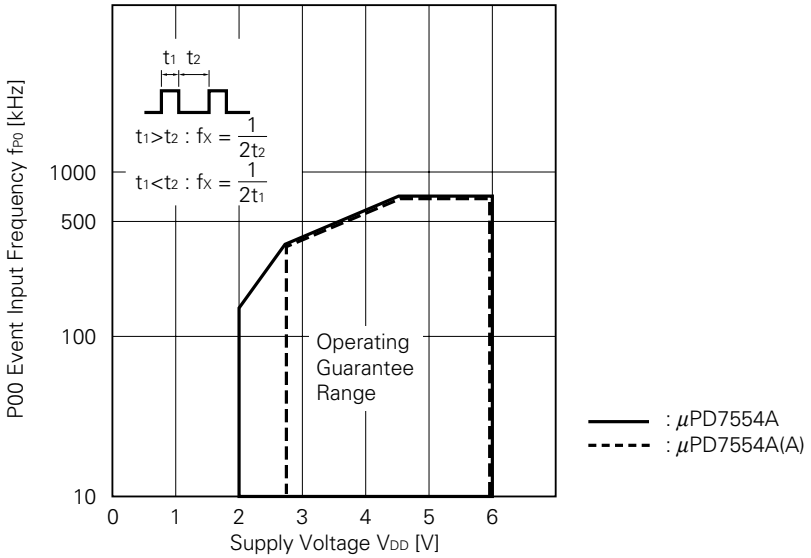

★ R vs. $V_{DD}$ Operating Guarantee Range

($\mu$PD7554A : $T_a$ = –10 to +70 °C
$\mu$PD7554A(A) : $T_a$ = –40 to +85 °C)

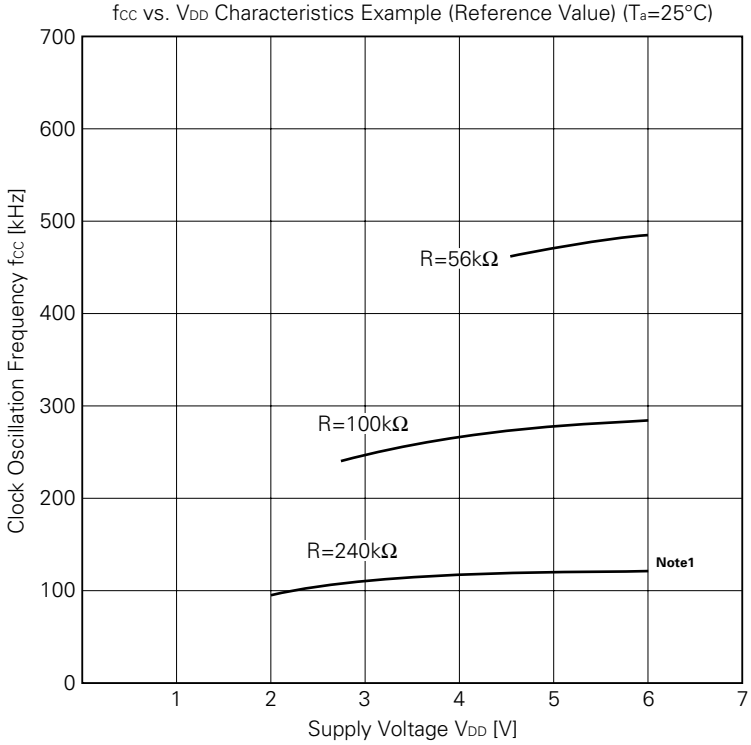



★ $f_{P0}$ vs. $V_{DD}$ Operating Guarantee Range

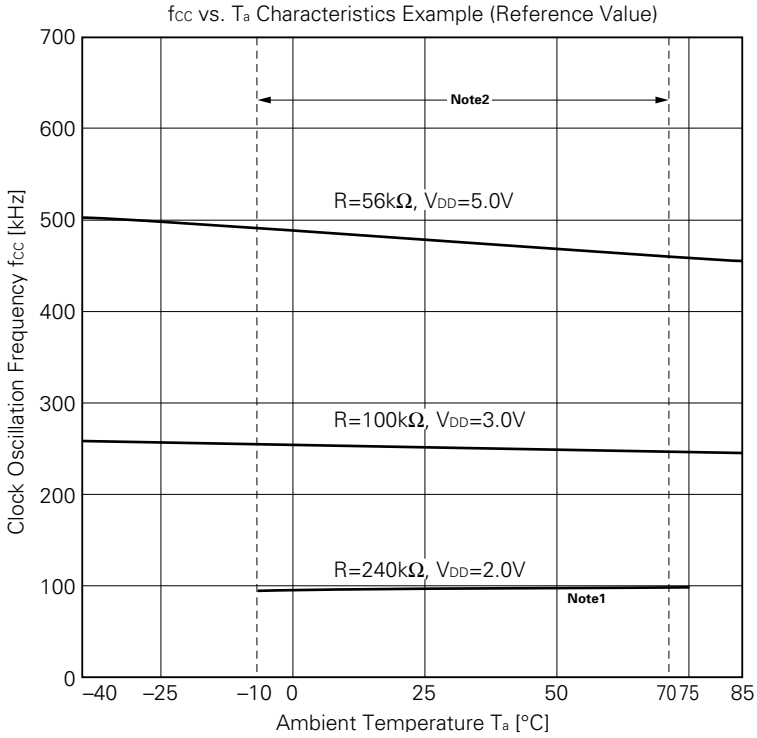
($\mu$PD7554A : $T_a$ = –10 to +70 °C
$\mu$PD7554A(A) : $T_a$ = –40 to +85 °C)



★ $f_{CC}$ vs. $V_{DD}$ Characteristics Example (Reference Value) ($T_a$=25°C)




★ $f_{CC}$ vs. $T_a$ Characteristics Example (Reference Value)

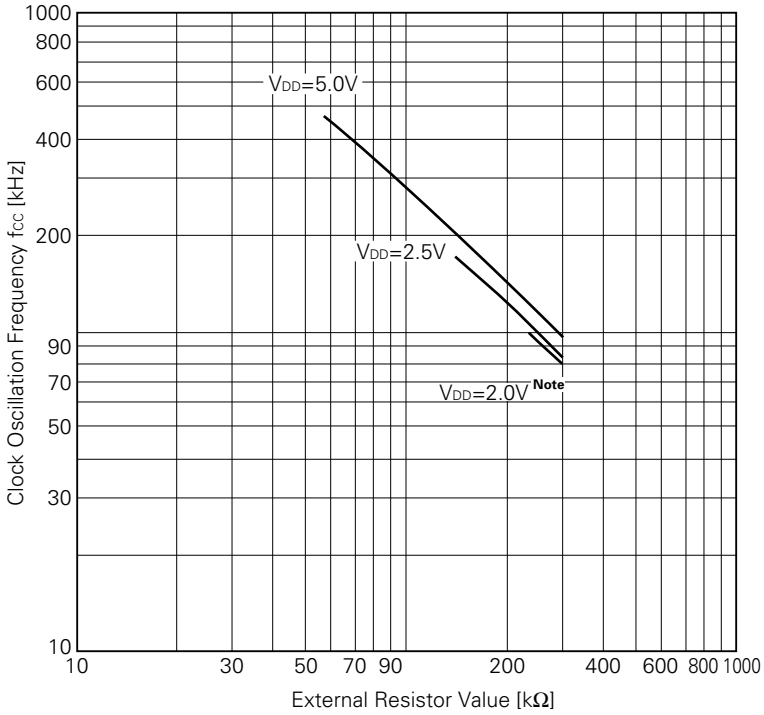



**Note 1.** μPD7554A only

**2.** μPD7554A only operates within this range

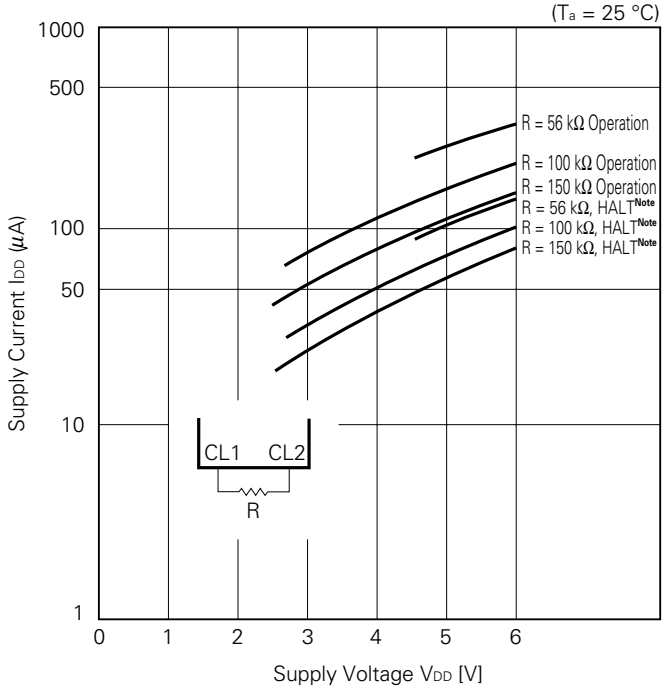
★

$f_{CC}$ vs. R Characteristics Example (Reference Value) ($T_a$=25°C)



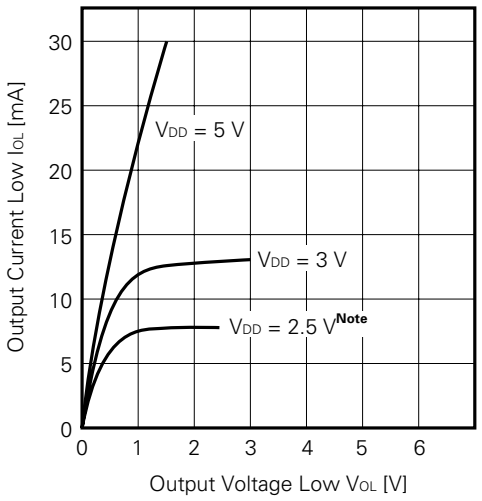

$I_{DD}$ vs. $V_{DD}$ Characteristic Example (Reference Value)

($T_a$ = 25 °C)



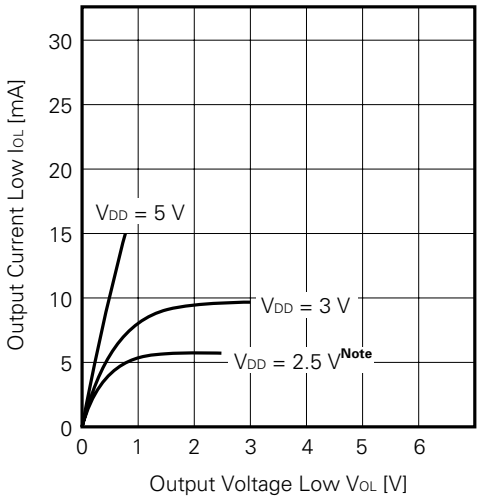

**Note** μPD7554A only

$I_{OL}$ vs. $V_{OL}$ Characteristic Example (Port 8)
(Reference Value)
($T_a$ = 25 °C)




**Caution The absolute maximum rating is 30 mA per pin.**

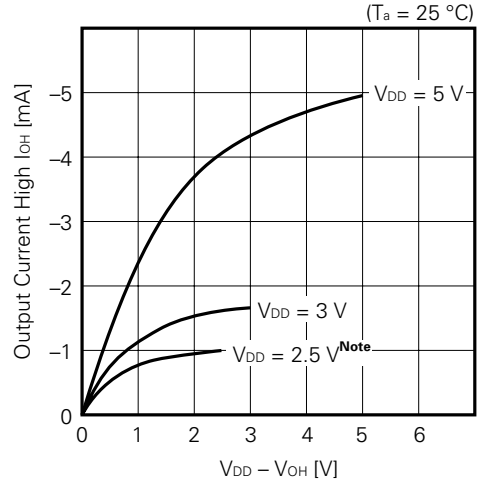
$I_{OL}$ vs. $V_{OL}$ Characteristic Example (Port 10, 11)
(Reference Value)
($T_a$ = 25 °C)




**Caution The absolute maximum rating is 15 mA per pin.**

**.**

$I_{OH}$ vs. $V_{OH}$ Characteristic Example
(Reference Value)
($T_a$ = 25 °C)

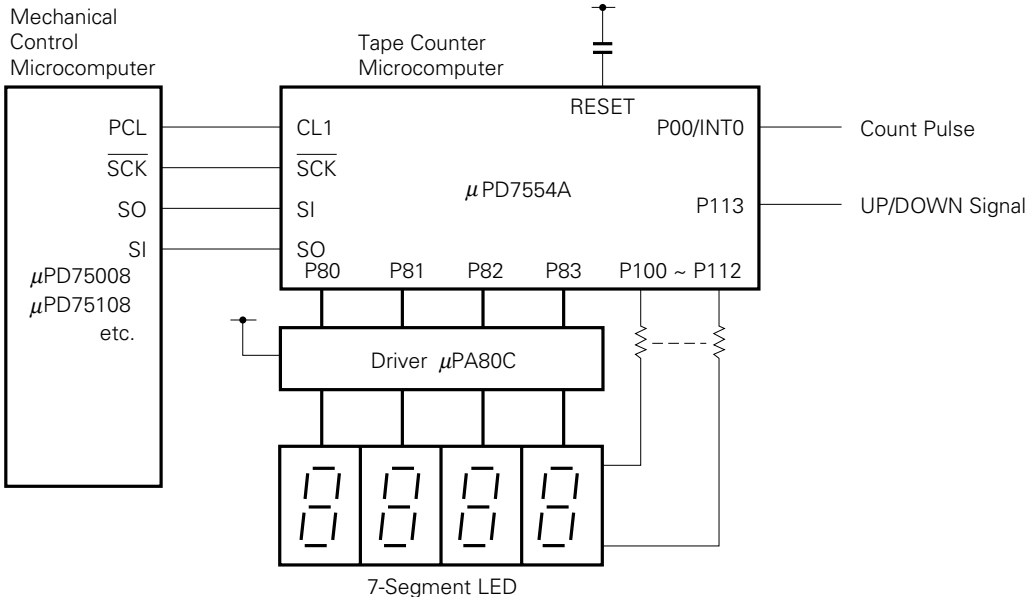



**Caution The absolute maximum rating is -5 mA per pin.**

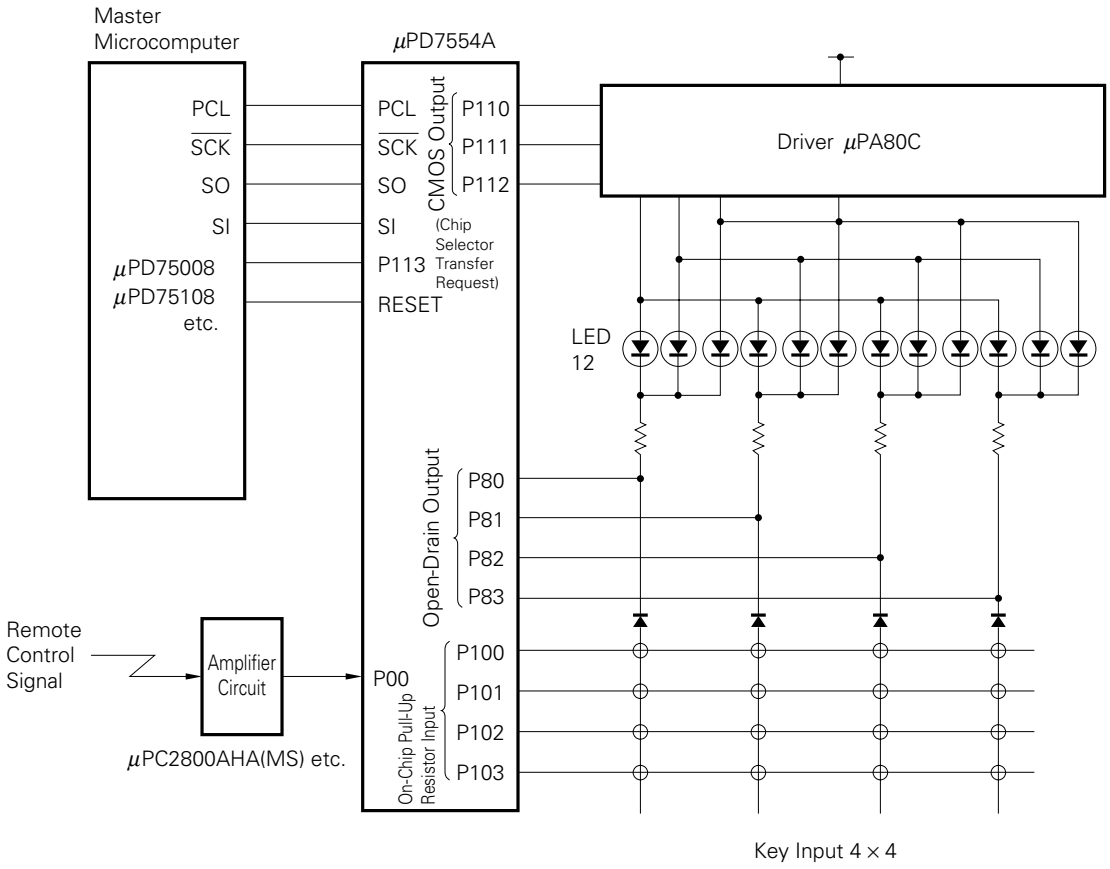
**Note** μPD7554A only

## 8. μPD7554A APPLIED CIRCUITS

### (1) Tape counter (VTR, deck)



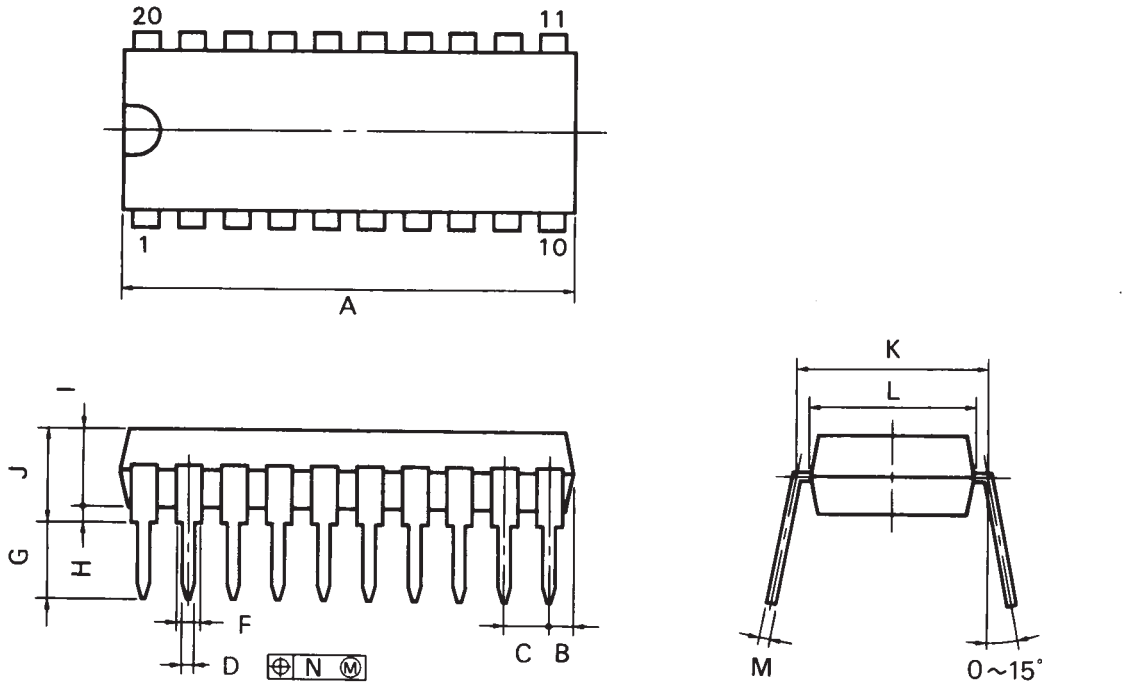

### (2) Remote control reception + key entry + LED display



## 9. PACKAGE INFORMATION

### DRAWINGS OF MASS-PRODUCTION PRODUCT PACKAGES (1/2)

## 20PIN PLASTIC SHRINK DIP (300 mil)




P20C-70-300B

**NOTES**

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

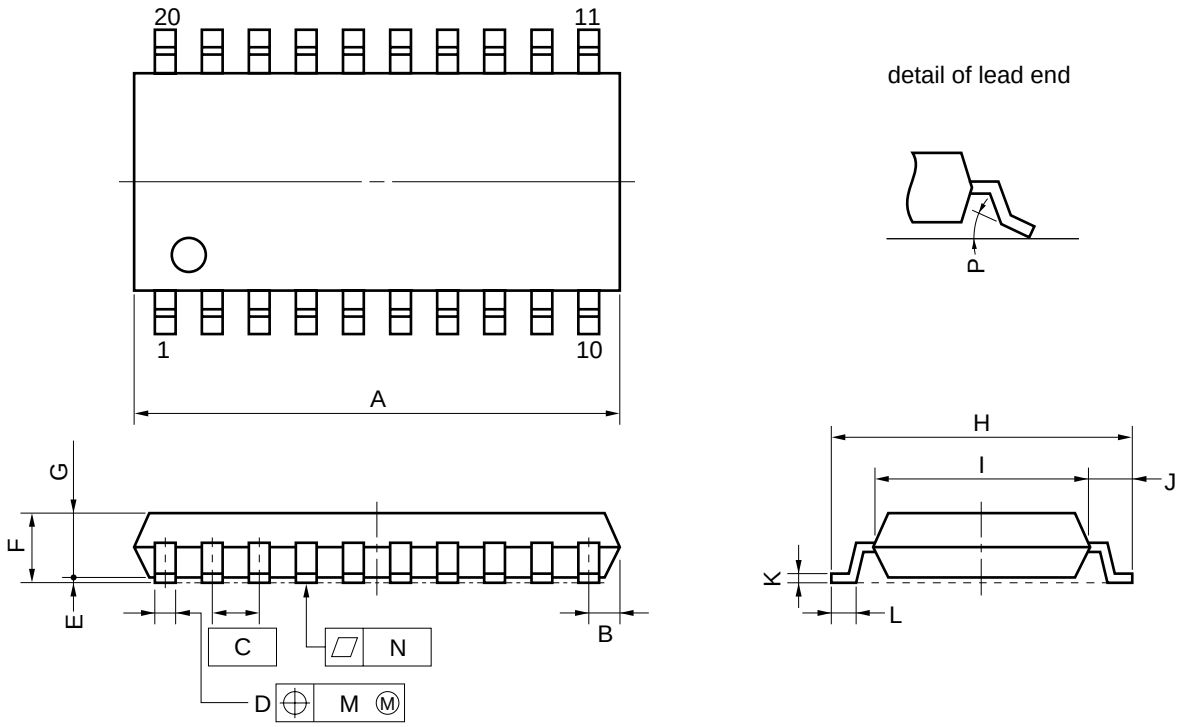
2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 19.57 MAX. | 0.771 MAX. |
| B | 1.78 MAX. | 0.070 MAX. |
| C | 1.778 (T.P.) | 0.070 (T.P.) |
| D | $0.50^{\pm 0.10}$ | $0.020^{+0.004}_{-0.005}$ |
| F | 0.85 MIN. | 0.033 MIN. |
| G | $3.2^{\pm 0.3}$ | $0.126^{\pm 0.012}$ |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.08 MAX. | 0.200 MAX. |
| K | 7.62 (T.P.) | 0.300 (T.P.) |
| L | 6.5 | 0.256 |
| M | $0.25^{+0.10}_{-0.05}$ | $0.010^{+0.004}_{-0.003}$ |
| N | 0.17 | 0.007 |

★ **Caution Dimentions of ES products are different from those of mass-production products. Refer to DRAWINGS OF ES PRODUCT PACKAGES (1/2).**

DRAWINGS OF MASS-PRODUCTION PRODUCT PACKAGES (2/2)

## 20 PIN PLASTIC SOP (300 mil)




**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

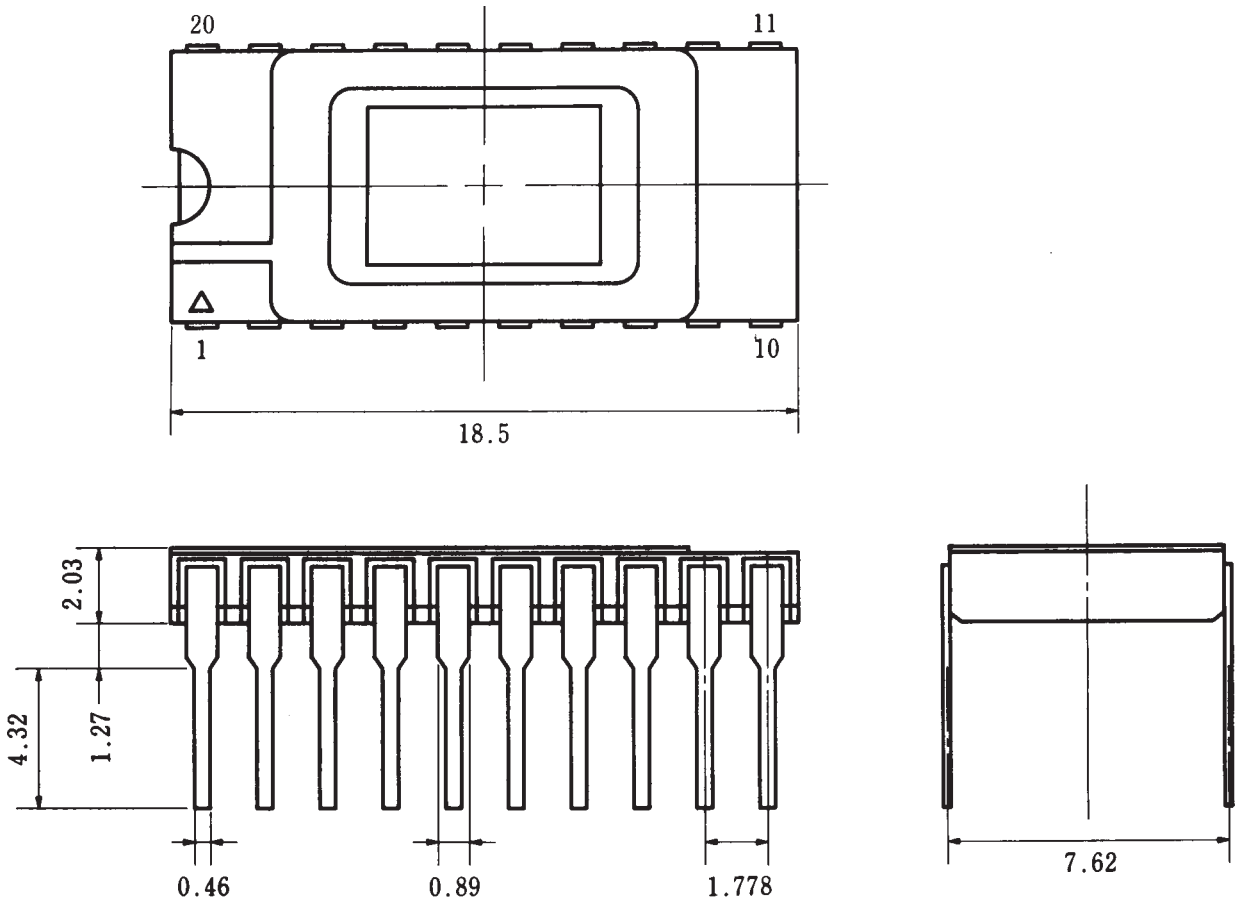
| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 13.00 MAX. | 0.512 MAX. |
| B | 0.78 MAX. | 0.031 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | $0.40^{+0.10}_{-0.05}$ | $0.016^{+0.004}_{-0.003}$ |
| E | 0.1±0.1 | 0.004±0.004 |
| F | 1.8 MAX. | 0.071 MAX. |
| G | 1.55 | 0.061 |
| H | 7.7±0.3 | 0.303±0.012 |
| I | 5.6 | 0.220 |
| J | 1.1 | 0.043 |
| K | $0.20^{+0.10}_{-0.05}$ | $0.008^{+0.004}_{-0.002}$ |
| L | 0.6±0.2 | $0.024^{+0.008}_{-0.009}$ |
| M | 0.12 | 0.005 |
| N | 0.10 | 0.004 |
| P | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |

P20GM-50-300B, C-4

**Caution Dimentions and materials of ES products are different from those of mass-production products. Refer to DRAWINGS OF ES PRODUCT PACKAGES (2/2).** ★

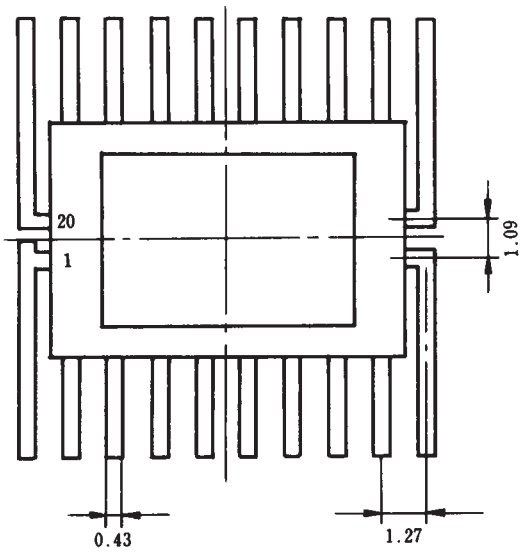
**DRAWINGS OF ES PRODUCT PACKAGES (1/2)**

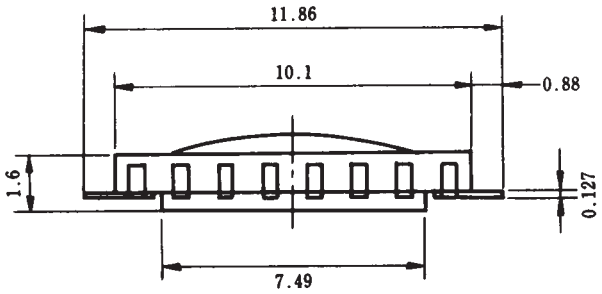
**20 PIN SHRINK DIP FOR ES (REFERENCE) (UNIT: mm)**

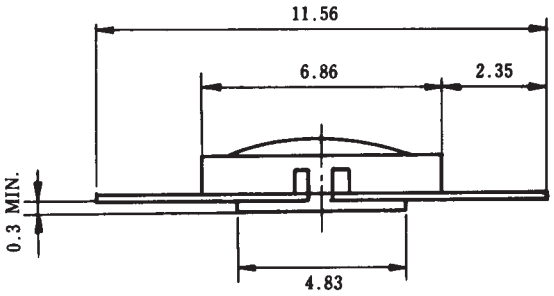


**DRAWINGS OF ES PRODUCT PACKAGES (2/2)**

**20 PIN CERAMIC SOP FOR ES (REFERENCE) (UNIT: mm)**

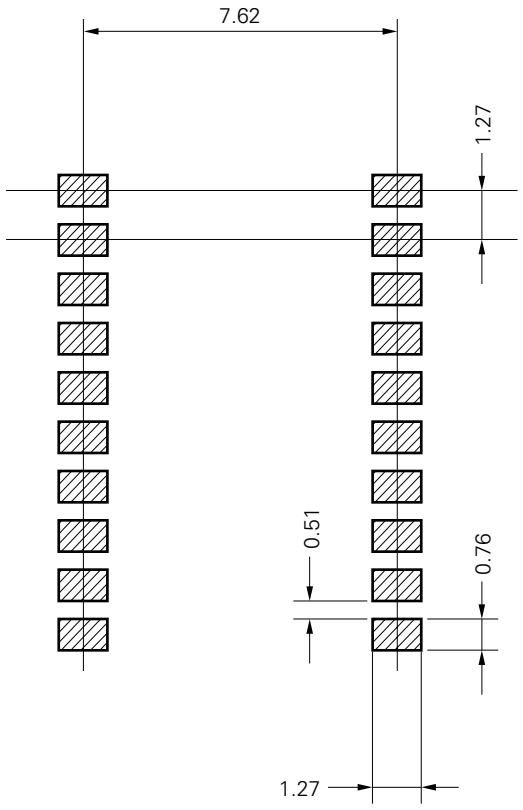



20B–50B

## 10. RECOMMENDED PACKAGING PATTERN OF PLASTIC SOP (REFERENCE) (UNIT: mm)




- This recommended pattern conforms to the General Rules for Integrated Citrcuit Outer Shape (IC-74-2) specified by the Electronic Industries Association of Japan (EIAJ).
- The above pattern dimensions are applicable to all the products designated as EIAJ flat DIP (mini flat) of "Form A 300 mil type".
- If there is any possibility of causing a solder bridge, adjust the width (0.76) of each pad while maintaining the same length (1.27).

## 11. RECOMMENDED SOLDERING CONDITIONS ★

Solder μPD7554A on the following recommended conditions.

For details of recommended soldering conditions, refer to the information document **"Semiconductor device mounting technology manual" (IEI-1207).**

For details on the soldering method and soldering conditions other than the recommended conditions, call the NEC salesman.

**Table 11-1 Surface Mounting Type Soldering Conditions**

**μPD7554AG-×××  : 20-pin plastic SOP (300 mil)**
**μPD7554AG(A)-×××: 20-pin plastic SOP (300 mil)**

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 230 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Once | IR30-00-1 |
| VPS | Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Once | VP15-00-1 |
| Wave soldering | Solder bath temperature: 260 °C or below, Duration: 10 sec. max., Number of times: once, Preparatory heating tempererature: 120 °C max. (Package surface temperature) | WS60-00-1 |
| Pin part heating | Pin temperature: 300 °C or below, Duration: 3 sec. max. (per device side) | — |

**Caution Use of more than one soldering method should be avoided (except in the case of pin part heating).**

**Table 11-2 Insertion Type Soldering Conditions**

**μPD7554ACS-×××  : 20-pin plastic shrink DIP (300 mil)**
**μPD7554ACS(A)-×××: 20-pin plastic shrink DIP (300 mil)**

| Soldering Method | Soldering Conditions |
|---|---|
| Wave soldering (pin only) | Solder bath temperatures: 260 °C or below, Duration: 10 sec. max. |
| Pin part heating | Pin temperature: 300 °C or below, Duration: 3 sec. max. (Per pin) |

**Caution Ensure that the application of wave soldering is limited to the pins and no solder touches the main unit directly.**

| Item \ Product Name | | μPD7554 | μPD75P54 | μPD7554A | μPD7554A(A) | μPD7564 | μPD75P64 | μPD7564A | μPD7564A(A) |
|---|---|---|---|---|---|---|---|---|---|
| Instruction cycle/ system clock (5 V) | RC | 4 μs/500 kHz | | | | – | | | |
| | Outside | 2.86 μs/700 kHz | | | | – | | | |
| | Ceramic | – | | | | 2.86 μs/700 kHz | | | |
| Instruction set | | 47 types (SET B) | | | | | | | |
| ROM | | 1024 × 8 | | | | | | | |
| RAM | | 64 × 4 | | | | | | | |
| I/O Ports | Total | 16 | | | | 15 | | | |
| | Port 0 | P00-P03 | | | | | | | |
| | Port 8 | P80-P82, P83 (CL2) | | | | P80-P82 | | | |
| | Withstand voltage | 12 V | | 9 V | | 12 V | | 9 V | |
| | Port 10 and 11 | P100-P103, P110-P113 | | | | | | | |
| | Withstand voltage | 12 V | | 9 V | | 12 V | | 9 V | |
| Timer/Event Counter | | 8 bits | | | | | | | |
| Serial Interface | | 4 channels | | | | | | | |
| Supply Voltage Range | | 2.5-6.0 V | 4.5-6.0 V | 2.0-6.0 V | 2.7-6.0 V | 2.7-6.0 V | 4.5-6.0 V | 2.7-6.0 V | 2.7-6.0 V |
| Package | | 20-pin plastic shrink DIP<br>20-pin plastic SOP | | | | | | | |

## APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for developing systems that use μPD7554A.

**Language Processor**

| | Host Machine | OS | Supply Medium | Ordering Code (Product Name) |
|---|---|---|---|---|
| μPD7550/7560 series absolute assembler | PC-9800 series | MS-DOS™ (Ver.3.10 to Ver.5.00A[Note]) | 3.5-inch 2HD | μS5A13AS7554 |
| | | | 5-inch 2HD | μS5A10AS7554 |
| | IBM PC/AT™ | PC DOS™ (Ver. 3.1) | 5-inch 2HC | μS7B10AS7554 |

**PROM Write Tools**

| | | | | | |
|---|---|---|---|---|---|
| Hardware | PG-1500 | PROM programmer which allows programming of single-chip microcomputer with typical PROM of 256K to 4M bits by stand-alone or from a host machine by connecting the accessory board and optional programmer adapter. | | | |
| | PA-75P54CS | μPD75P54/75P64 PROM programmer adapter. Used by connecting it to the PG-1500. | | | |
| Software | PG-1500 controller | Connects the PG-1500 and host machine by serial and parallel interface and controls the PG-1500 on the host machine. | | | |
| | | Host Machine | OS | Supply Medium | Ordering Code (Product Name) |
| | | PC-9800 series | MS-DOS (Ver.3.10 to Ver.5.00A[Note]) | 3.5-inch 2HD | μS5A13PG1500 |
| | | | | 5-inch 2HD | μS5A10PG1500 |
| | | IBM PC/AT | PC DOS (Ver.3.1) | 5-inch 2HC | μS7B10PG1500 |

**Note** A task swap function is provided in Ver. 5.00/5.00A, but the task swap function cannot be used with this software.

**Remark** Operation of the assembler and PG-1500 controller is only guaranteed on the host machines and OSs shown above.

**Debugging Tools**

<table>
<tr><td rowspan="3">Hardware</td><td>EVAKIT-7500B</td><td colspan="4">EVAKIT-7500B is an evaluation board that can be used for μPD7500 series models. For μPD7544A, EVAKIT-7500B and option board EV-7554A are combined and used for system development.<br>EVAKIT-7500B can operate alone. EVAKIT-7500B has a built-in serial interface on the board, so it enables debugging when it is connected to a TTY, TYPUTER, or RS-232-C console.<br>EVAKIT-7500B works as is a real-time tracer and traces state of the program counter and output port in real time. EVAKIT-7500B has a built-in PROM writer and improves debugging efficiency considerably.</td></tr>
<tr><td>EV-7554A</td><td colspan="4">EV-7554A is an adapter board which is connected to EVAKIT-7500B and evaluates μPD7554A.</td></tr>
<tr><td>SE-7554A</td><td colspan="4">SE-7554A is a simulation board that has the programs developed by EVAKIT-7500B. SE-7554A evaluates a system in place of μPD7554A.</td></tr>
<tr><td rowspan="5">Software</td><td rowspan="5">EVAKIT-7500<br>control program<br>(EVAKIT controller)</td><td colspan="4">EVAKIT-7500 Control Program connects EVAKIT-7500B and the host machine with RC-232-C and controls EVAKIT-7500B on the host machine.</td></tr>
<tr><td>Host Machine</td><td>OS</td><td>Supply Medium</td><td>Ordering Code<br>(Product Name)</td></tr>
<tr><td rowspan="2">PC-9800<br>series</td><td rowspan="2">MS-DOS<br>(Ver.3.10 to<br>Ver.5.00A<sup>Note</sup>)</td><td>3.5-inch 2HD</td><td>μS5A13EV7500-P01</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10EV7500-P01</td></tr>
<tr><td>IBM PC<br>series</td><td>PC DOS<br>(Ver.3.1)</td><td>5-inch 2HC</td><td>μS7B11EV7500-P01</td></tr>
</table>

**Note** A task swap function is provided in Ver. 5.00/5.00A, but the task swap function cannot be used with this software.

★ **Caution It is not possible to internally mount a pull-up resistor in a port in the EVAKIT-7500B. When evaluating, arrange to have a pull-up resistor mounted in the user system.**

**Remark** Operation of the assembler and PG-1500 controller is only guaranteed on the host machines and OSs shown above.

## APPENDIX C. RELATED DOCUMENTS ★

### DOCUMENT RELATED TO DEVICE

| Document Name | Document No. |
|---|---|
| User's Manual | IEU-1111D |
| μPD7500-series Selection Guide | IF-1027G |

### DOCUMENT RELATED TO DEVELOPMENT TOOL

| Document Name | | | Document No. |
|---|---|---|---|
| Hardware | EVAKIT-7500B User's Manual | | EEU-1017C |
| | EV-7554A User's Manual | | EEU-1034A |
| | PG-1500 User's Manual | | EEU-1335B |
| Software | μPD7550, 7560-series Absolute Assembler User's Manual | | EEM-1006 |
| | EVAKIT-7500 Control Program User's Manual | MS-DOS base | EEM-1356 |
| | | PC DOS base | EEM-1049 |
| | PG-1500 Controller User's Manual | | EEU-1291B |

### OTHER RELATED DOCUMENT

| Document Name | Document No. |
|---|---|
| Package Manual | IEI-1213 |
| Semiconductor Device Mounting Technology Manual | IEI-1207 |
| Quality Grade on NEC Semiconductor Devices | IEI-1209A |
| NEC Semiconductor Device Reliability/Quality Control System | IEI-1203A |
| Static Electricity Discharge (ESD) Test | IEI-1201 |
| Semiconductor Device Quality Guarantee Guide | MEI-1202 |
| Microcomputer-Related Product Guide-Third Party Product | **Note** |

**Remark** These documents above are subject to change without notice. Be sure to use the latest document for designing.

**Note** To be published.

[MEMO]

# NOTES FOR CMOS DEVICES

## ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.**

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.**

## ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.**

**[MEMO]**

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.



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