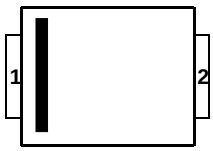
TISP5070H3BJ, TISP5080H3BJ, TISP5110H3BJ, TISP5150H3BJ
FORWARD-CONDUCTING
UNIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

JANUARY 1998 - REVISED MARCH 1999

TELECOMMUNICATION SYSTEM HIGH CURRENT OVERVOLTAGE PROTECTORS

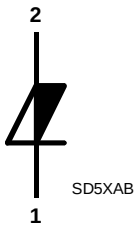
- **Analogue Line Card and ISDN Protection**
  - **Analogue SLIC**
  - **ISDN U Interface**
  - **ISDN Power Supply**
- **8 kV 10/700, 200 A 5/310 ITU-T K20/21 rating**
- **Ion-Implanted Breakdown Region**
  Precise and Stable Voltage
  Low Voltage Overshoot under Surge

SMBJ PACKAGE
(TOP VIEW)



MDXXBGB

device symbol



SD5XAB

DEVICE	V_{DRM} MINIMUM V	$V_{(BO)}$ MAXIMUM V
‘5070	-58	-70
‘5080	-65	-80
‘5110	-80	-110
‘5150	-120	-150

- **Rated for International Surge Wave Shapes**

WAVE SHAPE	STANDARD	I_{TSP} A
2/10 µs	GR-1089-CORE	500
8/20 µs	ANSI C62.41	300
10/160 µs	FCC Part 68	250
10/700 µs	ITU-T K20/21	200
10/560 µs	FCC Part 68	160
10/1000 µs	GR-1089-CORE	100

description

These devices are designed to limit overvoltages on the telephone and data lines. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line. A single device provides 2-point protection and is typically used for the protection of ISDN power supply feeds. Two devices, one for the Ring output and the other for the Tip output, will provide protection for single supply analogue SLICs. A combination of three devices will give a low capacitance protector network for the 3-point protection of ISDN lines.

The protector consists of a voltage-triggered unidirectional thyristor with an anti-parallel diode. Negative overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current prevents d.c. latchup as the diverted current subsides. Positive overvoltages are limited by the conduction of the anti-parallel diode.

This TISP5xxxH3BJ range consists of four voltage variants to meet various maximum system voltage levels (58 V to 120 V). They are guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. These high (H) current protection devices are in a plastic package SMBJ (JEDEC DO-214AA with J-bend leads) and supplied in embossed carrier reel pack.

absolute maximum ratings, T_A = 25°C (unless otherwise noted)

RATING		SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage, (see Note 1)	'5070	V_{DRM}	- 58	V
	'5080		- 65	
	'5110		- 80	
	'5150		-120	
Non-repetitive peak on-state pulse current (see Notes 2, 3 and 4)		I_{TSP}		A
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)			500	
8/20 µs (IEC 61000-4-5, 1.2/50 µs voltage, 8/20 current combination wave generator)			300	
10/160 µs (FCC Part 68, 10/160 µs voltage wave shape)			250	
5/200 µs (VDE 0433, 10/700 µs voltage wave shape)			220	
0.2/310 µs (I3124, 0.5/700 µs voltage wave shape)			200	
5/310 µs (ITU-T K20/21, 10/700 µs voltage wave shape)			200	
5/310 µs (FTZ R12, 10/700 µs voltage wave shape)			200	
10/560 µs (FCC Part 68, 10/560 µs voltage wave shape)			160	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)			100	
Non-repetitive peak on-state current (see Notes 2, 3 and 5)		I_{TSM}		A
20 ms (50 Hz) full sine wave			55	
16.7 ms (60 Hz) full sine wave			60	
1000 s 50 Hz/60 Hz a.c.			2.1	
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 140 A		di_T/dt	400	A/µs
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. See Figure 9 for voltage values at lower temperatures.
2. Initially the TISP5xxxH3BJ must be in thermal equilibrium with T_J = 25°C.
3. The surge may be repeated after the TISP5xxxH3BJ returns to its initial conditions.
4. See Figure 10 for current ratings at other temperatures.
5. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 8 for the current ratings at other durations. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C

electrical characteristics for terminal pair, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$	T_A = 25°C			-5	µA
			T_A = 85°C			-10	
$V_{(BO)}$	Breakover voltage	dv/dt = -750 V/ms, R_{SOURCE} = 300 Ω	'5070			-70	V
			'5080			-80	
			'5110			-110	
			'5150			-150	
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≥ -1000 V/µs, Linear voltage ramp, Maximum ramp value = -500 V di/dt = -20 A/µs, Linear current ramp, Maximum ramp value = -10 A	'5070			-80	V
			'5080			-90	
			'5110			-120	
			'5150			-160	
$I_{(BO)}$	Breakover current	dv/dt = -750 V/ms, R_{SOURCE} = 300 Ω		-0.15		-0.6	A
V_F	Forward voltage	I_F = 5 A, t_W = 500 µs	'5070 thru '5150			3	V
V_{FRM}	Peak forward recovery voltage	dv/dt ≤ +1000 V/µs, Linear voltage ramp, Maximum ramp value = +500 V di/dt = +20 A/µs, Linear current ramp, Maximum ramp value = +10 A	'5070 thru '5150			5	V
V_T	On-state voltage	I_T = -5 A, t_W = 500 µs				-3	V
I_H	Holding current	I_T = -5 A, di/dt = +30 mA/ms		-0.15		-0.6	A

PRODUCT INFORMATION

electrical characteristics for terminal pair, T_A = 25°C (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		-5			kV/µs
I_D	Off-state current	V_D = -50 V	T_A = 85°C			-10	µA
C_{off}	Off-state capacitance	f = 100 kHz, V_d = 1 Vrms, V_D = -1V, (see Note 6)	‘5070		300	420	pF
			‘5080		280	390	
			‘5110		240	335	
			‘5150		140	195	
		f = 100 kHz, V_d = 1 Vrms, V_D = -2 V	‘5070		260	365	
			‘5080		245	345	
			‘5110		205	285	
			‘5150		120	170	
		f = 100 kHz, V_d = 1 Vrms, V_D = -50 V	‘5070		90	125	
			‘5080		80	110	
			‘5110		65	90	
			‘5150		35	50	
		f = 100 kHz, V_d = 1 Vrms, V_D = -100 V	‘5150		30	40	

NOTE 6: Up to 10 MHz the capacitance is essentially independent of frequency. Above 10 MHz the effective capacitance is strongly dependent on connection inductance.

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, I_T = $I_{TSM(1000)}$, T_A = 25 °C, (see Note 7)			113	°C/W
		265 mm x 210 mm populated line card, 4-layer PCB, I_T = $I_{TSM(1000)}$, T_A = 25 °C		50		

NOTE 7: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

PARAMETER MEASUREMENT INFORMATION

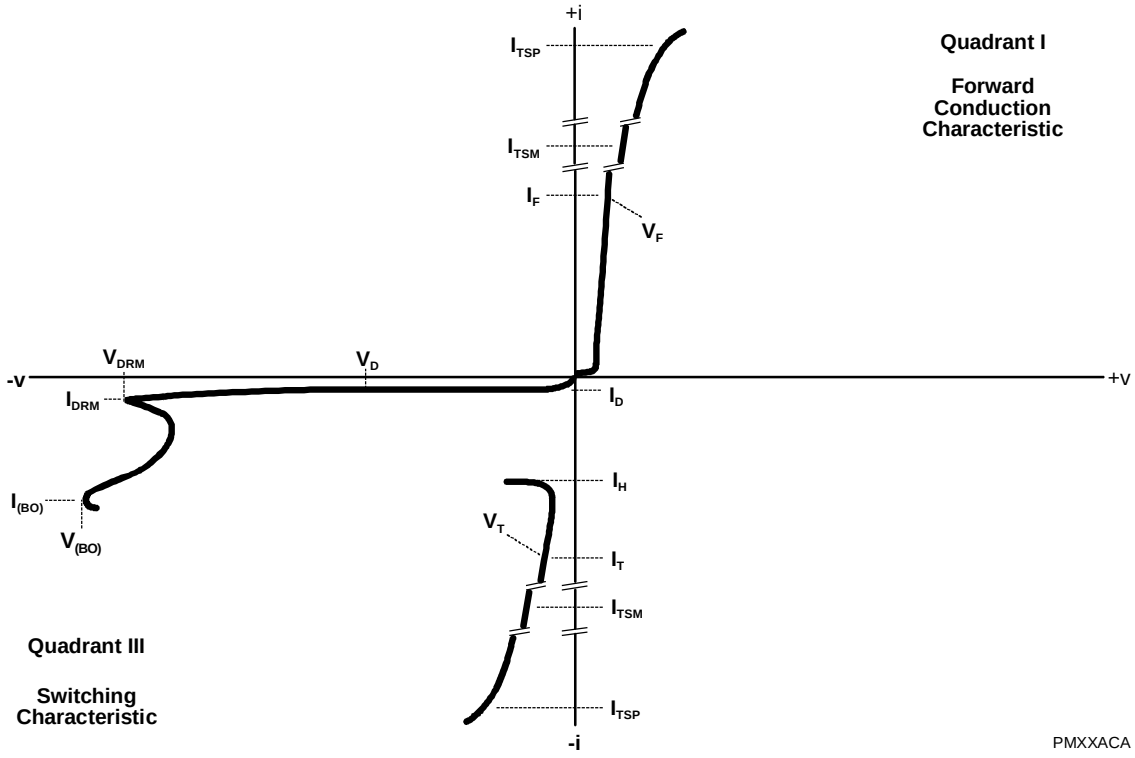


Figure 1. VOLTAGE-CURRENT CHARACTERISTIC FOR TERMINAL PAIR
ALL MEASUREMENTS ARE REFERENCED TO TERMINAL 1

TYPICAL CHARACTERISTICS

OFF-STATE CURRENT vs JUNCTION TEMPERATURE

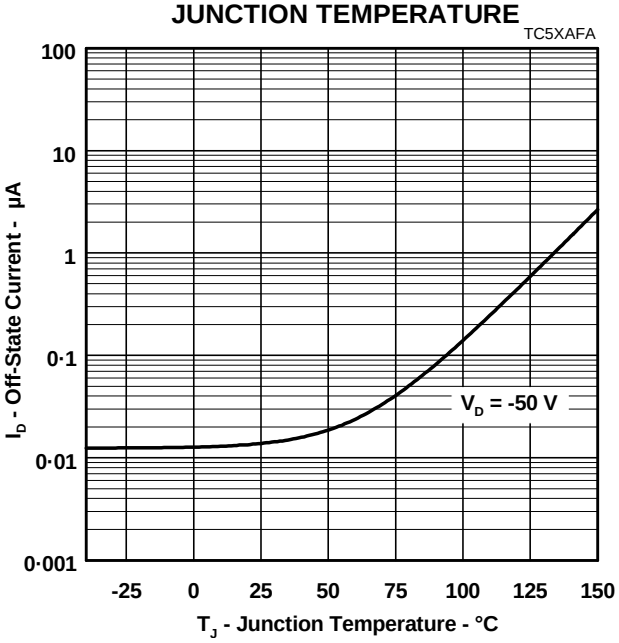


Figure 2.

NORMALISED BREAKOVER VOLTAGE vs JUNCTION TEMPERATURE

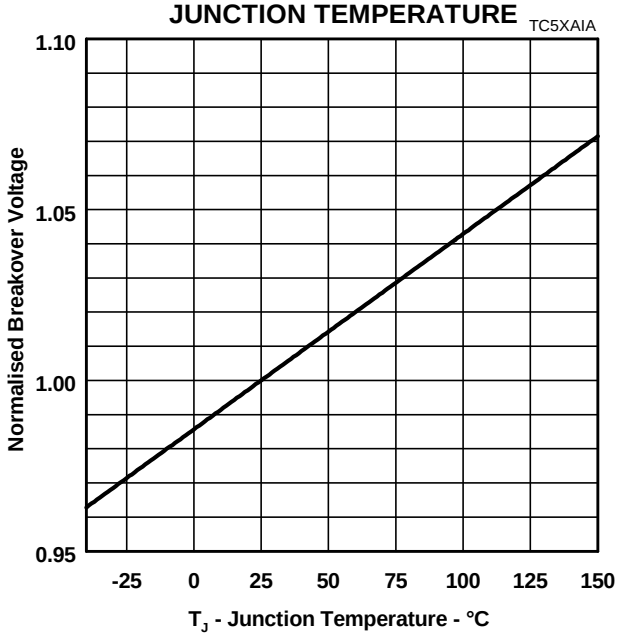


Figure 3.

ON-STATE AND FORWARD CURRENTS vs ON-STATE AND FORWARD VOLTAGES

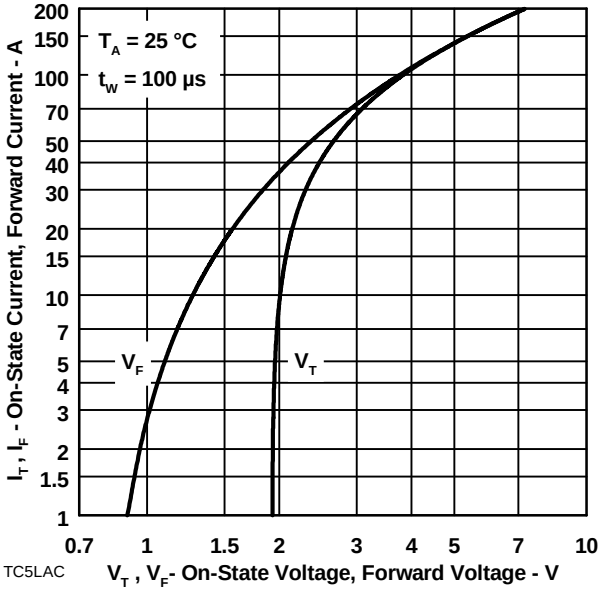


Figure 4.

NORMALISED HOLDING CURRENT vs JUNCTION TEMPERATURE

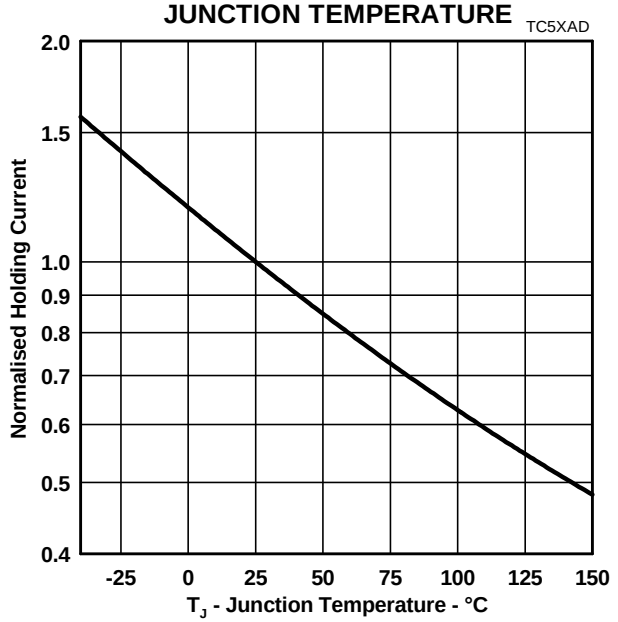


Figure 5.

TYPICAL CHARACTERISTICS

OFF-STATE CAPACITANCE
vs
OFF-STATE VOLTAGE

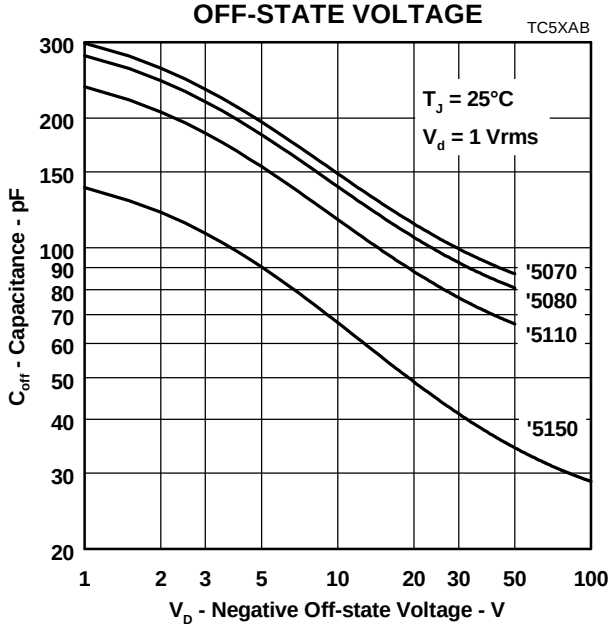


Figure 6.

DIFFERENTIAL OFF-STATE CAPACITANCE
vs
RATED REPETITIVE PEAK OFF-STATE VOLTAGE

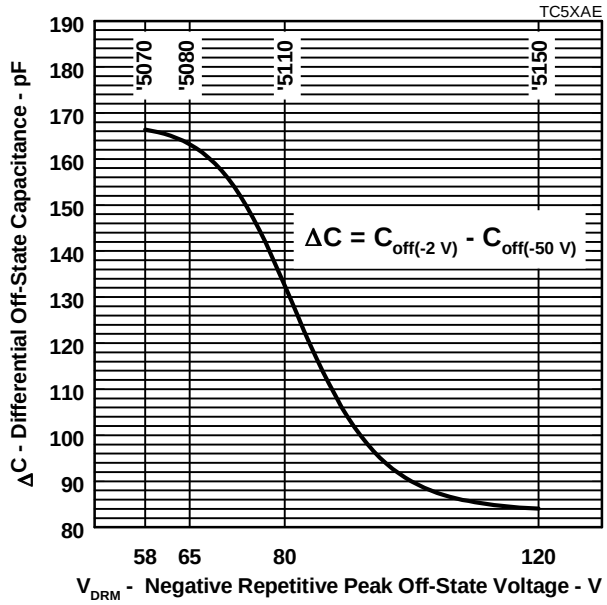


Figure 7.

RATING AND THERMAL INFORMATION

NON-REPETITIVE PEAK ON-STATE CURRENT
vs
CURRENT DURATION

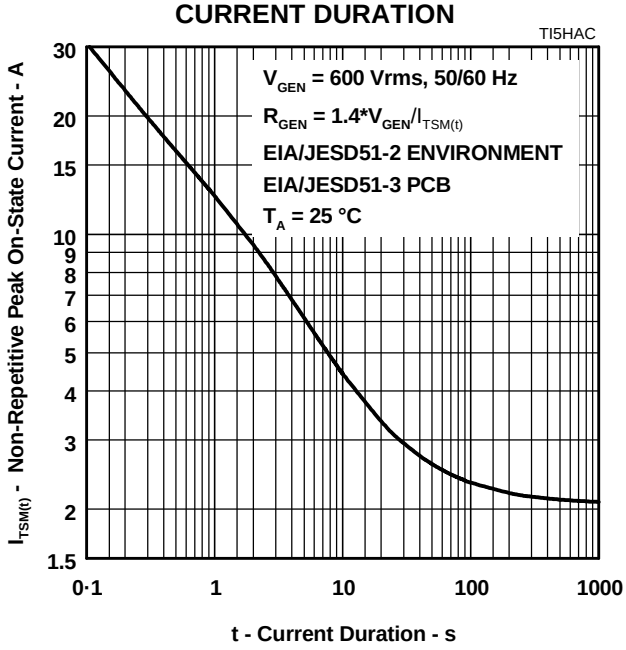


Figure 8.

V_{DRM} DERATING FACTOR
vs
MINIMUM AMBIENT TEMPERATURE

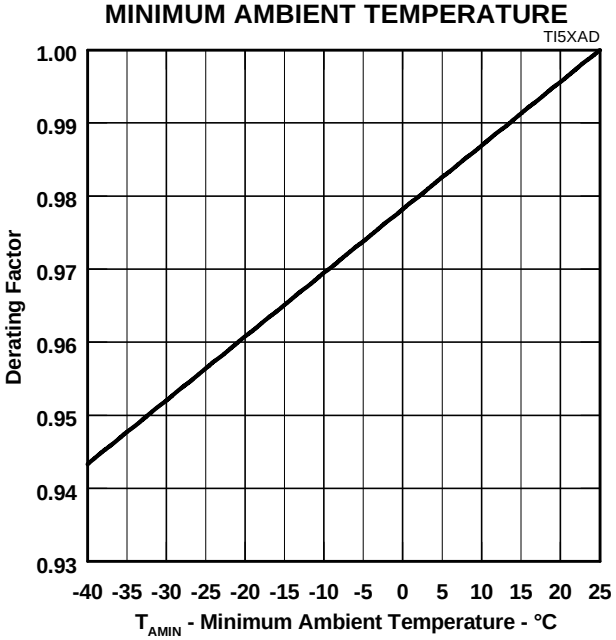


Figure 9.

IMPULSE RATING
vs
AMBIENT TEMPERATURE

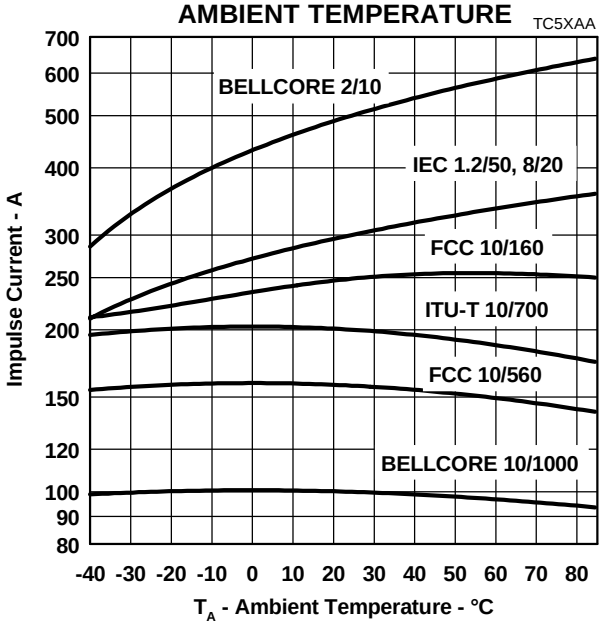


Figure 10.

APPLICATIONS INFORMATION

deployment

These devices are two terminal overvoltage protectors. They may be used either singly to limit the voltage between two points (Figure 11) or in multiples to limit the voltage at several points in a circuit (Figure 12).

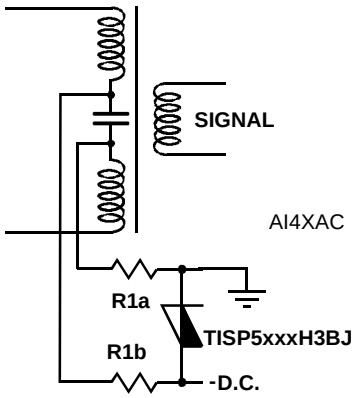


Figure 11. POWER SUPPLY PROTECTION

In Figure 11, the TISP5xxxH3BJ limits the maximum voltage of the negative supply to $-V_{(BO)}$ and $+V_F$. This configuration can be used for protecting circuits where the voltage polarity does not reverse in normal operation. In Figure 12, the two TISP5xxxH3BJ protectors, Th4 and Th5, limit the maximum voltage of the SLIC (Subscriber Line Interface Circuit) outputs to $-V_{(BO)}$ and $+V_F$. Ring and test protection is given by protectors Th1, Th2 and Th3. Protectors Th1 and Th2 limit the maximum tip and ring wire voltages to the $\pm V_{(BO)}$ of the individual protector. Protector Th3 limits the maximum voltage between the two conductors to its $\pm V_{(BO)}$ value. If the equipment being protected has all its vulnerable components connected between the conductors and ground, then protector Th3 is not required.

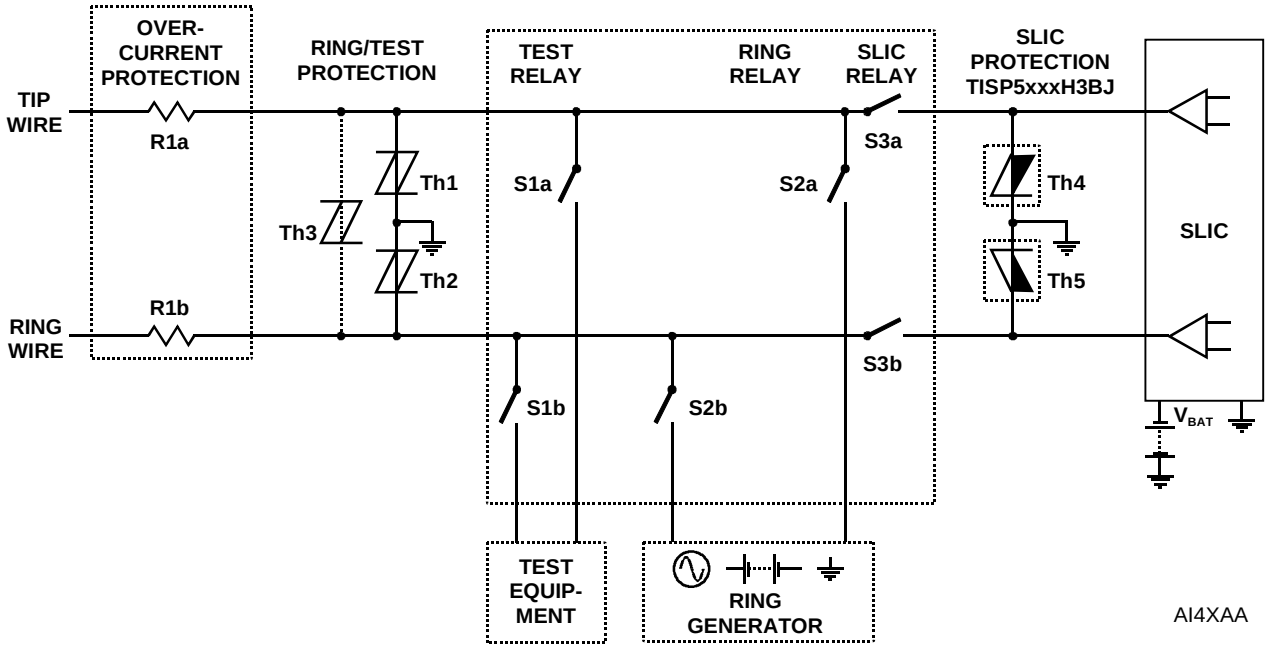


Figure 12. LINE CARD SLIC PROTECTION

broad-band protection.

The star-connection of three TISP5xxxH3BJ protectors gives a protection circuit which has a low differential capacitance to ground (Figure 13). This example, a -100 V ISDN line is protected. In Figure 13, the circuit illustration A shows that protector Th1 will be forward biased as it is connected to the most negative potential. The other two protectors, Th2 and Th3 will be reverse biased as protector Th1 will pull their common connection to within 0.5 V of the negative voltage supply.

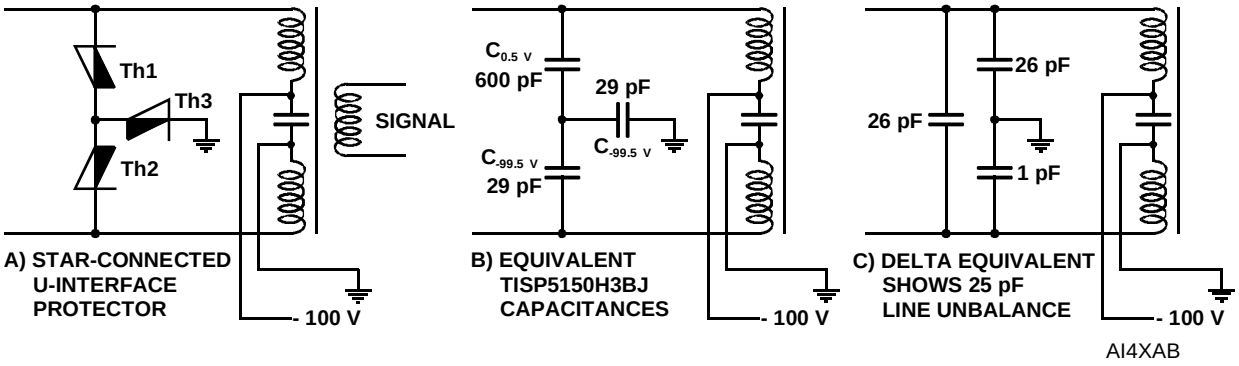


Figure 13. ISDN LOW CAPACITANCE U-INTERFACE PROTECTION

Illustration B shows the equivalent capacitances of the two reverse biased protectors (Th2 and Th3) as 29 pF each and the capacitance of the forward biased protector (Th1) as 600 pF. Illustration C shows the delta equivalent of the star capacitances of illustration B. The protector circuit differential capacitance will be 26 - 1 = 25 pF. In this circuit, the differential capacitance value cannot exceed the capacitance value of the ground protector (Th3).

A bridge circuit can be used for low capacitance differential. Whatever the potential of the ring and tip conductors are in Figure 14, the array of steering diodes, D1 through to D6, ensure that terminal 1 of protector Th1 is always positive with respect to terminal 2. The protection voltage will be the sum of the protector Th1, $V_{(BO)}$, and the forward voltage of the appropriate series diodes. It is important to select the correct diodes. Diodes D3 through to D6 divert the currents from the ring and tip lines. Diodes D1 and D2 will carry the sum of the ring and tip currents and so conduct twice the current of the other four diodes. The diodes need to be specified for forward recovery voltage, V_{FRM}, under the expected impulse conditions. (Some conventional a.c. rectifiers can produce as much as 70 V of forward recovery voltage, which would be an extra 140 V added to the $V_{(BO)}$ of Th1). In principle the bridge circuit can be extended to protect more than two conductors by adding extra legs to the bridge.

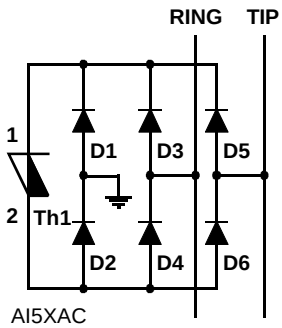


Figure 14. LOW CAPACITANCE BRIDGE PROTECTION CIRCUIT

ISDN device selection

The ETSI Technical Report ETR 080:1993 defines several range values in terms of maximum and minimum ISDN feeding voltages. The following table shows that ranges 1 and 2 can use a TISP5110H3BJ protector and ranges 3 to 5 can use a TISP5150H3BJ protector.

RANGE	FEEDING VOLTAGE MINIMUM V	FEEDING VOLTAGE MAXIMUM V	STANDOFF VOLTAGE V_{DRM} V	DEVICE #
1	51	69	-80	TISP5110H3BJ
2	66	70		
3	91	99	-120	TISP5150H3BJ
4	90	110		
5	105	115		

impulse testing

To verify the withstand capability and safety of the equipment, standards require that the equipment is tested with various impulse wave forms. The table below shows some common values.

STANDARD	PEAK VOLTAGE SETTING V	VOLTAGE WAVE FORM µs	PEAK CURRENT VALUE A	CURRENT WAVE FORM µs	TISP5xxxH3 25 °C RATING A	SERIES RESISTANCE Ω
GR-1089-CORE	2500	2/10	500	2/10	500	0
	1000	10/1000	100	10/1000	100	
FCC Part 68 (March 1998)	1500	10/160	200	10/160	250	0
	800	10/560	100	10/560	160	0
	1500	9/720 †	37.5	5/320 †	200	0
	1000	9/720 †	25	5/320 †	200	0
I3124	1500	0.5/700	37.5	0.2/310	200	0
ITU-T K20/K21	1500 4000	10/700	37.5 100	5/310	200	0

† FCC Part 68 terminology for the waveforms produced by the ITU-T recommendation K21 10/700 impulse generator

If the impulse generator current exceeds the protectors current rating then a series resistance can be used to reduce the current to the protectors rated value and so prevent possible failure. The required value of series resistance for a given waveform is given by the following calculations. First, the minimum total circuit impedance is found by dividing the impulse generators peak voltage by the protectors rated current. The impulse generators fictive impedance (generators peak voltage divided by peak short circuit current) is then subtracted from the minimum total circuit impedance to give the required value of series resistance. In some cases the equipment will require verification over a temperature range. By using the rated waveform values from Figure 10, the appropriate series resistor value can be calculated for ambient temperatures in the range of -40 °C to 85 °C.

If the devices are used in a star-connection, then the ground return protector, Th3 in Figure 13, will conduct the combined current of protectors Th1 and Th2. Similarly in the bridge connection (Figure 14), the protector Th1 must be rated for the sum of the conductor currents. In these cases, it may be necessary to include some series resistance in the conductor feed to reduce the impulse current to within the protectors ratings.

a.c. power testing

The protector can withstand currents applied for times not exceeding those shown in Figure 8. Currents that exceed these times must be terminated or reduced to avoid protector failure. Fuses, PTC (Positive Temperature Coefficient) resistors and fusible resistors are overcurrent protection devices which can be used

to reduce the current flow. Protective fuses may range from a few hundred milliamperes to one ampere. In some cases it may be necessary to add some extra series resistance to prevent the fuse opening during impulse testing. The current versus time characteristic of the overcurrent protector must be below the line shown in Figure 8. In some cases there may be a further time limit imposed by the test standard (e.g. UL 1459 wiring simulator failure).

capacitance

The protector characteristic off-state capacitance values are given for d.c. bias voltage, V_D, values of -1 V, -2 V and -50 V. The TISP5150H3BJ is also given for a bias of -100 V. Values for other voltages may be determined from Figure 6. Up to 10 MHz the capacitance is essentially independent of frequency. Above 10 MHz the effective capacitance is strongly dependent on connection inductance. In Figure 12, the typical conductor bias voltages will be about -2 V and -50 V. Figure 7 shows the differential (line unbalance) capacitance caused by biasing one protector at -2 V and the other at -50 V. For example, the TISP5070H3BJ has a differential capacitance value of 166 pF under these conditions.

normal system voltage levels

The protector should not clip or limit the voltages that occur in normal system operation. Figure 9 allows the calculation of the protector V_{DRM} value at temperatures below 25 °C. The calculated value should not be less than the maximum normal system voltages. The TISP5150H3BJ, with a V_{DRM} of -120 V, can be used to protect ISDN feed voltages having maximum values of -99 V, -110 V and -115 V (range 3 through to range 5). These three range voltages represent 0.83 (99/120), 0.92 (110/120) and 0.96 (115/120) of the -120 V TISP5150H3BJ V_{DRM}. Figure 9 shows that the V_{DRM} will have decreased to 0.944 of its 25 °C value at -40 °C. Thus the supply feed voltages of -99 V (0.83) and -110 V (0.92) will not be clipped at temperatures down to -40 °C. The -115 V (0.96) feed supply may be clipped if the ambient temperature falls below -21 °C.

JESD51 thermal measurement method

To standardise thermal measurements, the EIA (Electronic Industries Alliance) has created the JESD51 standard. Part 2 of the standard (JESD51-2, 1995) describes the test environment. This is a 0.0283 m^3 (1 ft^3) cube which contains the test PCB (Printed Circuit Board) horizontally mounted at the centre. Part 3 of the standard (JESD51-3, 1996) defines two test PCBs for surface mount components; one for packages smaller than 27 mm on a side and the other for packages up to 48 mm. The SMBJ measurements used the smaller 76.2 mm x 114.3 mm (3.0 “ x 4.5 “) PCB. The JESD51-3 PCBs are designed to have low effective thermal conductivity (high thermal resistance) and represent a worse case condition. The PCBs used in the majority of applications will achieve lower values of thermal resistance and so can dissipate higher power levels than indicated by the JESD51 values.

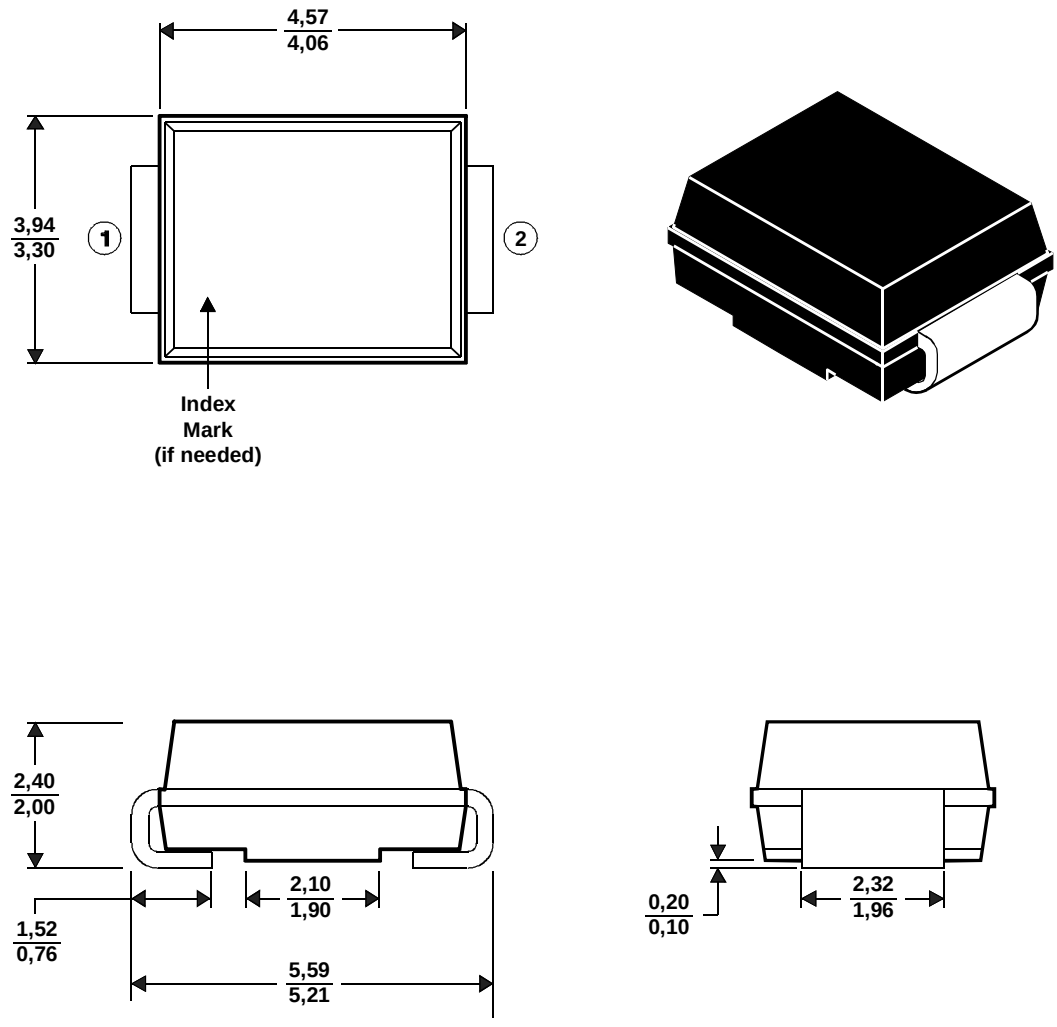
MECHANICAL DATA

SMBJ (DO-214AA)

plastic surface mount diode package

This surface mount package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

SMB



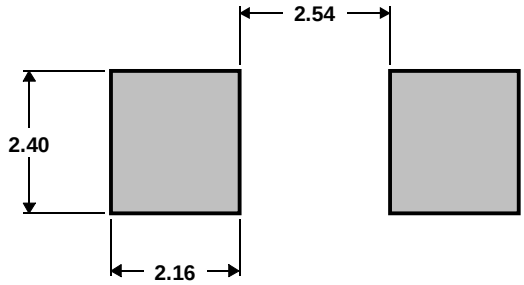
ALL LINEAR DIMENSIONS IN MILLIMETERS

MDXXBHA

MECHANICAL DATA

recommended printed wiring footprint.

SMB Pad Size



ALL LINEAR DIMENSIONS IN MILLIMETERS

MDXXBI

device symbolization code

Devices will be coded as below. Terminal 1 is identified by a bar index mark.

DEVICE	SYMOBLIZATION CODE
TISP5070H3BJ	5070H3
TISP5080H3BJ	5080H3
TISP5110H3BJ	5110H3
TISP5150H3BJ	5150H3

carrier information

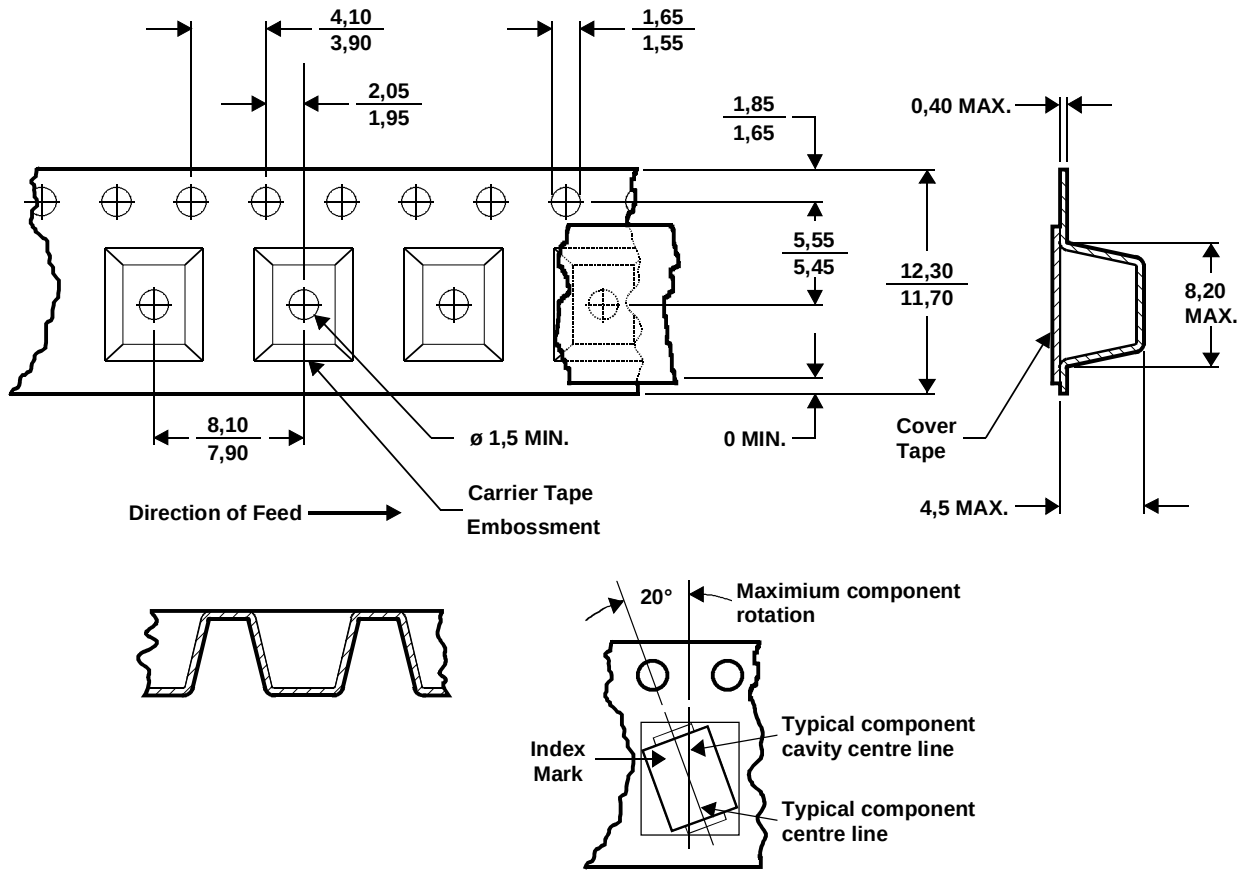
The carrier for production quantities is embossed tape reel pack. Evaluation quantities will be shipped in the most practical carrier.

CARRIER	ORDER #
Embossed Tape Reel Pack (3000 Devices are on a Reel)	TISP5xxxH3BJR

MECHANICAL DATA

tape dimensions

SMB Package Single-Sprocket Tape



ALL LINEAR DIMENSIONS IN MILLIMETERS

NOTES: A. The clearance between the component and the cavity must be within 0,05 mm MIN. to 0,65 mm MAX. so that the component cannot rotate more than 20° within the determined cavity. MDXXBJ

B. Taped devices are supplied on a reel of the following dimensions:-

Reel diameter:	330 ±3,0 mm
Reel hub diameter	75 mm MIN.
Reel axial hole:	13,0 ±0,5 mm

C. 3000 devices are on a reel.

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