1-W High-Voltage Switchmode Regulator

FEATURES

- CCITT Compatible
- Current-Mode Control
- Low Power Consumption (less than 5 mW)
- 10- to 120-V Input Range
- 200-V, 250-mA MOSFET
- Internal Start-Up Circuit
- $\overline{\text{SHUTDOWN}}$ and RESET
- Maximum Duty Cycle of 99.9%

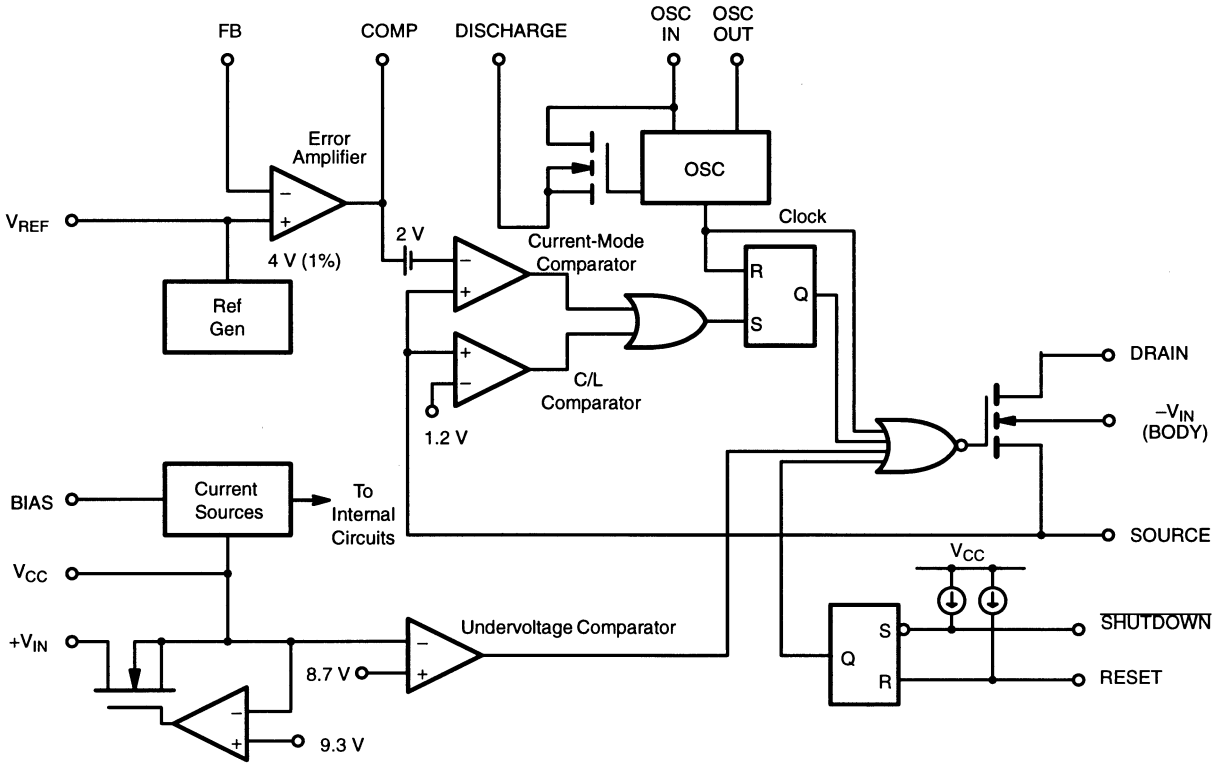
DESCRIPTION

The Si9108 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc/dc converter in ISDN terminals up to 3 watts. A 0.5-mA max supply current makes possible the design of a dc/dc converter with 60% efficiency at 25 mW, therefore meeting the recommended performance under the CCITT I.430 specifications.

This device may be used with an appropriate transformer to implement isolated flyback power converter topologies to provide single or multiple regulated dc outputs (i.e., ±5 V).

The Si9108 is available in 16-pin wide-body SOIC, 14-pin plastic DIP, and 20-pin PLCC packages, and is specified over the industrial, D suffix (-40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)

V_{CC} . . . . . 15 V
$+V_{IN}$ . . . . . 120 V
V_{DS} . . . . . 200 V
I_D (Peak) (300 µs pulse, 2% duty cycle) . . . . . 2 A
I_D (rms) . . . . . 250 mA
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) . . -0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SOURCE) . . . . . -0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) . . . . . 5 mA
Storage Temperature . . . . . -65 to 125°C
Operating Temperature . . . . . -40 to 85°C
Junction Temperature (T_J) . . . . . 150°C

Power Dissipation (Package)[a]
14-Pin Plastic DIP (J Suffix)[b] . . . . . 750 mW
16-Pin Plastic Wide-Body SOIC (W Suffix)[c] . . . . . 900 mW
20-Pin PLCC (N Suffix)[d] . . . . . 1400 mW

Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP . . . . . 167°C/W
16-Pin Plastic Wide-Body SOIC . . . . . 140°C/W
20-Pin PLCC . . . . . 90°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C
c. Derate 7.2 mW/°C above 25°C
d. Derate 11.2 mW/°C above 25°C

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$

V_{CC} . . . . . 10 V to 13.5 V
$+V_{IN}$ . . . . . 10 V to 120 V
f_{OSC} . . . . . 40 kHz to 1 MHz
R_{OSC} . . . . . 25 kΩ to 1 MΩ
Linear Inputs . . . . . 0 to V_{CC} - 3 V
Digital Inputs . . . . . 0 to V_{CC}

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 820 kΩ, R_{OSC} = 910 kΩ	Limits D-Suffix, -40°C to 85°C Temp[b]	Min[c]	Typ[d]	Max[c]	Unit
Reference							
Output Voltage	V_R	OSC IN = V_{IN} (OSC Disabled), R_L = 10 MΩ	Room	3.92	4.00	4.08	V
Output Impedance[e]	Z_{OUT}	OSC IN = $-V_{IN}$	Room	15	300	45	kΩ
Short Circuit Current	I_{SREF}	OSC IN = - V_{IN}, V_{REF} = $-V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}	OSC IN = $-V_{IN}$	Full		0.25	1.0	mV/°C
Long Term Stability[e]		t = 1000 hrs, T_A = 125°C	Room		5.00	25.00	mV
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	See Note e	Room	32	40	48	kHz
Voltage Stability	Δf/f	Δf/f = f (13.5 V) - f (9.5 V)/f (9.5 V)	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP, OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.96	4	4.04	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V	Room		25	500	nA
Open Loop Voltage Gain[e]	A_{VOL}	OSC IN = $-V_{IN}$ (OSC Disabled)	Room	60	80		dB
Input Offset Voltage	V_{OS}	OSC IN = $-V_{IN}$	Room		±15	±40	mV
Unity Gain Bandwidth[e]	BW		Room	0.5	0.8		MHz
Dynamic Output Impedance	Z_{OUT}		Room		1		kΩ
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	Room		-1.2	-0.32	mA
		Sink (V_{FB} = 4.5 V)	Room	0.05	0.08		
Power Supply Rejection	PSRR	10 V ≤ V_{CC} ≤ 13.5 V	Room		70		dB

SPECIFICATIONS[a]

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PWM							
Maximum Duty Cycle	D_{MAX}		Room	99.0	99.6	99.9	%
Dead Time			Room		100		ns
Minimum Duty Cycle	D_{MIN}		Room			0	%
Minimum Pulse Width Before Pulse Drops Out			Room		110	175	ns
Current Limit							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V	Room	0.8	1.0	1.2	V
Delay to Output[e]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	Room		200	300	ns
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	Room	120			V
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq$ 10 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = 7 V	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.5	9.3	9.7	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	Room	7.0	8.7	9.2	
V_{REG} - V_{UVLO}	V_{DELTA}		Room	0.25	0.5		
Supply							
Supply Current	I_{CC}		Room		0.35	0.5	mA
Bias Current	I_{BIAS}		Room		7.5		µA
$\overline{\text{SHUTDOWN}}$ Delay	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width	t_{RW}		Room	50			
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET Low	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	-35	-25		

SPECIFICATIONS[a]							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 820 kΩ, R_{OSC} = 910 kΩ	**Limits** D-Suffix, -40°C to 85°C **Temp**[b]	**Min**[c]	**Typ**[d]	**Max**[c]	**Unit**
MOSFET Switch							
Breakdown Voltage	$V_{(BR)DSS}$	I_{DRAIN} = 100 µA	Full	200	220		V
Drain-Source On Resistance[g]	$r_{DS(on)}$	I_{DRAIN} = 100 mA	Room		5	7	W
Drain Off Leakage Current	I_{DSS}	V_{DRAIN} = 100 V	Room			10	µA
Drain Capacitance	C_{DS}		Room		35		pF

Notes

a. Refer to PROCESS OPTION FLOWCHART for additional information.

b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

e. Guaranteed by design, not subject to production test.

f. C_{STRAY} Pin 8 = ≤ 5 pF

g. Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.

TIMING WAVEFORMS

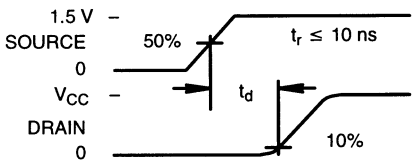


FIGURE 1.

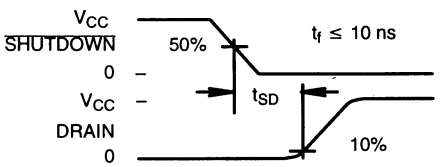


FIGURE 2.

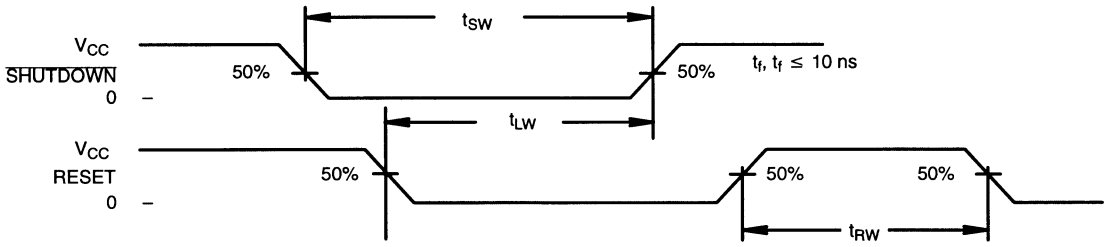


FIGURE 3.

TYPICAL CHARACTERISTICS

Output Switching Frequency vs. Oscillator Resistance

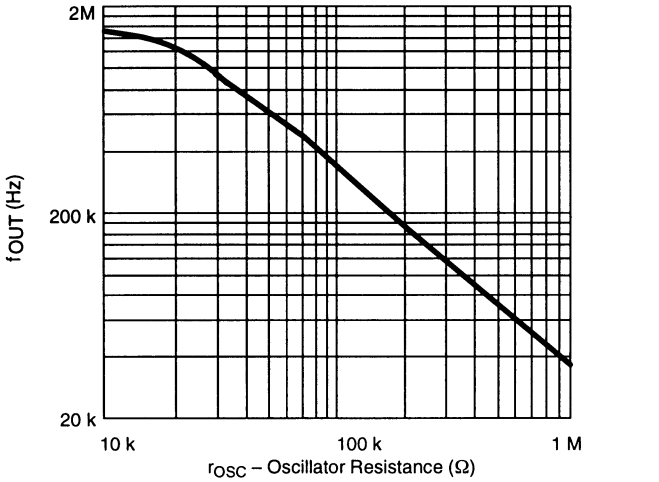
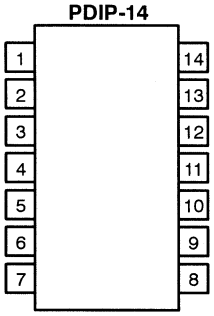


FIGURE 4.

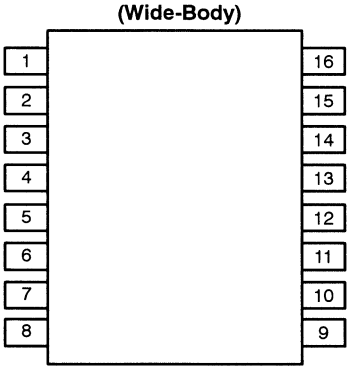
PIN CONFIGURATIONS

PDIP-14



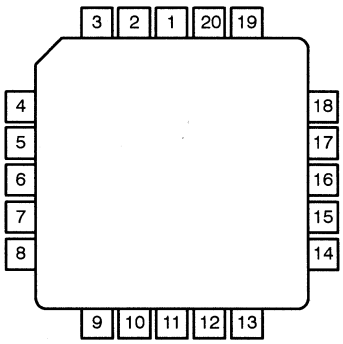
Top View
Order Number: Si9108DJ02

SO-16 (Wide-Body)



Top View
Order Number: Si9108DW

PLCC-20



Top View
Order Number: Si9108DN02

PIN DESCRIPTION

Function	Pin Number		
	14-Pin Plastic DIP	16-Pin SOIC	20-Pin PLCC
SOURCE	4	1	7
$-V_{IN}$	5	2	8
V_{CC}	6	4	9
OSC_{OUT}	7	5	10
OSC_{IN}	8	6	11
DISCHARGE	9	7	12
V_{REF}	10	8	14
$\overline{SHUTDOWN}$	11	9	16
RESET	12	10	17
COMP	13	11	18
FB	14	12	20
BIAS	1	13	2
$+V_{IN}$	2	14	3
DRAIN	3	16	5
NC		3, 15	1, 4, 6, 13, 15, 19