Data Sheet July 1999 File Number 2876.2

4A, 50V and 60V, 0.800 Ohm, Logic Level, N-Channel Power MOSFETs

The RFP4N05L and RFP4N06L are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09520.

Ordering Information

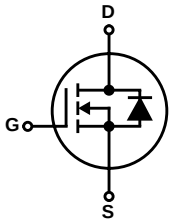
PART NUMBER	PACKAGE	BRAND
RFP4N05L	TO-220AB	RFP4N05L
RFP4N06L	TO-220AB	RFP4N06L

NOTE: When ordering, include the entire part number.

Features

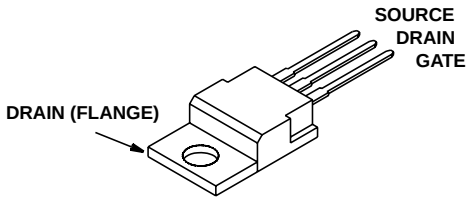
- 4A, 50V and 60V
- $r_{DS(ON)} = 0.800\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEL TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFP4N05L	RFP4N06L	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	50	60	V
Drain to Gate Voltage R_{GS} = 20KΩ (Note 1)	V_{DGR}	50	60	V
Gate to Source Voltage	V_{GS}	±10	±10	V
Drain Current, RMS Continuous	I_D	4	4	A
Pulsed (Note 3)	I_{DM}	10	10	A
Power Dissipation Total at $T_C = 25^oC$	P_D	25	25	W
Derating Above $T_C = 25^oC$		0.2	0.2	W/ ^oC
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering				
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V				
RFP4N05L			50	-	-	V
RFP4N06L			60	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA	1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}	-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, $T_C = 125^oC$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	-	-	±100	nA
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	I_D = 4A, V_{GS} = 5V	-	-	3.2	V
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 4A, V_{GS} = 5V, (Figures 6, 7)	-	-	0.800	Ω
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx$ 4A, V_{DD} = 30V, R_G = 6.25Ω, R_L = 7.5Ω, V_{GS} = 5V (Figures 10, 11, 12)	-	10	20	ns
Rise Time	t_r		-	65	130	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	20	40	ns
Fall Time	t_f		-	30	60	ns
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz (Figure 9)	-	-	225	pF
Output Capacitance	C_{OSS}		-	-	100	pF
Reverse-Transfer Capacitance	C_{RSS}		-	-	40	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	5	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 1A	-	-	1.4	V
Reverse Recovery Time	t_{rr}	I_{SD} = 2A, dI_{SD}/dt = 100A/μs	-	150	-	ns

NOTES:

2. Pulsed: pulse duration = 300μs max, duty cycle = 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

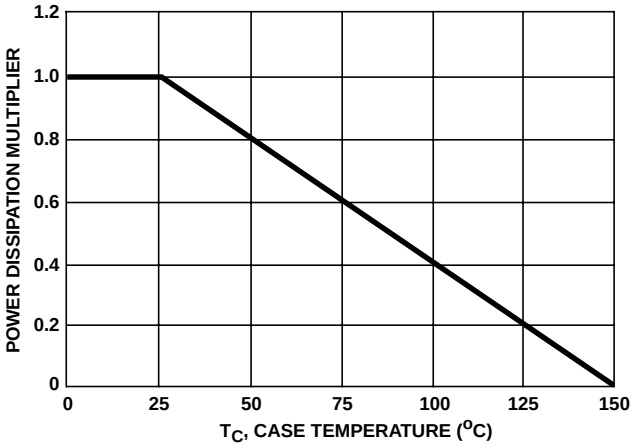


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

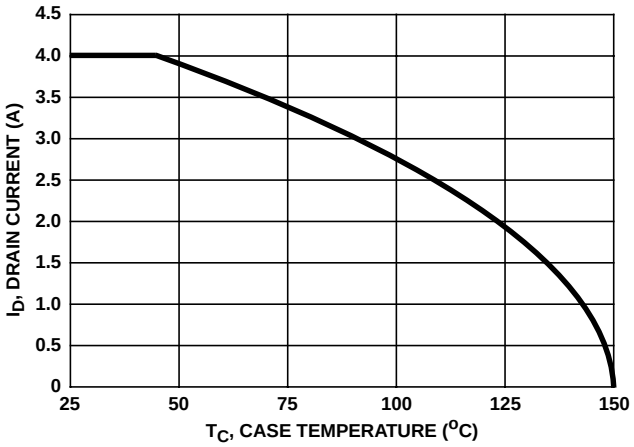


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

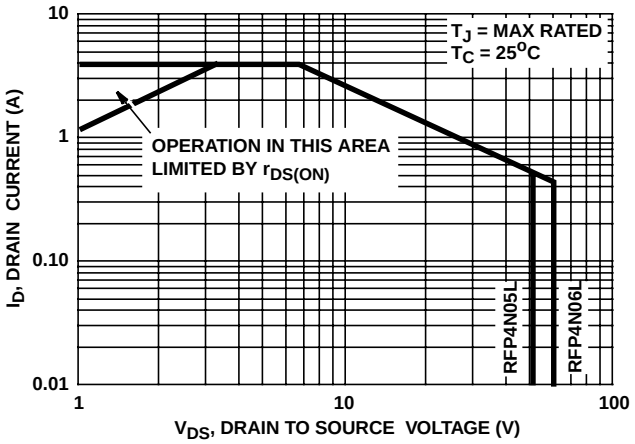


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

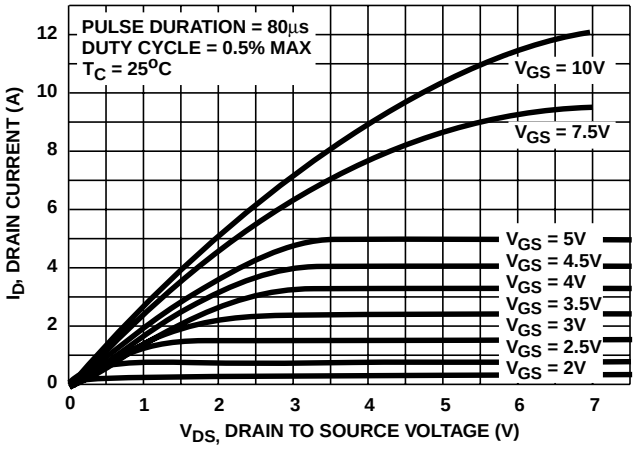


FIGURE 4. SATURATION CHARACTERISTICS

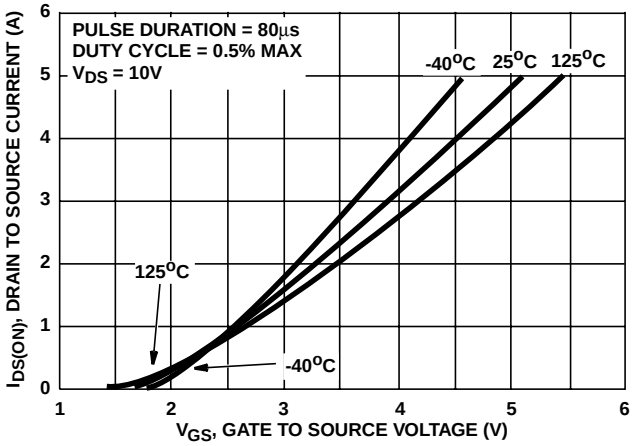


FIGURE 5. TRANSFER CHARACTERISTICS

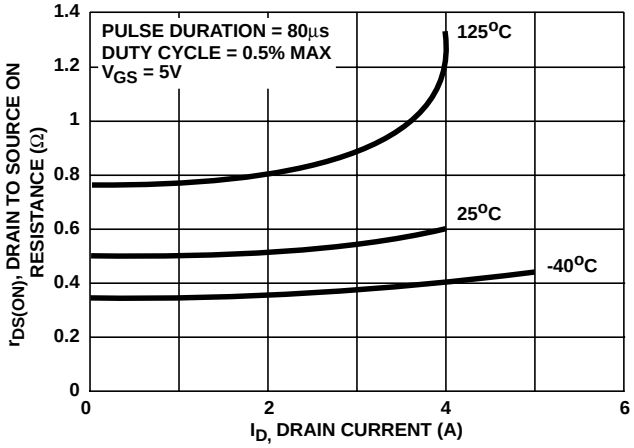


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

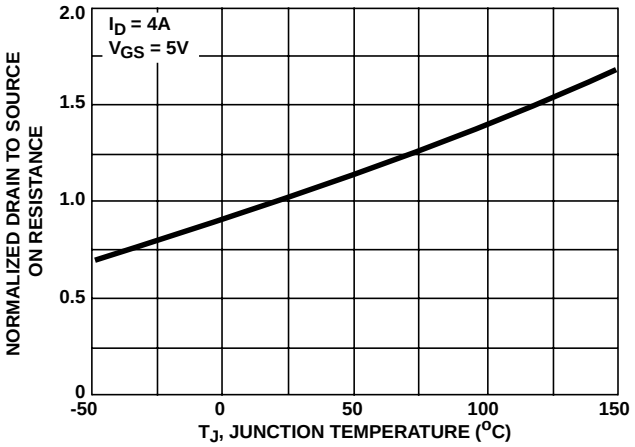


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

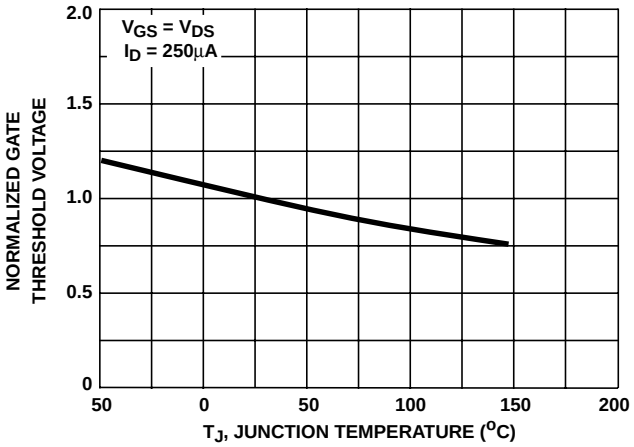


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

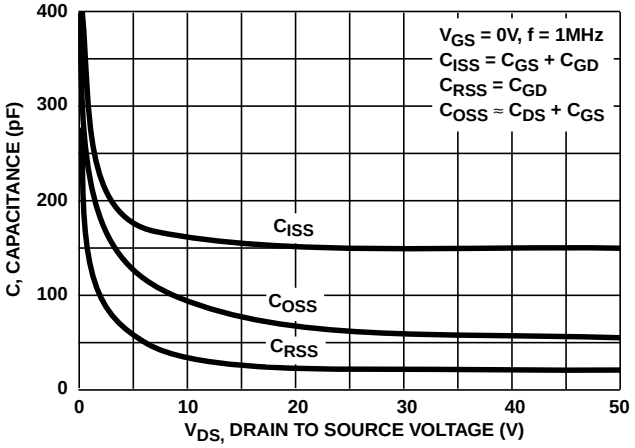
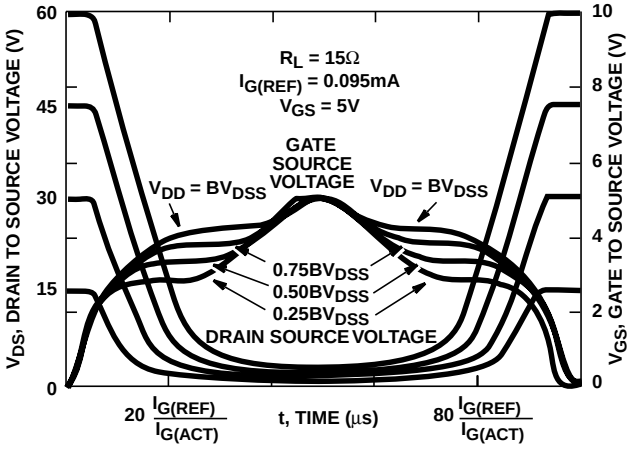


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

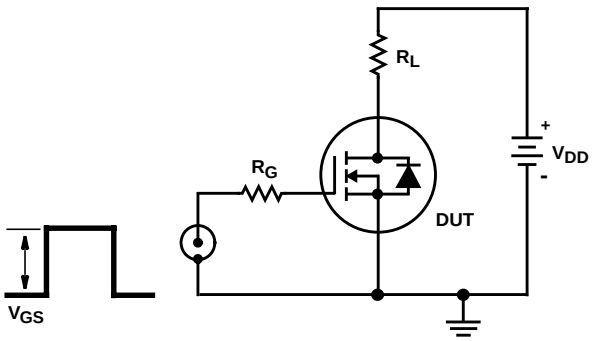


FIGURE 11. SWITCHING TIME TEST CIRCUIT

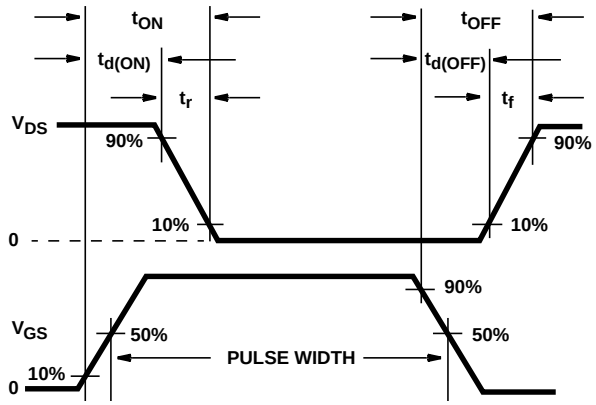


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

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