PM8313

D3MX

ANSWERS TO FREQUENTLY ASKED QUESTIONS REGARDING THE D3MX

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CONTENTS

REFERENCES

- ANSI T1.107 (1995), "Digital Hierarchy — Formats Specifications"

- ITU-T Recommendation G.703, Blue Book Vol. III, Fascicle III.4 (November 1988), "Physical/Electrical Characteristics of Hierarchical Digital Interfaces"

- ITU-T Recommendation G.704, Blue Book Vol. III, Fascicle III.4 (November 1988), "Synchronous Frame Structures Used at Primary and Secondary Hierarchical Levels"

- ITU-T Recommendation G.743, Blue Book Vo. III, Fascicle III.4 (November 1988), "Second Order Digital Multiplex Equipment Operating at 6312 kbit/s and Using Positive Justification"

- ITU-T Recommendation G.747, Blue Book Vo. III, Fascicle III.4 (November 1988), "Second Order Digital Multiplex Equipment Operating at 6312 kbit/s and Multiplexing Three Tributaries at 2048 kbit/s"

- ITU-T Recommendation G.824 (03/93), "Digital Networks — The Control of Jitter and Wander Within Digital Networks Which are Based on the 1544 kbit/s Hierarchy"

- ITU-T Recommendation I.363 (03/93), "B-ISDN ATM Adaptation Layer Specification"

- PMC-Sierra, PMC-920702S4, July 1994, Data Book for PM8313 D3MX M13 Multiplexer.

DEFINITIONS AND TERM GLOSSARY

AAL1   ATM Adaptation Layer, Type 1. This term is used for a standardized (ITU-T I.363) ATM Adaptation Layer structure used for constant bit rate applications such as circuit emulation.

AIS   Alarm Indication Signal. AIS is transmitted when there is no good data to transmit (due to an upstream failure), and is useful for maintaining a timing reference to downstream equipment. For DS1, DS2, and E1 formats, AIS consists of a all-ones serial digital data. For DS3 format, AIS consists of a framed 1010... pattern. The D3MX can detect and generate DS3 and DS2 AIS and can also propagate DS2 and DS1 AIS.

AMI   Alternate Mark Inversion. This is a ternary coding scheme for electrical transmission of digital data. Each binary one that is transmitted is represented by a RZ pulse which is of opposite polarity of the preceding pulse. Each binary zero that is transmitted is represented by a space (no pulse).

ANSI   American National Standards Institute. This is a non-profit, non-government federation of standards-making and standards-using organizations. It publishes standards, but does not develop them. Compliance with an American National Standard is voluntary and does not preclude anyone from manufacturing, marketing, purchasing, or using products, processes, or procedures not conforming to the standards.

ATM   Asynchronous Transfer Mode. This is a cell-based transmission scheme defined for the user-network interface of a Broadband ISDN network. An ATM cell consists of 5 bytes of overhead and 48 bytes of payload. There are standardized mappings of ATM cells into most common transport formats.

C-Bit Parity C-Bit Parity Format. This is a standardized (ANSI T1.107) format for DS3 channelized signals.

CRC   Cyclic Redundancy Check. This is a scheme for error monitoring by making a Boolean cyclic polynomial calculation over a digital data payload. The transmitter transmits the results of this calculation, and the receiver compares this to it's own calculation. If there is a difference, it is assumed that one or more bits have been corrupted during transmission of the digital payload. In C-Bit Parity applications, the FCS of the LAPD packets transmitted on the data link is a CRC.

D3MX   M13 Multiplexer. This is PMC-Sierra's mnemonic for the PM8313 M13 Multiplexer device.

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DS1	Digital Signal, Level 1. This term refers to a standardized (ANSI T1.107) format for transmitting serial digital data at 1544 kbit/s.
DS2	Digital Signal, Level 2. This term refers to a standardized (ANSI T1.107) format for transmitting serial digital data at 6312 kbit/s.
DS3	Digital Signal, Level 3. This term refers to a standardized (ANSI T1.107) format for transmitting serial digital data at 44736 kbit/s.
E1	European Transmission Format, Level 1. This term refers to a standardized (ITU-T G.704) format for transmitting serial digital data at 2048 kbit/s.
E1XC	E1 Framer/Transceiver. This is PMC-Sierra's mnemonic label for the PM6341 E1 framer/transceiver device. This is a fully integrated framer suitable for processing the E1 tributaries multiplexed/demultiplexed by the D3MX.
EQUAD	E1 Quad Framer. This is PMC-Sierra's mnemonic label for the PM6344 Quad E1 framer device. This is a fully integrated quad framer suitable for processing the E1 tributaries multiplexed/demultiplexed by the D3MX.
FEAC	Far-End Alarm and Control. This term is applied to channels in a transmitted data stream which are reserved for carrying alarm and control information to and from the far-end equipment.
FEBE	Far-End Block Error. This is a signal indicating that the far-end equipment found at least one bit error in a block of data (typically a frame).
FERF	Far-End Receive Failure. This is a signal indicating that the far-end equipment cannot find frame alignment in its received serial stream.
FCS	Frame Check Sequence. This is a CRC calculation performed at the end of a LAPD packet to check for bit errors.
FIFO	First-In First-Out buffer. This term refers to a digital buffer which outputs data in the same order as it was input.
FRMR	Framer. This term is PMC-Sierra's mnemonic label for the DS2 and DS3 frame aligner functional blocks within the D3MX.
HDB3	High Density Bipolar of Order 3. This is a statndardized (ITU-T G.703) zeros suppression scheme which replaces four consecutive zeros with a decodeable sequence of LCVs. Zero suppression is important to ensure proper operation of clock recovery circuits.

HDLC   High-Level Data Link Control. This is a packet-based serial communications protocol which consists of flag-delimited packets. These packets use a CRC-16 FCS for bit error monitoring.

ISDN   Integrated Services Digital Network. This is a world-wide public telecommunications network that is implemented as a set of digital switches and paths supporting a broad range of services.

ITU-T   International Telecommunication Union - Telephony. This is a committee within a United Nations treaty organization. The charter is "to study and issue recommendations on technical, operating, and tariff questions relating to telegraphy and telephony." Its primary objective is end-to-end compatibility of international telecommunications connections.

LAPD   Link Access Procedure for D-Channel. LAPD is a subset of the HDLC protocol and is used for transmission of path maintenance information over the C-Bit Parity data link.

LCV   Line Code Violation. This term denotes a received bipolar pulse which violates the HDB3 ternary coding scheme. LCV events are detected and accumulated by the D3MX.

LIU   Line Interface Unit. This term refers to circuitry which interfaces a serial communications circuit to a transmission medium such as coaxial cabling. The electrical interfaces for DS1, E1, DS2, and DS3 are standardized (ITU-T G.703).

LOS   Loss-of-Signal. This term refers to the state a clock recovery unit is in when there is no input signal. Since DS3 requires either a minimum pulse density or the use of a zero code suppression scheme (such as HDB3), the D3MX monitors for LOS by monitoring the number of consecutive spaces (zeros) received.

M12   Multiplexer, Order 1 to Order 2. This term generally refers to a system used for asynchronous multiplexing/demultiplexing of four DS1 formatted signals to/from a single DS2 serial stream.

        This term is also used for the associated multiplexing format defined in ANSI T1.107.

M23   Multiplexer, Order 2 to Order 3. This term generally refers to a system used for asynchronous multiplexing/demultiplexing of seven DS2 formatted signals to/from a single DS3 serial stream.

        This term is also used for the associated multiplexing format defined in ANSI T1.107.

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MX12   Multiplexer, Order 1 to Order 2. This is PMC-Sierra's mnemonic label for the functional blocks in the D3MX which performs asynchronous multiplexing/demultiplexing of four DS1 formatted signals to/from a single DS2 serial stream.

MX23   Multiplexer, Order 2 to Order 3. This is PMC-Sierra's mnemonic label for the functional block in the D3MX which performs asynchronous multiplexing/demultiplexing of seven DS2 formatted signals to/from a single DS3 serial stream.

NRZ   Non-Return-to-Zero. This refers to the common electrical coding scheme for serial digital data. Logical ones are represented as a pulse which is high for the full bit period. Logical zeros are represented as no pulse for the full bit period. This scheme is useful for serial digital data which has an associated clock signal.

OOF   Out-Of-Frame alignment. This is the state a framer circuit is in if it cannot find the frame alignment pattern within the received serial data.

PLL   Phase-Locked Loop. The generic term for a feed-back system which generates a clock with a fixed (locked) phase/frequency relationship to some reference clock.

QDSX   Quad DSX/E1 Transceiver. This is PMC-Sierra's mnemonic label for the PM4314 Quad DSX/E1 Transceiver device. This is a fully integrated quad T1/E1 LIU which is fully compatible to the standardized (ITU-T G.703) electrical interfaces for the 1544 kbit/s and 2048 kbit/s transmission rates.

PMON   Performance Monitor. This is PMC-Sierra's mnemonic label for the Performance Monitor functional block of the D3MX. It contains counters which accumulate the performance statistics (typically updated once a second).

RBOC   Receive Bit-Oriented Code processor. This is PMC-Sierra's mnemonic label for the functional block of the D3MX which monitors and extracts bit-oriented codewords from the received C-Bit Parity FEAC channel.

RFDL   Receive Facility Data Link processor. This is PMC-Sierra's mnemonic label for the functional block of the D3MX which monitors and extracts LAPD packets from the received C-Bit Parity path maintenance data link channel.

RZ   Return-to-Zero. This refers to an electrical coding scheme for serial digital data. Logical ones are represented as a pulse which is high for half the bit period then returns to low (zero) for the remainder of the bit period. Logical zeros are represented as no pulse. This scheme is useful for serial digital data from which a clock must be recovered.

SRTS   Synchronous Residual Time Stamp. This is a standardized (ITU-T I.363) method of conveying timing information across an ATM network carrying AAL1 structures. SRTS gives information about the difference between the ATM transport timing and the timing of the AAL1 tributary.

T1   Transmission format level 1. This term describes systems carrying DS1-formatted signals electrically over a physical cable plant.

T1XC   T1 Framer/Transceiver. This is PMC-Sierra's mnemonic label for the PM4341A T1 framer/transceiver device. This is a fully integrated framer suitable for processing the DS1 tributaries multiplexed/demultiplexed by the D3MX.

T3   Transmission format level 3. This term describes systems carrying DS3-formatted signals electrically over a physical cable plant.

TRAN   Transmit Framer. This is PMC-Sierra's mnemonic label for the functional block of the D3MX which generates and inserts the DS3 framing overhead in the transmit data path.

TQUAD   T1 Quad Framer. This is PMC-Sierra's mnemonic label for the PM4344 Quad T1 framer device. This is a fully integrated quad framer suitable for processing the DS1 tributaries multiplexed/demultiplexed by the D3MX.

XBOC   Transmit Bit-Oriented Code processor. This is PMC-Sierra's mnemonic label for the functional block of the D3MX which generates bit-oriented codewords (under microprocessor control) in the transmitted C-Bit Parity FEAC channel.

XFDL   Transmit Facility Data Link processor. This is PMC-Sierra's mnemonic label for the functional block of the D3MX which constructs LAPD packets (under microprocessor control) in the transmitted C-Bit Parity path maintenance data link channel.

BACKGROUND AND OVERVIEW

PMC-Sierra's PM8313 M13 Multiplexer is a full-featured device for multiplexing and demultiplexing DS1, E1, or DS2 serial streams to and from a DS3 serial stream.

Due to the versatility of the D3MX, the data book for that device is quite lengthy. In order to help customers quickly find the answers to their questions, the following list of answers to frequently asked questions has been compiled.

FREQUENTLY ASKED QUESTIONS

Q1)   Are there any reference designs available for the D3MX?

A1)   Yes. There is a reference design (PMC-951003) available for a D3MX module which is part of PMC-Sierra's PM4944 M13 Multiplexer Reference Design . This design shows the interface of the D3MX to the AT&T T7295-6 and T7296 DS3 LIU chip set.

Additionally, a document (PMC-941142) is available which contains a description, schematics and layout information for the D3MX evaluation board used for PMC-Sierra's in-house feature testing and product verification.

There is an application note (PMC-950946) available which contains some implementation information for interfacing the D3MX to the Silicon Systems 78P7200 DS3 LIU. The application note addresses a recommended way of buffering the weak outputs of the 78P7200 to improve compatibility with the D3MX inputs.

PMC-Sierra Sales Representatives have copies of these documents available for distribution. It is suggested that customers periodically query their local PMC-Sierra Sales Representative for the latest application notes for the D3MX.

PMC-Sierra also has a World Wide Web site at http://www.pmc-sierra.com from which documentation can be ordered or down-loaded.

Q2)   What are the recommended DS3 line interface units to use with the D3MX?

A2)   There are two solutions for the DS3 LIU that are commonly used with the D3MX. Silicon Systems has the SSI 78P72000 which is a single chip DS3 LIU. AT&T Microelectronics has a two-chip T7295-6 and T7296 DS3 LIU. The AT&T devices are also second-sourced by EXAR Corporation.

Both LIU solutions are suitable for use with the D3MX provided the recommendations given in the D3MX reference designs and application notes are followed.

Q3) **What are some recommended oscillator manufacturers for use in D3MX designs?**

A3) Any reputable crystal oscillator manufacturer should be able to provide the 44.736MHz oscillator to source the D3MX's required TICLK input signal. Since this is a non-standard frequency, they will generally have to be custom cut. The 1100 series of custom-cut crystal oscillators is suitable and available from most manufacturers. The oscillator should output TTL (or TTL-compatible) levels.

Some manufacturers which PMC-Sierra has used in-house with the D3MX are: Champion Technologies, Connor-Winfeld, Ecliptek Corporation, and Fox Corporation. These should be available from most electronics components distributors.

Custom cut oscillators can have very long lead times (16 weeks typical) so they should be ordered well in advance of when they will be needed.

Q4) **What are the gapping/jitter characteristics of the receive tributary output clocks, RD1CLK[28:1]?**

A4) The receive tributary output clocks, RD1CLK[28:1], of the D3MX are produced by two stages (MX23 and MX12) of demultiplexing. The demultiplexing operation intrinsically creates gapped clocks due to de-stuffing. Therefore, although the RD1CLK[28:1] output frequencies will be nominally the tributary line rate, they will have instantaneous frequency deviations (which are not smoothed out by the D3MX). Circuitry attached to the RD1CLK[28:1] outputs must be designed to accommodate the distortions of frequency and duty cycle which will occur.

The following calculations explain the characteristics of an RD1CLK[x] output associated with a DS1 receive tributary. The operation is similar for DS2 and E1 tributaries.

The high phase of RD1CLK[x] is always equal to 50% of the minimum tributary bit period giving:

$$T_{high} = \frac{50\%}{f_{max}} = \frac{50\%}{(44.736 \text{ MHz})\left(\frac{1}{28}\right)} = 313 \text{ ns}$$

The D3MX reacts to the stuffing information in the DS3 and DS2 overhead by extend the low phase of RD1CLK[x] to accommodate overhead and stuff gaps. The minimum low phase is equal to T_{high}:

$$T_{low\_min} = T_{high} = 313 \text{ ns}$$

The maximum low phase is equal to:

$$T_{low\_max} = T_{low\_min} + \text{M12 gapping} + \text{M23 gapping}$$

$$= T_{low\_min} + \text{DS2 overhead} + \text{M12 stuffing} + \text{DS3 overhead} + \text{M23 stuffing}$$

$$= T_{low\_min} + 1 \text{ DS2 period} + 4 \text{ DS2 periods} + 1 \text{ DS3 period} + 7 \text{ DS3 periods}$$

$$= 313 \text{ ns} + \frac{1+4}{6.312 \text{ MHz}} + \frac{1+7}{44.736 \text{ MHz}}$$

$$T_{low\_max} = 1284 \text{ ns}$$

In many designs, the D3MX's receive tributary outputs are connected directly to the receive inputs of PMC-Sierra's TQUAD device. The TQUAD data sheet gives a duty cycle requirement on its receive clock inputs, RCLKI[x], which seems to be violated by the characteristics of the D3MX's RD1CLK[x] signals; however, this is not the case because the TQUAD duty cycle requirement is related to minimum high and low phases of the clock at the highest frequency acceptable to the TQUAD which is much higher than the highest frequency of the RD1CLK[x] signals.

Instead, the TQUAD specification for its RCLKI[x] inputs should read that the minimum RCLKI[x] high and low phase widths are:

$$W_{high\_min} = W_{low\_min} = \frac{40\%}{1.6 \text{ MHz}} = 250 \text{ ns}$$

This shows that the RD1CLK[x] output signals from the D3MX easily satisfy the requirements of the RCLKI[x] inputs of the TQUAD, so the TQUAD is directly compatible with the D3MX. (Similar calculations will show that the PMC-Sierra's T1XC, EQUAD, E1XC, and QDSX devices are also directly compatible with D3MX.)

Q5) **During DS3 and DS2 out-of-frame conditions in the D3MX, how can the resulting off-frequency receive tributary clocks be compensated for?**

A5)   As indicated in Issue 1 of the D3MX Data Book Errata (PMC-950329), the MX23 and MX12 functional blocks of the D3MX continue to interpret the received C-Bit stuffing information even while in an AIS, OOF, or LOS condition. The result is that, under these conditions, the receive tributary clock outputs, RD1CLK[28:1], cannot be guaranteed to be stable.

Therefore, in designs where the receive tributary clocks are used as a timing reference to other circuitry, there should be a provision to select a "good" timing reference (perhaps from a local oscillator) in place of the receive tributary clocks which are derived from a MX12 or MX23 stage of the D3MX for which the associated FRMR functional block is under an AIS, OOF, or LOS condition.

Q6) How can loop-timing be provided in a D3MX design?

A6) The D3MX does not provide the ability to internally loop-time (i.e. use the receive DS3 clock as the reference for the transmit timing). Historically, DS3 is a plesiochronous format meaning that there is no requirement for each direction of a DS3 link to have its timing synchronized as long as it has a tight constraint ($\pm$ 20 ppm) on its long-term frequency tolerance.

If loop-timing is desired in a D3MX application, it must be done externally. This simply entails providing a multiplexer which provides the option of routing the same signal applied the D3MX's RCLK input to the TICLK input. Such an option is shown in the schematics of the D3MX Module of the M13 Reference Design (document PMC-951003).

Q7) Does DS1 timing derived from a AAL1 SRTS meet the jitter requirements of the D3MX's TD1CLK[28:1] inputs?

A7) In ITU-T I.363 Section 2.5.2.2.1.a, it says that "the SRTS method is capable of meeting the jitter specifications of … the 1544 kbit/s hierarchy in Recommendation G.824."

ITU-T G.824 Section 3.3 states that "the jitter specifications for digital muldexes using positive justification are found in Recommendations G.743 and G.752." These specifications apply to the D3MX: G.743 specifies M12 multiplexing, and G.752 specifies M23 multiplexing.

ITU-T G.743 Figure 1 shows the lower limit of maximum tolerable input jitter to the M12 stage of multiplexing. The D3MX meets that specification.

These references imply that SRTS method can produce DS1 signals with jitter characteristics suitable to input directly into a multiplexer such as the D3MX.

However, care must still be taken since the jitter characteristics of the SRTS-derived timing depends on many factors. The clock signal applied to each of the TD1CLK[28:1] inputs of the D3MX will be generated by a PLL which is controlled by the AAL1 SRTS information. Therefore, the jitter on a TD1CLK[x] signals will be the combination of the intrinsic jitter of that PLL plus the jitter transferred through that PLL. The total jitter transferred will be a result of both the transport timing jitter as well as extraction jitter (generated by extracting the ATM cells from the transport overhead and extracting the AAL1 payload from the ATM cells) plus the jitter of the original DS1 signal being emulated.

Generally, the SRTS method is compatible with the D3MX so long as the PLL generating the TD1CLK[28:1] signals meets the muldex interface jitter requirements of ITU-T G.743.

Q8) **Does DS1 timing derived from a AAL1 SRTS meet the frequency requirements of the D3MX's TD1CLK[28:1] inputs?**

A8) Both the D3MX specification and the SRTS specification for frequency tolerance are directly related to the limits of the rate adaptation for each method.

The D3MX implements the ANSI T1.107 M12 and M23 (or C-Bit Parity) multiplexing formats. Both of these formats use bit stuffing (positive justification) to pad the tributaries to fill up the higher order bandwidth. There are a limited number of bit stuffing opportunities per higher order frame, therefore only a limited frequency difference can be tolerated.

Similarly, the SRTS can only convey a limited amount of frequency difference. ITU-T I.363 states that SRTS has a frequency range of ±200ppm frequency.

The SRTS will convey the long-term frequency tolerance of the source of the DS1 information across the ATM network. Therefore, as long as the original source of the DS1 timing is within ±130ppm, there should not be a problem with interfacing to the D3MX. This should generally be the case as ITU-T G.703 specifies that DS1-formatted signals must have a frequency tolerance of ±50ppm.

Q9) **What are the maximum data delays through the D3MX?**

A9) In the transmit path, the maximum delay is:

$$D_{tx\_max} = 15 \text{ DS2 periods} + 20 \text{ DS3 periods}$$

$$= \frac{15}{6.312 \text{ MHz}} + \frac{20}{44.736 \text{ MHz}}$$

$$D_{tx\_max} = 2.823 \text{ }\mu s$$

In the receive direction the maximum delay is:

$$D_{tx\_max} = 5 \text{ DS2 periods} + 15 \text{ DS3 periods}$$

$$= \frac{5}{6.312 \text{ MHz}} + \frac{15}{44.736 \text{ MHz}}$$

$$D_{tx\_max} = 1.127 \text{ } \mu s$$

Q10) **What is the correspondence between the D3MX's DS3 functionality and the ANSI T1.107 specification?**

A10) Section 9 of ANSI T1.107 (1995) specifies the DS3 format.

The D3MX's FRMR, PMON, RBOC, and RFDL functional blocks are responsible for finding and processing the DS3 framing overhead and for extracting the payload from the received 44.736 MHz serial digital stream (input on the RPOS, RNEG and RCLK pins); the D3MX's TRAN, XBOC, and XFDL functional blocks are responsible for generating the appropriate DS3 framing overhead and interleaving it with the transmit payload to create the transmitted 44.736MHz serial digital stream (output on the TPOS, TNEG and TCLK pins).

The F-Bit and M-Bit channels in the DS3 framing overhead are used to indicate the subframe and frame alignment respectively as described in ANSI T1.107 Sections 9.1.1.1 and 9.1.1.2.

- The D3MX's FRMR functional block first finds the F-Bit alignment, then the M-Bit alignment, as described in the Functional Description in the D3MX Data Book. Once both F-Bit and M-Bit alignment is determined, the FRMR declares in-frame (OOFV=0 in Register 37H) and begins to extract and process the remain framing overhead channels, as explained below. (The received DS3 framing overhead is also extracted serially to the RODAT, ROCLK, RMFP, RMSFP, ROHP, ROHCLK, ROHFP, and ROH pins.)

  The D3MX always accumulates received F-Bit and M-Bit errors in the PMON FERR Counter (Registers 16H and 17H) based on the current (or last known) frame alignment.

  The FRMR declares out-of-frame (OOFV=1 in Register 37H) based on an algorithm selected by the M308 bit in Register 34H.

- The D3MX's TRAN functional block inserts the F-Bits and M-Bits with the cyclic patterns defined in ANSI T1.107 Sections 9.1.1.1 and 9.1.1.2. F-Bit and M-Bit errors can be forced (for diagnostic purposes) by the microprocessor (controlled by the DFERR and DMERR bits respectively in Register 0DH).

The P-Bit channel in the DS3 framing overhead is used to indicate parity information for the preceding DS3 frame as described in ANSI T1.107 Sections 9.1.1.3 and 9.1.5.

• The D3MX always accumulates received P-Bit errors in the PMON PERR Counter (Registers 16H and 17H) based on the current (or last known) frame alignment.

• The D3MX's TRAN functional block always calculates and inserts the P-Bits as required by ANSI T1.107 Section 9.1.5. P-Bit errors can be forced (for diagnostic reasons) by the microprocessor (controlled by the DPERR bit in Register 0DH).

The X-Bit channel in the DS3 framing overhead is used for a Remote Alarm Indication (RAI) as described in ANSI T1.107 Section 9.1.1.4.

• The D3MX declares a Far End Receive Failure (FERFV=1 in Register 37H) when the received X-Bits are equal and logic zero. It clears the Far End Receive Failure (FERFV=0) when the received X-Bits are equal and logic one. If the X-Bits are not equal, then the FERF status will remain in the previous state. During an out-of-frame state (OOFV=1 in Register 37H), the FERF status will be frozen in its last state. The FERF status is buffered so that there is a better than 99.99% chance of freezing the correct value.

• The D3MX's TRAN functional block can control the outgoing X-Bits via the FERF bit in Register 0CH.

The C-Bit channel in the DS3 framing overhead has application-specific usage. The three applications standardized in ANSI T1.107 are M23 (Section 9.2), C-Bit Parity (Section 9.3), and unchannelized (Section 9.4). Only the M23 and C-Bit Parity applications apply to the D3MX.

In either format, the first C-Bit in M-subframe 1 is used as an application identification channel (AIC) — for C-Bit Parity, the AIC shall be set to logic one; for M23, the AIC can be random.

• The D3MX monitors the received AIC and will indicate (CBITV=1 in Register 37H) if the C-Bit Parity application is expected. In the M23 application, the C-Bits are employed to convey stuffing information related to the multiplexing of the DS2 tributaries — this functionality is explained for another frequently asked question, answered below. In the C-Bit Parity application, the C-Bits are used for a variety of functions, as explained below.

• The D3MX's TRAN functional block will automatically generate the AIC according to the application selected with the CBTRAN bit in Register 0CH.

In the M23 application, the C-Bits are employed to denote the presence or absence of stuffed bits as described in ANSI T1.107 Section 9.2.

- The D3MX's MX23 functional block monitors the received C-Bits and use the stuffing information to demultiplex the received DS2 tributaries.

- The D3MX's MX23 functional block controls the outgoing C-Bits to reflect the stuffing actions performed to multiplex the transmitted DS2 tributaries.

The C-Bit channel is also used to request far-end loopbacks as described in ANSI T1.107 Section 9.2.1. Whether or not the C3 bit in each M-subframe is equal to the C1 and C2 bits indicates if a loopback is requested.

- The D3MX's MX23 functional block monitors the received C-Bits for loopback requests (as defined by the LBCODE[1:0] bits in Register 28H) and can indicate and/or interrupt if a loopback request is detected or cleared. The loopbacks can be controlled by the microprocessor (using LBA[7:1] bits in Register 2BH).

- The D3MX's MX23 functional block allows the insertion of loopback requests in the transmitted C-Bits (using the ILBR[7:1] bits in Register 2CH).

In the C-Bit Parity application, the second C-Bit in M-subframe 1 is designated as a reserved Network Requirement bit as described in ANSI T1.107 Section 9.3.2.

- The D3MX monitors the received Network Requirement bit and reflects it in the RNR bit in Register 06H.

- The D3MX TRAN transmit the Network Requirement bit as indicated by the TNR bit in Register 06H.

In the C-Bit Parity application, the third C-Bit in M-subframe 1 provides a FEAC channel as described in ANSI T1.107 Section 9.3.3. The FEAC channel is used to carry 16-bit codewords to convey information on far-end alarm status and to initiate loopbacks at the far-end terminal.

- The D3MX's RBOC functional block monitors the received FEAC channel and can generate interrupts when a codeword is received. The D3MX does not interpret the codewords, rather it extracts them to a register (Register 33H) for microprocessor processing.

- The D3MX's XBOC functional block transmits bit-oriented codes on the FEAC channel under microprocessor control (via Register 31H).

In the C-Bit Parity application, the three C-Bits in M-subframe 3 are designated as path parity bits (CP-Bits) as described in ANSI T1.107 Section 9.3.5. The CP-Bits are duplicates of the original P-Bits, but whereas the P-Bits may be regenerated while traversing the network, the path parity bits should pass through unchanged (except for CP-Bit errors and AIS insertion).

- The D3MX accumulates received CP-Bit errors in the PMON CPERR Counter (Registers 1CH and 1DH) based on the current (or last known) frame alignment.

- The D3MX's TRAN functional block automatically generates and inserts the CP-Bits. CP-Bit errors can be forced (for diagnostic reasons) by the microprocessor (controlled by the DCPERR bit in Register 0DH).

In the C-Bit Parity application, the three C-Bits in M-subframe 4 are designated as Far-End Block Error (FEBE) indications as described in ANSI T1.107 Section 9.3.6.

- The D3MX accumulates received FEBEs in the PMON FEBE Counter (Registers 1EH and 1FH) based on the current (or last known) frame alignment.

- The D3MX's TRAN functional block automatically generates outgoing FEBEs in response to the condition defined by the ALTFEBE bit in Register 06H. A FEBE can also be forced by the microprocessor (controlled by the DFEBE bit in Register 0DH).

In the C-Bit Parity application, the three C-Bits in M-subframe 5 are designated as path maintenance data link bits (DL-Bits) as described in ANSI T1.107 Section 9.3.7. The format of this data link is LAPD (a subset of HDLC). The LAPD packets convey information on DS3 path ID, DS3 Idle ID, and DS3 Test Signal ID.

- The D3MX's RFDL functional block is an integrated HDLC serial controller capable of terminating the DL-Bits. Additionally, the DL-Bits are extracted serial to the RDLSIG and RDLCLK pins so that they can be processed by an external serial HDLC controller. The RFDL detects the start and end of packets, extracts the packet payload octets into a FIFOed register (Register 27H) and calculates the frame check sequence indicating errors if any (with CRC bit in Register 26H). The use of the RFDL functional block is explained in detail in the D3MX data book in the section entitled "Using the Internal Data Link Receiver."

- The D3MX's XFDL functional block is an integrated HDLC serial controller capable of generating the DL-Bits. The XFDL automatically delimits packets with flags and automatically generates the FCS. The payload data is inserted via Register 22H. Optionally, the internal controller can be bypassed (using the TEXHDLC bit in Register 03H) and the transmit data link data inserted from an external source via the TDLSIG and TDLCLK pins. The use of the RFDL functional block is explained in detail in the D3MX data book in the section entitled "Using the Internal Data Link Transmitter."

Q11) What is the correspondence between the D3MX's DS2 functionality and the ANSI T1.107 specification?

A11) Section 8 of ANSI T1.107 (1995) specifies the DS2 format.

The D3MX's DS2-FRMR functional blocks are responsible for finding and processing the DS2 framing overhead and for extracting the payload from each of the seven received 6.312MHz serial digital stream; the D3MX's MX12 functional blocks are responsible for generating the appropriate DS2 framing overhead and interleaving it with the transmit payloads to create the seven transmitted 6.312MHz serial digital streams.

The DS2-FRMR and MX12 functional blocks conform to ANSI T1.107 format requirements when the G747 bits in Registers 40H, 50H, etc. and 48H, 58H, etc. are cleared to logic zero. Otherwise, these functional blocks conform to ITU-T G.747. Note that each of these blocks can be independently programmed for either T1.107 or G.747 mode as needed.

The F-Bit and M-Bit channels in the DS2 framing overhead are used to indicate the subframe and frame alignment respectively as described in ANSI T1.107 Sections 8.1.1.1 and 8.1.1.2.

- The D3MX's DS2-FRMR functional block first finds the F-Bit alignment, then the M-Bit alignment, as described in the Functional Description in the D3MX Data Book. Once both F-Bit and M-Bit alignment is determined, the DS2-FRMR declares in-frame (OOFV=0 in Registers 43H, 53H, etc.) and begins to extract and process the remain framing overhead channels, as explained below.

  The D3MX always accumulates received F-Bit and M-Bit errors in the DS2-FRMR FERR Counter (Registers 45H, 55H, etc.) based on the current (or last known) frame alignment.

  The FRMR declares out-of-frame (OOFV=1 in Registers 43H, 53H, etc.) based on an algorithm selected by the M2O5 bit in Registers 40H, 50H, etc.

- The D3MX's MX12 functional blocks insert the F-Bits and M-Bits with the cyclic patterns defined in ANSI T1.107 Sections 8.1.1.1 and 8.1.1.2. F-Bit and M-Bit errors can be forced (for diagnostic purposes) by the microprocessor (controlled by the FINV and MINV bits respectively in Register 48H, 58H, etc.).

The X-Bit channel in the DS2 framing overhead is used for a Remote Alarm Indication (RAI) as described in ANSI T1.107 Section 8.1.2.2.

- The D3MX declares a Far End Receive Failure (FERFV=1 in Registers 43H, 53H, etc.) when the received X-Bit is logic zero for two consecutive DS2 M-frames. It clears the Far End Receive Failure (FERFV=0) when the received X-Bit is logic one for two consecutive DS2 M-frames.

- The D3MX's MX12 functional block can control the outgoing X-Bits (via the XFERF bit in Registers 48H, 58H, etc.).

The C-Bit channel in the DS2 framing overhead has application-specific usage. Only one application is standardized in ANSI T1.107: MX12 multiplex. This is the application used by the D3MX.

The C-Bit channel is employed to denote the presence or absence of stuffed bits as describe in ANSI T1.107 Section 8.2.

- The D3MX's MX12 functional blocks monitor the received C-Bits and use the stuffing information to demultiplex the received DS1 tributaries.

- The D3MX's MX12 functional blocks control the outgoing C-Bits to reflect the stuffing actions performed to multiplex the transmitted DS1 tributaries.

The C-Bit channel is also used to request far-end loopbacks as described in ANSI T1.107 Section 8.2.1.1. Whether or not the C3 bit in each M-subframe is equal to the C1 and C2 bits indicates if a loopback is requested.

- The D3MX's MX12 functional block monitors the received C-Bits for loopback requests (as defined by the LBCODE[1:0] bits in Registers 49H, 59H, etc.) and can indicate and/or interrupt if a loopback request is detected or cleared. The loopbacks can be controlled by the microprocessor (using LBA[4:1] bits in Registers 4BH, 5BH, etc.).

- The D3MX's MX12 functional block allows the insertion of loopback requests in the transmitted C-Bits (using the ILBR[4:1] bits in Registers 4BH, 5BH, etc.).

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