

*Product Preview*

**TMOS V™**

**SO-8 for Surface Mount**

**N-Channel Enhancement-Mode Silicon Gate**

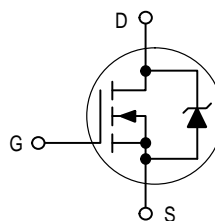
TMOS V is a new technology designed to achieve an on-resistance area product about one-half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E-FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

**New Features of TMOS V**

- On-resistance Area Product about One-half that of Standard MOSFETs with New Low Voltage, Low RDS(on) Technology
- Faster Switching than E-FET Predecessors

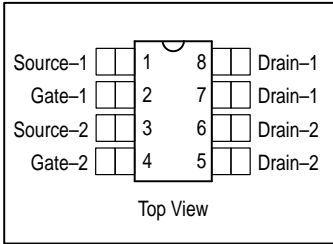
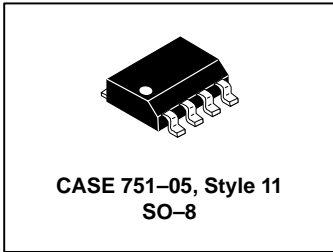
**Features Common to TMOS V and TMOS E-FETS**

- Avalanche Energy Specified
- IDSS and VDS(on) Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E-FET
- Miniature SO-8 Surface Mount Package – Saves Board Space
- Mounting Information for SO-8 Package Provided



**MMDF2N06VL**

**DUAL TMOS MOSFET**  
**2.5 AMPERES**  
**60 VOLTS**  
**RDS(on) = 0.130 OHM**



**MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	60	Vdc
Drain-to-Gate Voltage, (R <sub>G</sub> S = 1 MΩ)	V <sub>DGR</sub>	60	Vdc
Gate-to-Source Voltage — Continuous	V <sub>G</sub> S	± 15	Vdc
Drain Current — Continuous @ T <sub>A</sub> = 25°C	I <sub>D</sub>	2.5	Adc
— Continuous @ T <sub>A</sub> = 100°C	I <sub>D</sub>	0.5	
— Single Pulse (t <sub>p</sub> ≤ 10 μs)	I <sub>DM</sub>	7.5	Apk
Total Power Dissipation @ T <sub>A</sub> = 25°C (1)	P <sub>D</sub>	2.0	W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy — Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 25 Vdc, V <sub>G</sub> S = 5.0 Vdc, Peak I <sub>L</sub> = 3.3 Apk, L = 10 mH, R <sub>G</sub> = 25 Ω)	E <sub>AS</sub>	54	mJ
Thermal Resistance, Junction to Ambient (1)	R <sub>θJA</sub>	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 0.0625" from case for 10 seconds	T <sub>L</sub>	260	°C

**DEVICE MARKING**

2N6VL

(1) Mounted on G10/FR4 glass epoxy board using minimum recommended footprint.

**ORDERING INFORMATION**

Device	Reel Size	Tape Width	Quantity
MMDF2N06VLR1	7"	12mm embossed tape	500
MMDF2N06VLR2	13"	12mm embossed tape	2500

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# MMDF2N06VL

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 0.25 mAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 —	— 66	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	— —	— —	10 100	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ± 15 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	—	—	100	nAdc

## ON CHARACTERISTICS(1)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 —	1.5 3.0	2.0 —	Vdc mV/°C
Static Drain-to-Source On-Resistance (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 2.5 Adc)	R <sub>DS(on)</sub>	—	0.12	0.13	Ohm
Drain-to-Source On-Voltage (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 2.5 Adc) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 1.25 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	— —	— —	0.4 0.3	Vdc
Forward Transconductance (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 1.25 Adc)	g <sub>FS</sub>	1.0	3.0	—	Mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	—	340	480	pF
Output Capacitance		C <sub>oss</sub>	—	110	150	
Transfer Capacitance		C <sub>rss</sub>	—	27	50	

## SWITCHING CHARACTERISTICS(2)

Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 2.5 Adc, V <sub>GS</sub> = 5.0 Vdc, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	—	10	20	ns
Rise Time		t <sub>r</sub>	—	30	60	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	32	60	
Fall Time		t <sub>f</sub>	—	28	60	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 2.5 Adc, V <sub>GS</sub> = 5.0 Vdc)	Q <sub>T</sub>	—	11	20	nC
		Q <sub>1</sub>	—	1.5	—	
		Q <sub>2</sub>	—	3.8	—	
		Q <sub>3</sub>	—	3.5	—	

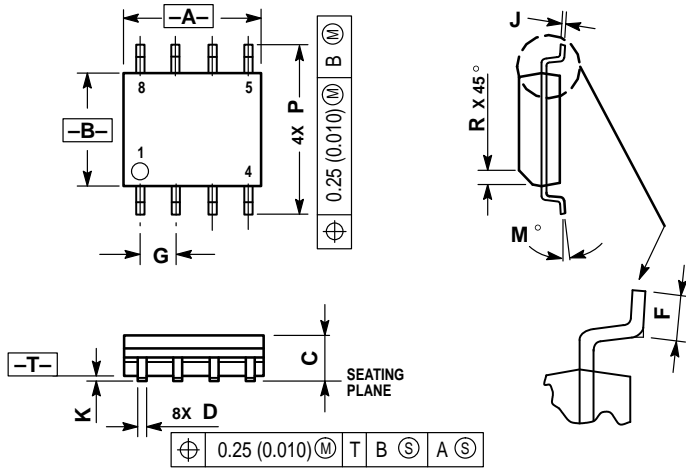
## SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage(1)	(I <sub>S</sub> = 2.5 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 2.5 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	— —	0.84 0.67	1.2 —	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 2.5 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	—	49	—	ns
		t <sub>a</sub>	—	32	—	
		t <sub>b</sub>	—	17	—	
Reverse Recovery Storage Charge		Q <sub>R</sub>	—	0.08	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS




- NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
  2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  3. DIMENSIONS ARE IN MILLIMETER.
  4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0°	7°
P	5.60	6.20
R	0.25	0.50

- STYLE 11:
1. SOURCE 1
  2. GATE 1
  3. SOURCE 2
  4. GATE 2
  5. DRAIN 2
  6. DRAIN 2
  7. DRAIN 1
  8. DRAIN 1

CASE 751-05  
SO-8  
ISSUE P

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