MC149571

Advance Information

Multi-Standard Video Processor

The MC149571 multi-standard video processor provides the video compression and scaling functions for Qorus® video conferencing system applications. To support video communications, the video processor can encode either H.261 or H.263 video bitstream. The processor has a direct interface to a NTSC/PAL decoder. It requires 1 Mbyte EDO DRAMs for frame storing. The MC149571 video processor performs two major independent video functions: Video Pre-Processing, Video Encoding. The functional block diagram in **Figure 1** shows the major functional modules that enable the MC149571 to perform these functions.

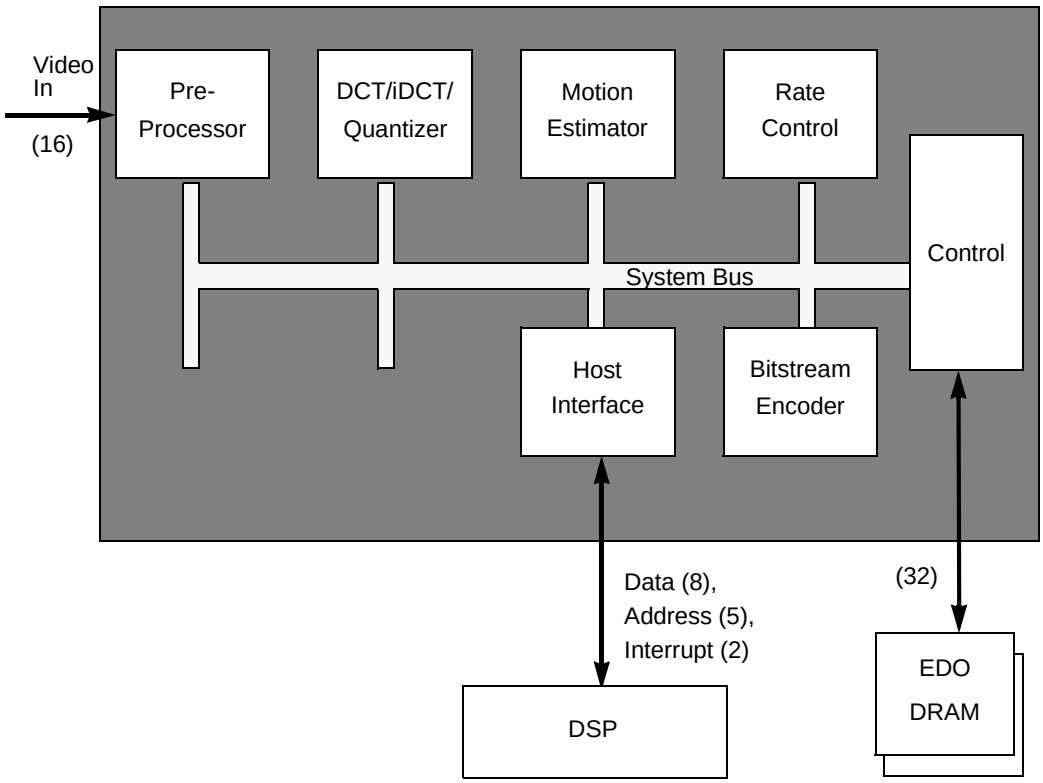

Figure 1. MC149571 Functional Block Diagram

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FOR TECHNICAL ASSISTANCE:

Telephone: 1-800-521-6274

Internet: http://www.mot-sps.com/sps/general/sales.html

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the RESET pin is active when low.)
asserted	Means that a high true (active high) signal is high or that a low true (active low) signal is low
deasserted	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Features

- Multiple ITU Video Standard support:
  - ITU H.261
  - ITU H.263
- Video encode engine:
  - Encodes CIF (352 × 288) and QCIF (176 × 144) sized images
  - Encodes CIF at 15 frames per second and QCIF at 30 frames per second
- Supports from 16 to 384 kbps video bit rates
- Video Pre-Processing
  - Accepts NTSC or PAL input video signals
  - Non-linear temporal noise core filter reduces noise and improves coding efficiency
  - Data input stream compliant with 4:2:2 (16-bit) CCIR 601 standard
  - Glueless interface to industry standard NTSC/PAL video decoders
- Motion Estimation
  - Fully supports H.263 Annex F Advanced Prediction Mode
  - Four motion vectors per macroblock generated supports overlapped block motion compression for better picture quality at lower bit rates
  - Unrestricted motion vectors can extend past picture boundaries to improve performance
  - Motion estimation vector range extends to ±15.5 vertical and horizontal
  - 384 full pel motion vector candidates
  - Half-pixel search motion estimation
- Rate Control
  - Intelligent frame rate control
  - Dynamic trade-off between temporal/spatial quality and low latency frame rate adjustment on user input during video calls
  - Minimum delay due to fully pipelined processing
- Other features
  - 8-bit Host Interface provides chip control and bitstream interface
  - Twenty three On-chip registers allow the user to program video parameters
  - On-chip DRAM controller interfaces EDO DRAM through a 32-bit Data Bus
  - Programmable on-chip Phase Lock Loop (PLL) that can be programmed to run from 27 MHz to 44 MHz
  - Operating frequency of 44 MHz with video input frequency of 13.5 MHz
  - 5 V tolerant interface on I/O pins
  - Optimized for 3.3 V operation from 0°C to 70°C ambient temperature
  - 208 Plastic QFP package

1

Signal Descriptions

1.1 Signal Groupings

The input and output signals of the MC149571 are organized into functional groups, as shown in **Table 1-1** and as illustrated in **Figure 1-1**. The MC149571 is operated from a 3.3 V supply; however, all the input and bidirectional pins can tolerate 5 V.

Table 1-1. MC149571 Functional Signal Groupings

Functional Group	Number of Signals	Detailed Description
Power (VCC_xx) and Ground (GND_xx)	55	**Table 1-2**
Reset	1	**Table 1-3**
Phase Lock Loop (PLL) and Clock	2	**Table 1-4**
Operation Mode Select	3	**Table 1-5**
Host Interface	18	**Table 1-6**
Video Input	19	**Table 1-7**
DRAM Interface	45	**Table 1-8**

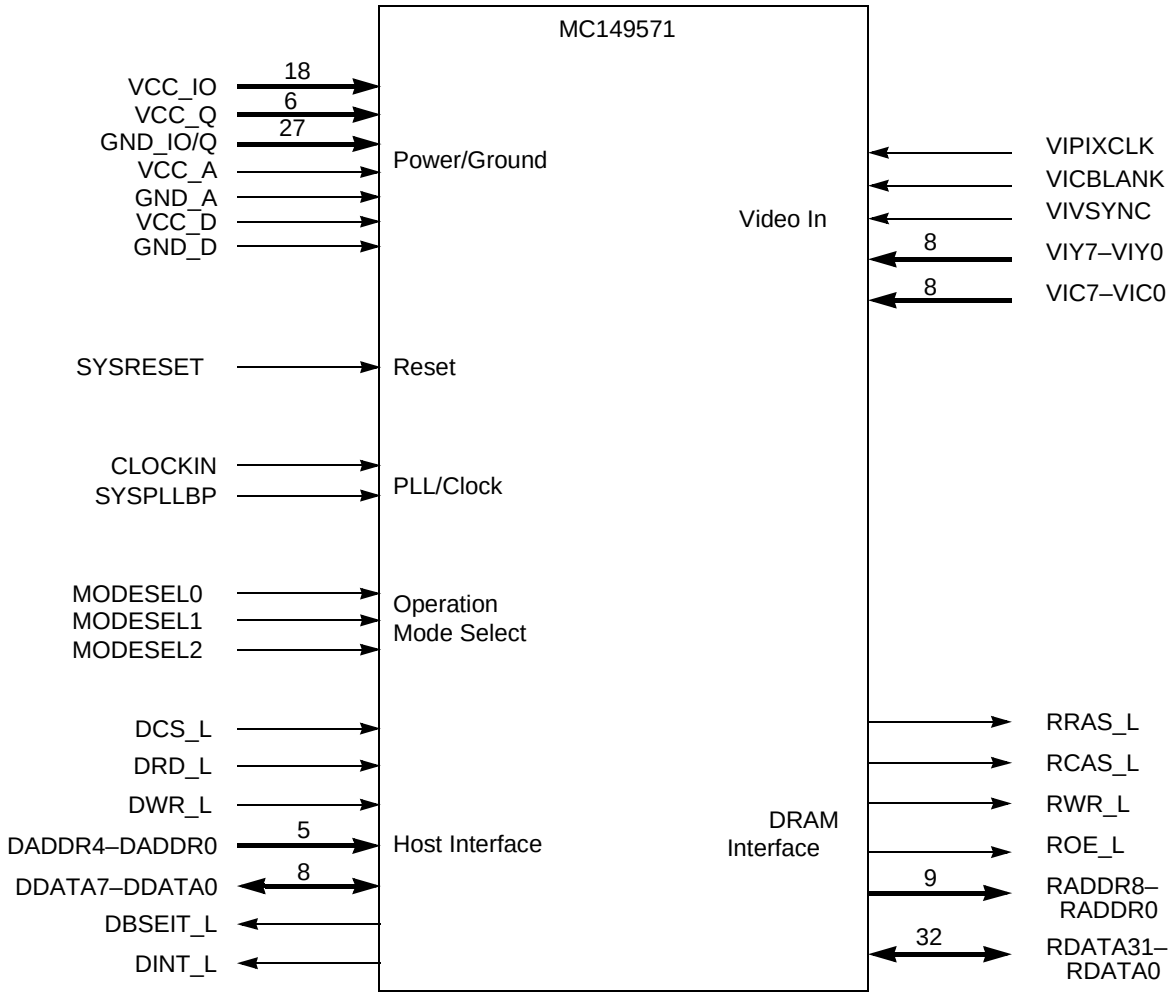

Figure 1-1. *MC149571 Signals Identified by Functional Group*

1.2 Power and Ground Signals

Table 1-2. MC149571 Power and Ground Signals

Signal Name	Description
VCC_IO	I/O Power
VCC_Q	Core Power
GND_IO/Q	I/O and Core Ground
VCC_A	PLL Analog Power
GND_A	PLL Analog Ground
VCC_D	PLL Digital Power
GND_D	PLL Digital Ground

1.3 Reset Signals

Table 1-3. MC149571 Reset Signal

Signal Name	Signal Type	Detailed Description
SYSRESET	Input*	Chip reset

Note: All inputs are 5 V tolerant.

1.4 PLL and Clock Signals

Table 1-4. MC149571 PLL and Clock Signals

Signal Name	Signal Type	Detailed Description
CLOCKIN	Input[1]	Clock input to the on-chip PLL (default = 20 MHz)
SYSPLLBP	Input[1,2]	Asserting this signal bypasses the on-chip PLL. This pin must be asserted to bypass the PLL before changing the Operation Mode from Normal to the PLL Programming Mode.

Notes: 1. All inputs are 5 V tolerant.
2. See **Section 1.5** for information about selecting the Operation Mode and its effect on PLL operation.

1.5 Operation Mode Signals

Table 1-5. MC149571 Operation Mode Signals

Signal Name	Signal Type	Detailed Description
MODESEL2–MODESEL0	Input[1]	The MODESEL signals combine to define eight operational modes for normal operations and diagnostics.[2,3,4]

Notes: 1. All inputs are 5 V tolerant.
2. Only two operation modes are available to users:
- Normal Operation Mode (all three signals = 0), and
- PLL Programming Mode (all three signals = 1).

3. In the Normal Operation Mode, the PLL generates a default internal clock frequency of 2.2 times CLOCKIN. For example, if CLOCKIN = 20 MHz, the internal clock frequency is 44 MHz.
4. To change the ratio between CLOCKIN and the internal clock, select the PLL Programming Mode. See the MC149571 Programming Manual for information about programming the PLL ratio.

1.6 Host Interface Signals

Table 1-6. MC149571 Host Interface Signals

Signal Name	Signal Type	Detailed Description
DCS_L	Input[1]	Chip select from Embedded Controller
DRD_L	Input[1]	Read enable from Embedded Controller
DWR_L	Input[1]	Write enable from Embedded Controller
DADDR4–DADDR0	Input[1]	Emedded Controller Address bus
DDATA7–DDATA0	Bidirectional	Embedded Controller Interface data bus; 5 V tolerant
DBSEIT_L	Output	Embedded Controller BSE Interrupt
DINT_L	Output	Embedded Controller Interrupt

Note: 1. All inputs are 5 V tolerant.

1.7 Video Input Signals

Table 1-7. MC149571 Video Input Signals

Signal Name	Signal Type	Detailed Description
VIPIXCLK	Input[1]	Pixel clock
VICBLANK	Input[1]	Composite BLANK
VIVSYNC	Input[1]	Vertical Sync
VIY7–VIY0	Input[1]	Luma data Y in 4:2:2
VIC7–VIC0	Input[1]	Chroma data Cb/Cr

Note: 1. All inputs are 5 V tolerant.

1.8 DRAM Interface Signals

Table 1-8. MC149571 DRAM Interface Signals

Signal Name	Signal Type	Detailed Description
RRAS_L	Output	Row address strobe to EDO DRAMs
RCAS_L	Output	Column address strobe to EDO DRAMs
RWR_L	Output	Write enable to EDO DRAMs
ROE_L	Output	Output enable for EDO DRAMs
RADDR8–RADDR0	Output	Address bus to EDO DRAMs
RDATA31–RDATA0	Bidirectional	Memory data bus (5 V tolerant): • RDATA7–RDATA0 = Byte 1 • RDATA15–RDATA8 = Byte 2 • RDATA23–RDATA16 = Byte 3 • RDATA31–RDATA24 = Byte 4

2

Pinout and Packaging Information

2.1Introduction

This section provides a table showing how the signals described in **Section 1** are allocated. The MC149571 is available in a 208-pin Plastic QFP package.

Detailed package drawing for this device is avaiable on the Motorola web page at:

http://mot-sps.com/cgi-bin/cases

Use package 872-02 for the search.

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Table 2-1. MC149571 208 PQFP Package Signal List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VCC_IO	31	VCC_IO	61	VCC_IO	91	Reserved
2	GND_IO	32	GND_IO	62	DADDR0	92	VCC_IO
3	VIY0	33	Reserved	63	DADDR1	93	GND_IO
4	VIY1	34	Reserved	64	DADDR2	94	Reserved
5	VIY2	35	Reserved	65	DADDR3	95	Reserved
6	VIY3	36	Reserved	66	DADDR4	96	Reserved
7	VIY4	37	Reserved	67	VCC_IO	97	VCC_IO
8	VIY5	38	Reserved	68	GND_IO	98	GND_IO
9	VIY6	39	VCC_IO	69	DDATA0	99	ROE_L
10	VIY7	40	GND_IO	70	DDATA1	100	RWE_L
11	VCC_Q	41	GND_Q	71	DDATA2	101	RRAS_L
12	GND_Q	42	VCC_Q	72	DDATA3	102	VCC_IO
13	GND_IO	43	Reserved	73	VCC_IO	103	GND_IO
14	VCC_IO	44	Reserved	74	GND_IO	104	RADDR0
15	VIC0	45	Reserved	75	DDATA4	105	RADDR1
16	VIC1	46	Reserved	76	DDATA5	106	RADDR2
17	VIC2	47	Reserved	77	DDATA6	107	RADDR3
18	VIC3	48	Reserved	78	DDATA7	108	RADDR4
19	VIC4	49	Reserved	79	VCC_IO	109	RADDR5
20	VIC5	50	Reserved	80	GND_IO	110	RADDR6
21	VIC6	51	VCC_IO	81	GND_Q	111	RADDR7
22	VIC7	52	GND_IO	82	VCC_Q	112	RADDR8
23	VCC_IO	53	GND_IO	83	DBSEIT_L	113	VCC_IO
24	GND_IO	54	GND_IO	84	DINT_L	114	GND_IO
25	Reserved	55	GND_IO	85	DCS_L	115	RDATA0
26	Reserved	56	Reserved	86	VCC_IO	116	RDATA1
27	Reserved	57	Reserved	87	GND_IO	117	RDATA2
28	Reserved	58	VCC_Q	88	DWR_L	118	RDATA3
29	Reserved	59	GND_Q	89	DRD_L	119	RDATA4
30	Reserved	60	GND_IO	90	Reserved	120	RDATA5

Table 2-1. MC149571 208 PQFP Package Signal List (Continued)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
121	RDATA6	144	RDATA23	167	GND_IO	190	Reserved
122	RDATA7	145	RDATA24	168	Reserved	191	Reserved
123	VCC_Q	146	GND_IO	169	Reserved	192	Reserved
124	GND_Q	147	VCC_IO	170	Reserved	193	Reserved
125	RDATA8	148	RDATA25	171	Reserved	194	Reserved
126	RDATA9	149	RDATA26	172	Reserved	195	Reserved
127	RDATA10	150	Reserved	173	Reserved	196	Mode Select 0
128	RDATA11	151	RDATA28	174	Reserved	197	VCC_Q
129	RDATA12	152	RDATA29	175	DDATA4	198	GND_Q
130	RDATA13	153	RDATA30	176	Reserved	199	SYSRESET
131	RDATA14	154	Reserved	177	Reserved	200	Reserved
132	RDATA15	155	RDATA31	178	Reserved	201	SYSPLLBP
133	RCAS_L	156	Mode Select 1	179	GND_A	202	Reserved
134	VCC_IO	157	Mode Select 2	180	VCC_A	203	Reserved
135	GND_IO	158	Reserved	181	CLOCK_IN	204	Reserved
136	RDATA16	159	Reserved	182	VCC_D	205	Reserved
137	RDATA17	160	Reserved	183	GND_D	206	VIPIXCLK
138	RDATA18	161	Reserved	184	Reserved	207	VIVSYNC
139	RDATA19	162	Reserved	185	Reserved	208	VICBLANK
140	RDATA20	163	Reserved	186	Reserved		
141	RDATA21	164	Reserved	187	Reserved		
142	Reserved	165	Reserved	188	Reserved		
143	RDATA22	166	VCC_IO	189	Reserved		

Notes:

1. All pins marked RESERVED shall not be connected, otherwise, the device may not operate.

3

Specifications

3.1 Introduction

The MC149571 specifications are preliminary and are from design simulations. They may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after full characterization and device qualifications are complete.

3.2 Maximum Ratings

Table 3-1. Power and Temperature Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	–0.3 to +4.0	V
All input voltage	V_{IN}	GND to 5.5	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{STG}	–55 to +150	°C

Note: Absolute maximum ratings are stress ratings only and functional operation at the maximum limits is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

3.3 Thermal Characteristics

Table 3-2. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	32	°C/W

3.4 DC Electrical Characteristics

Table 3-3. DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	5.5	V
Input Low Voltage	V_{IL}	0	—	0.8	V
Output High Voltage • DDATA7–DDATA0, RCAS_L (I_{OH} = -8mA) • RDATA31–RDATA0, RADDR8–RADDR0, ROE_L, RRAS_L, RWR_L (I_{OH} = -4 mA) • DBSEIN_L, DINT_L (I_{OH} = -2 mA)	V_{OH}	2.4	—	VCC	V
Output Low Voltage • DDATA7–DDATA0, RCAS_L (I_{OL} = 8mA) • RDATA31–RDATA0, RADDR8–RADDR0, ROE_L, RRAS_L, RWR_L (I_{OL} = 4 mA) • DBSEIN_L, DINT_L (I_{OL} = 2 mA)	V_{OL}	0	—	0.4	V
Input Leakage Current (@ 5.5V / Maximum V_{CC} / 0.0V)	I_{IN}	–10	—	10(1)	µA
Input Leakage Current (2) (@ Maximum V_{CC} / 0.0V)	I_{IN}	–10	—	100	µA
High Impedance Input Current	I_{tsi}	–10	—	10	µA
Icc in Normal Operation Mode	I_{CC}	—	—	450	mA
Input Capacitance	—	—	9		pF

Notes:

1.Not including the following 5 input pins with internal pull down resistor:

Mode Select 0, Mode Select 1, Mode Select 2, SYSRESET, SYSPLLBP

2. Input Leakage Current for:

Mode Select 0, Mode Select 1, Mode Select 2, SYSRESET, SYSPLLBP

3.5 AC Electrical Characteristics

The timing waveforms shown in this section are tested with a Vil maximum of 0.0 V and Vih minimum of 3.0V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. Output levels are measured with the production test machine Vol and Voh reference levels set at 1.2V and 1.6V, respectively.

3.5.1 MC149571 Chip Reset

MC149571 supports a level-sensitive reset. To generate a chip-level reset, assert the SYSRESET signal. This resets the registers associated with the PLL control. Then, 1 ms later, deassert SYSRESET. At this transition, the divide-by-two clock circuit is reset, and the internal chip reset is generated for eight system clock cycles as shown in **Figure 3-1**. Given a 20 MHz CLOCKIN and the default setting for the PLL programming register (F/R register), the MC149571 should be able to accept programmed values 22 CLOCKIN cycles after the falling edge of SYSRESET.

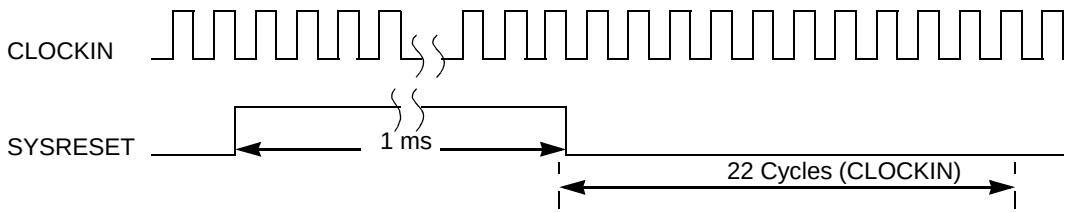

Figure 3-1. Reset Timing

3.5.2 PLL Programming Mode

MC149571 enters the PLL Programming mode when the three mode pins (MODESEL0, MODELSEL1, and MODESEL2) are set to all ones (111). In the PLL programming mode, the on-chip PLL is automatically by-passed and the MC149571 runs at half the frequency of CLOCKIN. The on-chip PLL can then be programmed by writing a desired ratio value into the PLL_R_F register ($1F). Note that the ratio of F/R can not be less than 1. Due to a settle time requirement for the PLL, the PLL must stay in this mode for at least 1 mSec after writing to the PLL_R_F register. An internal reset is triggered as soon as MC149571 exits the PLL Programming mode. The internal reset performs the same function as the normal system reset while reserving the new R and F values.

Warning: Performing a normal system reset after exiting the PLL programming mode returns the MC149571 to the default values.

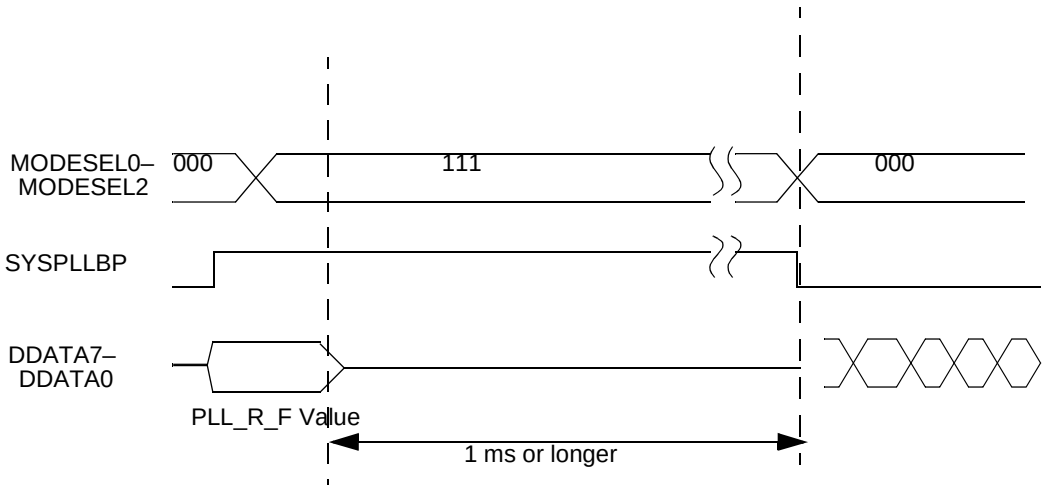

Figure 3-2. PLL ProgrammingTiming

3.5.3 Host Interface Write Timings

Table 3-4. Host Interface Write Timings (Host Writes to MC149571)

No.	Characteristics	Min Delay	Max Delay	Units
1	Address valid to Write Enable Deassertion	9	-	ns
2	Write Enable Cycle Time	35	-	ns
3	Write Enable Deassertion Time	3	-	ns
4	Write Data Setup Time w.r.t Write Enable Deassertion	5	-	ns
5	Write Data Hold Time w.r.t. Write Enable Deassertion	2	-	ns
6	Previous Read Enable Deassertion to Write Enable Deassertion	35	-	ns
7	Write Enable Deassertion to Address Not Valid	2	-	ns
8	Chip Select to Write Enable Assertion	0.1	-	ns
9	Write Enable Deassertion to Chip Select Inactive	2	-	ns

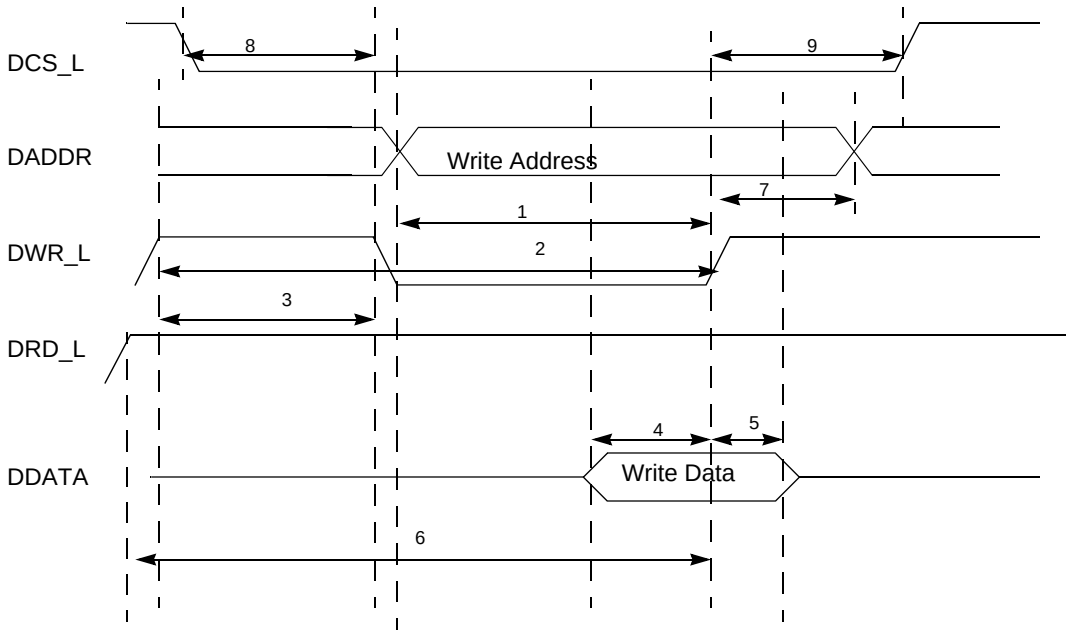

Figure 3-3. Host Interface Write Timings

3.5.4 Host Interface Read Timings

Table 3-5. Host Interface Read Timings (Host Read from MC149571)

No.	Characteristics	Min	Max	Units
1	Address valid to Data Active		16	ns
2	Read Enable Cycle Time	35	-	ns
3	Read Enable Deassertion Time	3	-	ns
4	Read Enable Assertion to Data Active		9	ns
5	Read Data Hold Time w.r.t. Read Enable Deassertion	1	6	ns
6	Previous Write Enable Deassertion to Read Enable Deassertion	35	-	ns
7	Read Enable Deassertion to Address Invalid	2	-	ns
8	Chip Select to Read Enable Assertion	0.1	-	ns
9	Read Enable De-assertion to Chip Select Inactive	2	-	ns

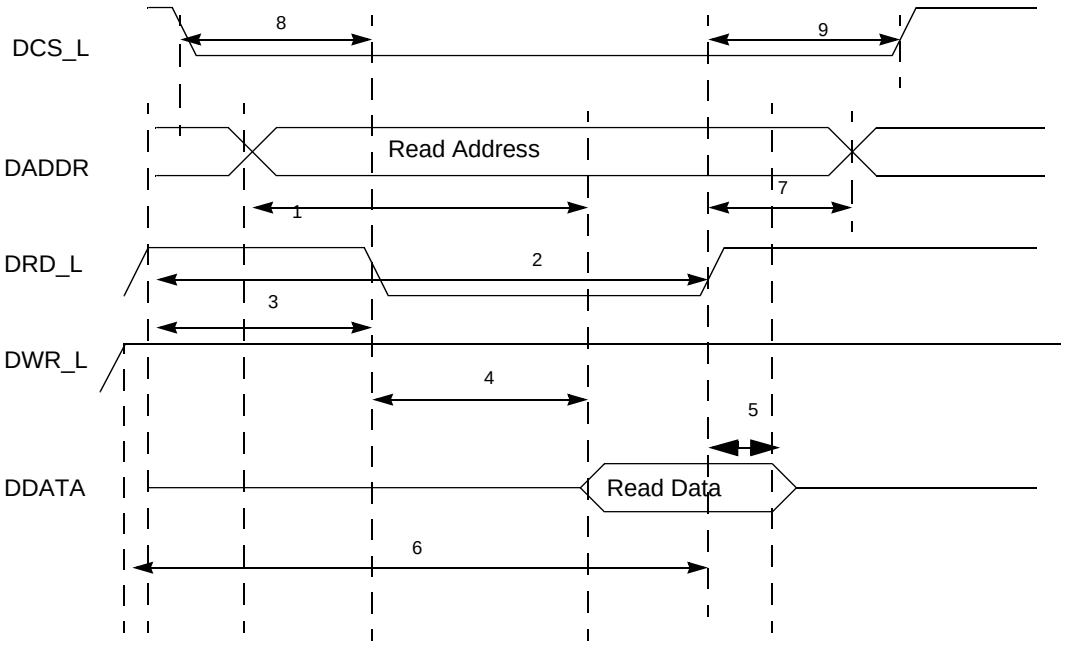

Figure 3-4. Host Interface Read Timings

3.5.5 Interrupt Timings

Table 3-6. Periodic Interrupt Latency Timings

Periodical Interrupts	Max. Host Response Time after an Interrupt Request	Minimum Time Between Interrupts	Units
Request for transmit of encoded bitstream (DBSEIT_L)	9	25.7	µs
Request for bits transmitted over channel (DINT_L)	1	33	ms
Request for incoming bitstream(DINT_L)	not limited	25.7	µs

There are no defined limits for non-periodic interrupts, such as:

- Unsupported H.263 options:
  - Unrestricted motion Vectors
  - CPM
  - PB frame
  - Arithmetic coding
- H.261/H.263 errors
  - Invalid Picture Type
  - Illegal Variable Length Code
  - More than 64 coefficients for run-length decode
  - Unexpected start code
  - Incorrect # Macroblocks
- Buffer Underflow/Overflow
  - Bitstream receive buffer
  - Bitstream transmit buffer

3.5.6 Video Signal Timing

Table 3-7. Video Timing

Clock Signals	Frequency	Units
VIPIXCLK	13.5	MHz

Note: The standard pixel clock used to interface to NTSC/PAL devices is 13.5 MHz. Other pixel clock rates are possible. Contact Motorola for additional information.

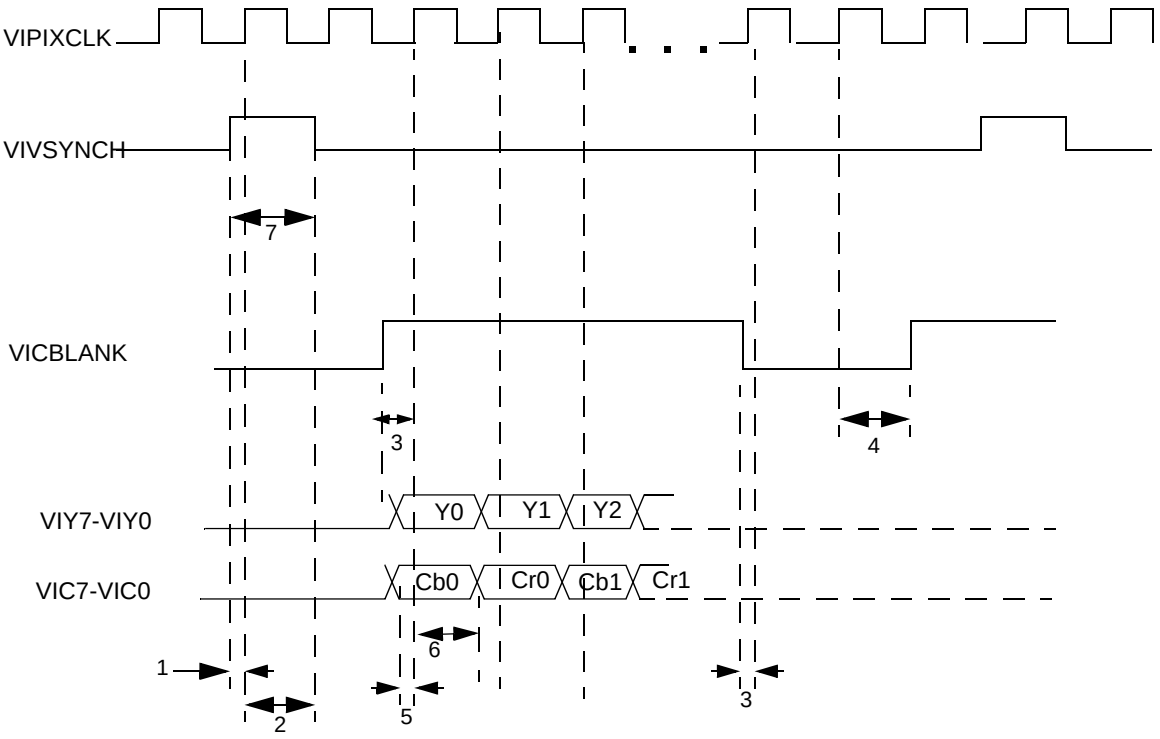

Figure 3-5. Input Video Signals

Table 3-8. Video Input Timings

No.	Characteristics	Min	Max	Units
1	VIVSYNCH Set-up Time	3	-	ns
2	VIVSYNCH Hold Time	3	—	ns
3	VICBLANK Active and Inactive Set-upTime	6	-	ns
4	VICBLANK Hold Time	3	-	ns
5	Data Set-up Time	3	-	ns
6	Data Hold Time	3	—	ns
7	VIVSYNCH Pulse Width	1	—	PCLK Cycle

4

Programmability

4.1 Programming Registers

MC149571 has programmable registers as shown in **Figure 4-1**. The registers provide system configurability for the supported major video functions.

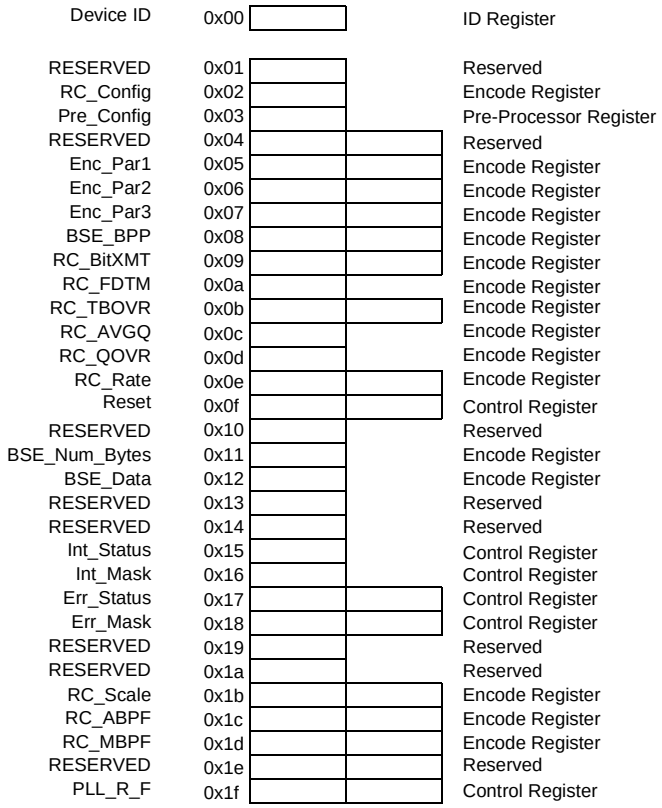

Figure 4-1. MC149571 Configuration Register Layout

4.2 Programmable Features

Table 4-1. MC149571 Programmable Features

Video Processing	Feature	Value
Pre-Processing	Noise Core Filtering	On or Off
	Picture Format to be captured	NTSC or PAL
Encoding	Encode Resolution	CIF or QCIF
	Bitstream Syntax	H.261 or H.263
	BCH Framing	On or Off
	Advanced Prediction Mode (APM)	On or Off
	Freeze Picture Release	On or Off
	Number of GOB Headers	Four options: every other, every fourth, all, and none
	Adjusted Quantization Target	1–31
	Minimum Picture Interval	0–31
	Intraframe Count	0–31
	Channel Bit Rate	(0–8191) * 64
PLL Programming	Clock Scalability	27 MHz–44 MHz

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