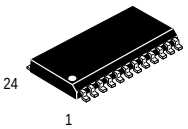
MC145173

Advance Information

Dual-Band PLL Frequency Synthesizer with ADC and Frequency Counter

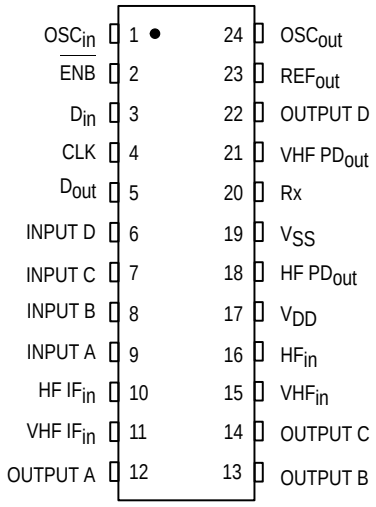
CMOS



DW SUFFIX
SOG PACKAGE
CASE 751E

ORDERING INFORMATION
MC145173DW SOG Package

PIN ASSIGNMENT



The MC145173 is a single–chip CMOS synthesizer with a four–wire serial interface for primary use in AM–FM broadcast receivers. The device also finds use in long–wave (LW) and short–wave (SW) receivers. Two inputs to a single high–speed N counter are provided, along with 2 phase detectors; one for a VHF loop up to 130 MHz, and another for an HF loop up to 40 MHz. The VHF phase detector has a current source/sink output and both detectors feature linear transfer functions (no dead zones). An external crystal ties across on–chip circuitry which drives a completely–programmable reference counter. Thus, a broad range of tuning resolution is possible. The crystal oscillator is buffered and fed to an open–drain output which is active in the HF mode only.

Due to the patented BitGrabber™ registers, address or steering bits are not needed in the serial data stream for random access of the registers. The serial port is byte–oriented to facilitate control via an MCU. Tuning across a band is accomplished with a two–byte transfer to the N register.

The 6–bit analog–to–digital converter (ADC) has two input channels. The converter is read via a one–byte transfer which includes an end–of–conversion (EOC) bit.

A 22–stage frequency counter is provided and accepts two IF (intermediate frequency) signals. Primary use for the frequency counter is for the seek or scan function on broadcast radio receivers. A proper frequency count ensures tuning of valid stations on their center frequencies. Reading the count is accomplished with a three–byte serial transfer which includes a count–complete (CC) bit.

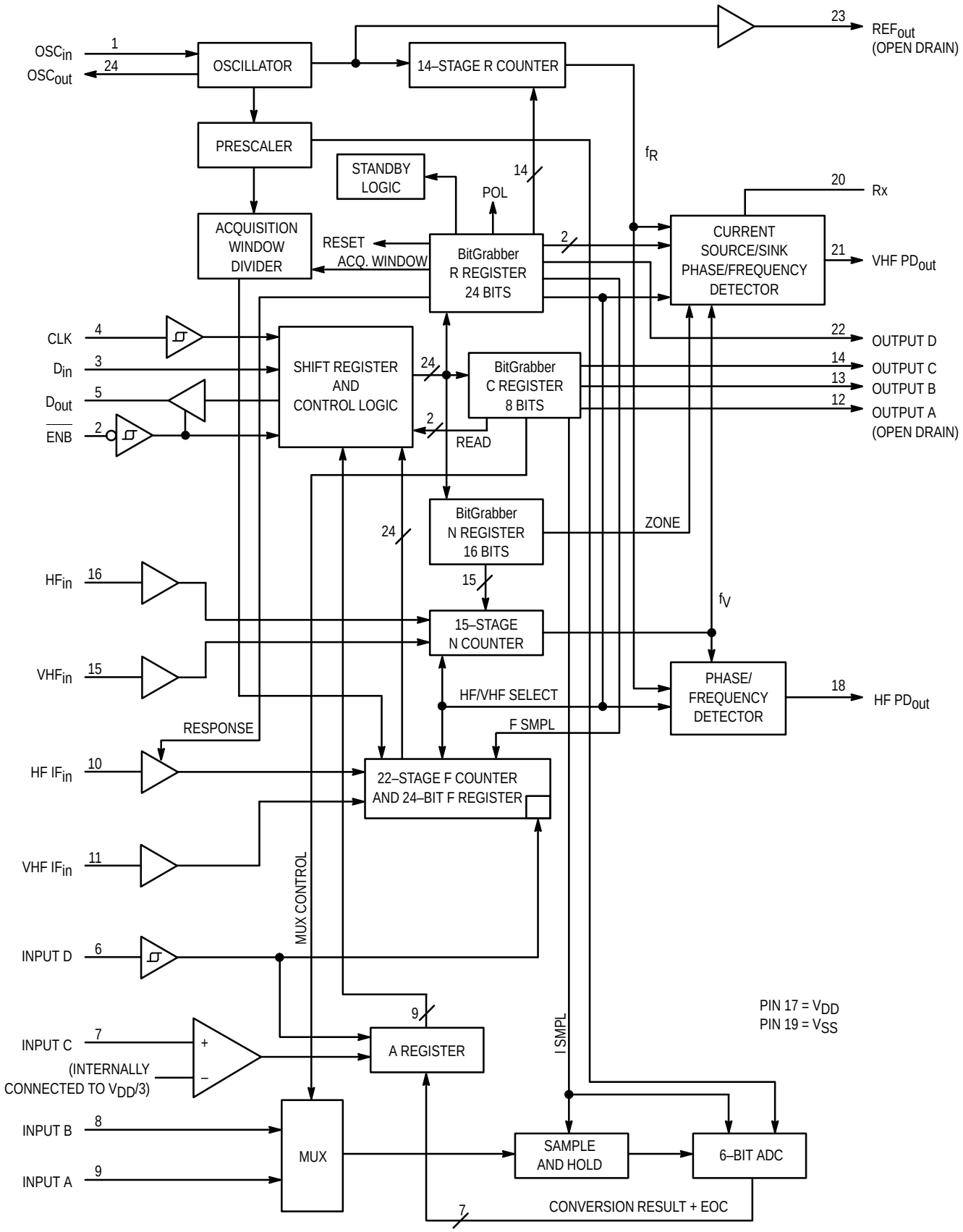
Four general purpose digital outputs are included. One of the outputs is open–drain; the others are totem–pole (push–pull). Two general purpose digital inputs are provided also. One input has a comparator with a switch point at 33% of V_{DD}.

- Operating Voltage Range: 4.5 to 5.5 V
- Maximum Operating Frequency: VHF_{in} = 130 MHz @ 210 mV p–p
  HF_{in} = 40 MHz @ 210 mV p–p
- Maximum Frequency of Reference Counter: 15 MHz
- Maximum Frequency of Frequency Counter: 20 MHz
- Maximum Supply Current: Operating Mode = 12 mA
  Standby Mode = 30 μA
- Approximate ADC Conversion Time: 360 μs
- Operating Temperature Range: – 40 to + 85°C
- R Counter Division Range: 1 and 5 to 16,383
- N Counter Division Range: 40 to 32,767
- Accommodates Downconversion or Upconversion Receiver Design for AM Broadcast Band
- Direct Interface to Motorola SPI Data Port
- Programmer's Guide Included in Datasheet

BitGrabber is a trademark of Motorola, Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

For proper termination of unused pins, see the Pin Descriptions section.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, Voltages Referenced to V_{SS}, T_A = –40 to +85°C)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		0.25 x V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		0.65 x V_{DD}	V
V_{IL}	Maximum Low–Level Input Voltage (Input D, HF IF_{in}, VHF IF_{in}, HF_{in}, VHF_{in}, OSC_{in})	dc coupled	0.3 x V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (Input D, HF IF_{in}, VHF IF_{in}, HF_{in}, VHF_{in}, OSC_{in})	dc coupled	0.7 x V_{DD}	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		0.3	V
V_{TH}	Threshold Voltage (INPUT C)	V_{in} Ramped Down from V_{DD}	0.28 x V_{DD} to 0.38 x V_{DD}	V
V_{OL}	Maximum Low–Level Output Voltage (D_{out}, OUTPUT A, OUTPUT B, OUTPUT C, OUTPUT D, HF PD_{out})	I_{out} = 20 μA	0.1	V
V_{OH}	Minimum High–Level Output Voltage (D_{out}, OUTPUT B, OUTPUT C, OUTPUT D, HF PD_{out}, REF_{out})	I_{out} = –20 μA	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (HF PD_{out})	V_{out} = 0.4 V	0.36	mA
I_{OH}	Minimum High–Level Output Current (HF PD_{out})	V_{out} = V_{DD} – 0.4 V	– 0.36	mA
I_{OL}	Minimum Low–Level Output Current (D_{out})	V_{out} = 0.4 V	1.6	mA
I_{OH}	Minimum High–Level Output Current (D_{out})	V_{out} = V_{DD} – 0.4 V	– 1.6	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT B, OUTPUT C, OUTPUT D)	V_{out} = 1.0 V	2.0	mA
I_{OH}	Minimum High–Level Output Current (OUTPUT B, OUTPUT C, OUTPUT D)	V_{out} = V_{DD} – 1.0 V	– 2.0	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT A)	V_{out} = 1.0 V	2.0	mA
I_{OH}	Minimum High–Level Output Current (REF_{out})	V_{out} = V_{DD} – 1.0 V	– 1.75	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, ENB, OSC_{in}, INPUT A, INPUT B, INPUT C, INPUT D)	V_{in} = V_{DD} or V_{SS}, Device NOT in Standby**	± 1.0	μA
I_{in}	Maximum Input Current (HF_{in}, VHF_{in}, HF IF_{in}, VHF IF_{in})	V_{in} = V_{DD} or V_{SS}, Device NOT in Standby	± 120	μA
I_{OZ}	Maximum Output Leakage Current (HF PD_{out})	V_{out} = V_{DD} or V_{SS}, Output in High–Impedance State	± 200	nA
I_{OZ}	Maximum Output Leakage Current (VHF PD_{out})	V_{out} = 1.75 or V_{DD} – 1.5 V, Output in High–Impedance State	± 200	nA
I_{OZ}	Maximum Output Leakage Current (REF_{out}, OUTPUT A, D_{out})	V_{out} = V_{DD} or V_{SS}, Output in High–Impedance State	± 2	μA

Continued on next page.

** While in Standby, the OSC_{in} pin is pulled low by a weak on–chip FET.

DC ELECTRICAL CHARACTERISTICS (continued) (V_{DD} = 4.5 to 5.5 V, Voltages Referenced to V_{SS}, T_A = –40 to +85°C)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
I_{STBY}	Maximum Standby Supply Current	V_{in} on D_{in}, CLK, INPUT A, INPUT B, INPUT C, INPUT D = V_{DD} or V_{SS}; V_{in} on ENB = V_{DD}; V_{in} on OSC_{in}, HF IF_{in}, VHF IF_{in} = V_{SS} or Floating (ac coupled); V_{in} on HF_{in} = V_{DD} or V_{SS} or Floating (ac coupled); V_{in} on VHF_{in} = Floating (ac coupled); D_{out} tied to V_{DD} or V_{SS} through 100 kΩ resistor; Other Outputs Open	30	μA
I_{dd}	Maximum Operating Supply Current	V_{in} on D_{in}, CLK, INPUT A, INPUT B, INPUT C, INPUT D = V_{DD} or V_{SS}; D_{out} tied to V_{DD} or V_{SS} through 100 kΩ resistor; V_{in} on ENB = V_{DD}; OSC_{in} = 10.35 MHz @ 1 V p–p; VHF_{in} = 120 MHz @ 210 mV p–p; VHF IF_{in} = 10.7 MHz @ 210 mV p–p	12	mA

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUT — VHF PD_{out}
($I_{out} \leq$ 2.5 mA, V_{DD} = 4.5 to 5.5 V, Voltages Referenced to V_{SS})

Parameter	Test Condition	Guaranteed Limit	Unit
Maximum Source Current Variation (Part–to–Part)	V_{out} = 0.5 x V_{DD}	± 20	%
Maximum Sink–vs–Source Mismatch (Note 3)	V_{out} = 0.5 x V_{DD}	12	%
Output Voltage Range (Note 3)	I_{out} variation ≤ 20%	1.25 to V_{DD} – 1.25 V	V

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor value.
3. This parameter is guaranteed for any specific temperature within – 40 to + 85°C.

ADC CHARACTERISTICS (T_A = – 40 to 85°C, V_{DD} = 4.5 to 5.5 V, f_{OSC} = 9.5 to 10.4 MHz)

Parameter	Test Condition	Guaranteed Limit	Unit
Resolution		6	Bits
Conversion Time	Per Figure 1	3584	OSC_{in} Cycles
Maximum Nonlinearity	V_{in} = V_{SS} + (0.1 x V_{DD}) to V_{DD} – (0.09 x V_{DD})	±1.5	LSBs

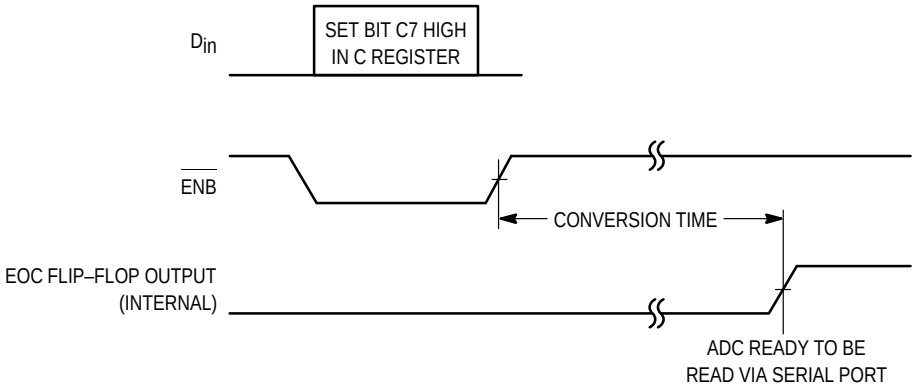


Figure 1.

AC INTERFACE CHARACTERISTICS

(V_{DD} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure #	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to CLK t_w below)	2	dc to 2.1	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to D_{out}	2, 8	150	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to Output B, Output C, Output D	6, 8	300	ns
t_{PLZ}, t_{PZL}	Maximum Propagation Delay, $\overline{ENB}$ to Output A	7, 9	300	ns
t_{PLZ}, t_{PHZ}	Maximum Disable Time, D_{out} Active to High Impedance	3, 9	400	ns
t_{PZL}, t_{PZH}	Access Time, D_{out} High Impedance to Active	3, 9	0 to 200	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, D_{out} CL = 50 pF	2, 8	100	ns
	CL = 200 pF	2, 8	400	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		10	pF
C_{out}	Maximum Output Capacitance – D_{out}		10	pF

TIMING REQUIREMENTS (T_A = – 40 to + 85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure #	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	4	100	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	5	200	ns
$t_{w(H)}$	Minimum Inactive–High Pulse Width, $\overline{ENB}$	5	600	ns
t_w	Minimum Pulse Width, CLK	2	238	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK (Source Impedance ≤ 5 kΩ)	2	50	µs

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = – 40 to + 85°C)

Symbol	Parameter	Test Condition	Figure #	Guaranteed Range		Unit
				Min	Max	
f_{in}	Input Frequency, HF_{in}	V_{in} ≥ 210 mV p–p Sine Wave, N Counter set to divide ratio such that f_V ≤ 1 MHz (Note 1)	10	10 (Note 4)	40	MHz
		V_{in} ≥ 2.2 V p–p Sine Wave, N Counter same as above	10	1	40	MHz
f_{in}	Input Frequency, VHF_{in}	V_{in} ≥ 210 mV p–p Sine Wave, N Counter set to divide ratio such that f_V ≤ 1 MHz (Note 1)	11	40 (Note 4)	130	MHz
f_{in}	Input Frequency, OSC_{in} Externally driven with ac–coupled signal (Note 2)	V_{in} ≥ 1.0 V p–p Sine Wave, R Counter set to divide ratio such that f_R ≤ 1 MHz (Note 3)	12	2 (Note 4)	15	MHz
f_{XTAL}	Crystal Frequency, OSC_{in} and OSC_{out} (Note 2)	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance, R Counter set to divide ratio such that f_R ≤ 1 MHz (Note 3)	13	2	15	MHz
f_{in}	Input Frequency, HF IF_{in}	V_{in} ≥ 85 mV p–p Sine Wave, K bit cleared low or set high	10	400	500	kHz
f_{in}	Input Frequency, VHF IF_{in}	V_{in} ≥ 85 mV p–p Sine Wave	10	8 (Note 4)	20	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 20 pF, V_{out} ≥ 1.5 V p–p	14, 15	dc	10.4	MHz

NOTES:
1. f_V is the output signal of the N Counter.
2. The ADC is guaranteed over an OSC_{in} range of 9.5 to 10.4 MHz only.
3. f_R is the output signal of the R Counter.
4. For operation below this frequency, use dc coupling with a signal level of at least V_{IL} to V_{IH}. See Pin Description.

SWITCHING WAVEFORMS

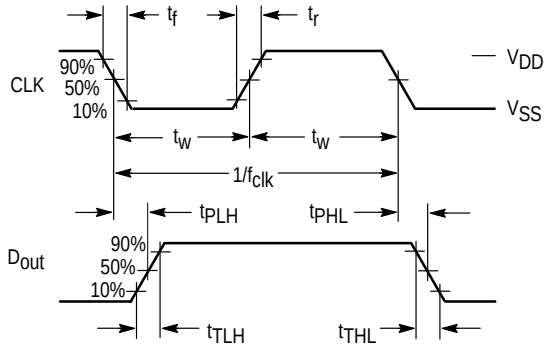


Figure 2.

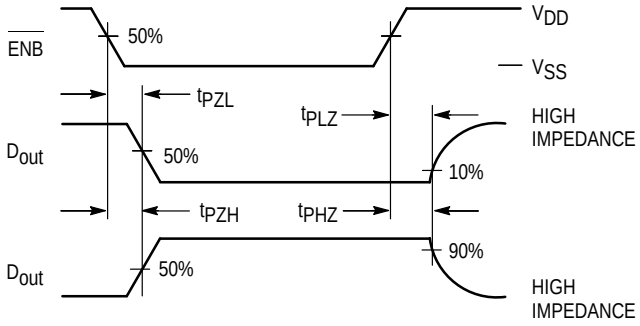


Figure 3.

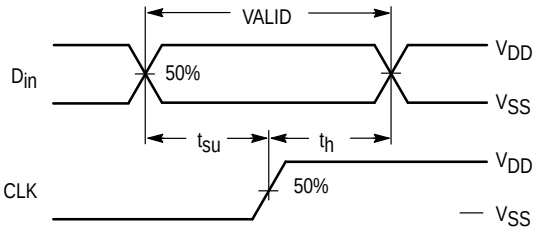


Figure 4.

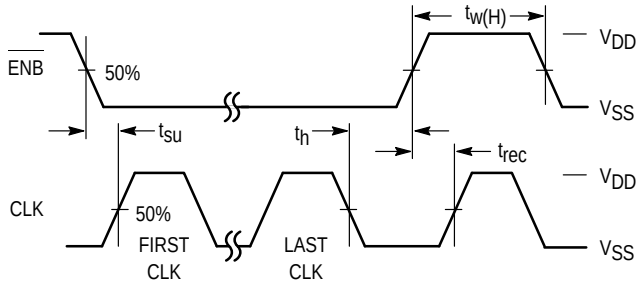


Figure 5.

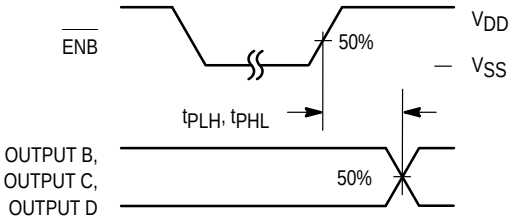


Figure 6.

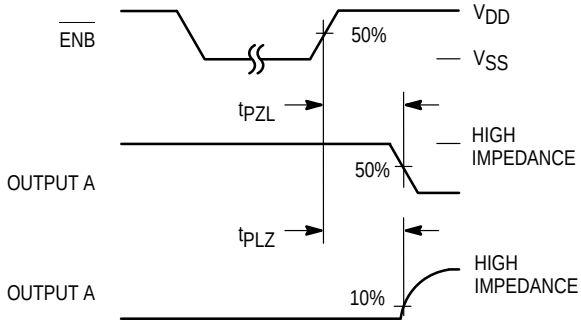
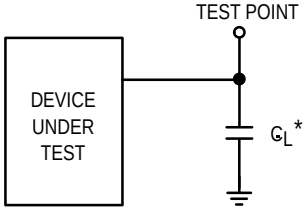
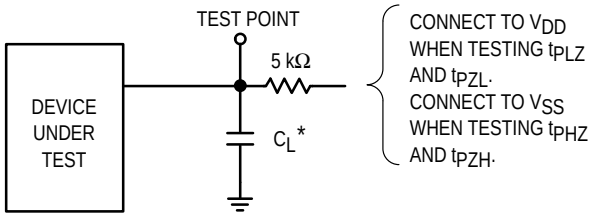


Figure 7.



*Includes all probe and fixture capacitance.

Figure 8. Test Circuit



*Includes all probe and fixture capacitance.

Figure 9. Test Circuit

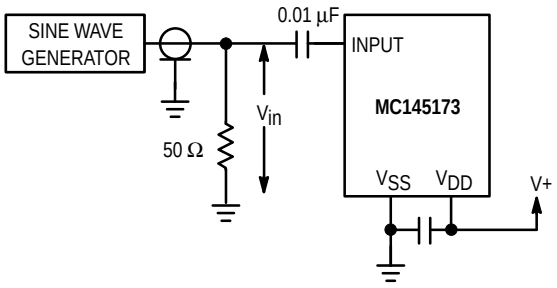


Figure 10. Test Circuit

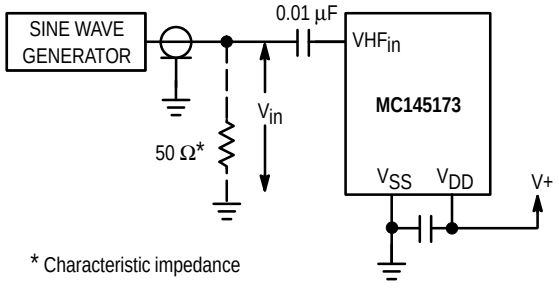


Figure 11. Test Circuit

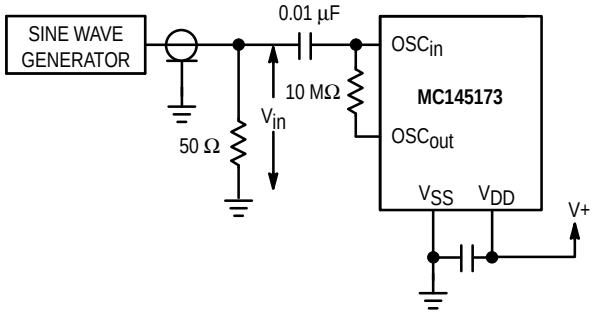


Figure 12. Test Circuit

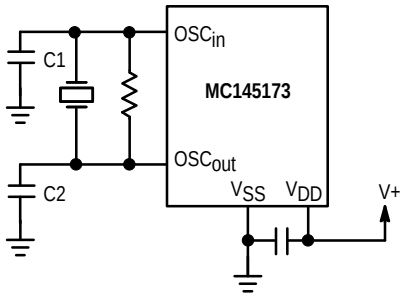


Figure 13. Test Circuit

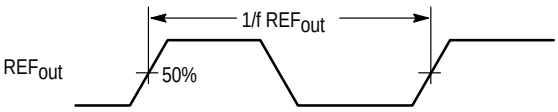


Figure 14. Switching Waveform

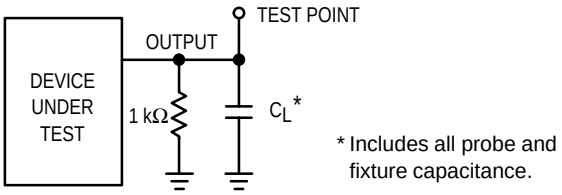


Figure 15. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 3)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. (See Table 1.) The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by ENB.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 4.5 to 5.5 V. The formats are shown in Figures 17, 18, and 20.

D_{in} typically switches near 45% of V_{DD} for good noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1Write–Only Registers
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
24	R Register	R23, R22, R21, . . ., R0
Other Values ≤ 32	Not Allowed	
Values > 32	Not Allowed	

Table 2Read–Only Registers
(MSBs are shifted out first; A7 and F23 are the MSBs)

Number of Clocks	Register	Bit Nomenclature
8, 9, or 16	A Register	A7, A6, A5, . . ., A0, A#
24	F Register	F23, F22, F21, . . ., F0

CLK
Serial Data Clock Input (Pin 4)

Low–to–high transitions on Clock shift bits available at D_{in}, while high–to–low transitions shift bits from D_{out}. The chip's 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. 24 cycles are used to access the R register. (See Table 1 and Figures 17, 18, and 20.)

The A register is read using 8, 9, or 16 clock cycles. The F register is read using 24 clocks. (See Table 2 and Figures 21 and 22.)

CLK typically switches near 45% of V_{DD} and has a Schmitt–triggered input buffer. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. That is, the CLK input should not be floated or toggled while the V_{DD} pin is ramping from 0 to at least 4.5 V. If control of the CLK pin is not practical during power up, then the RST bit in the R Register must be utilized. See the R Register Bits section.

$\overline{ENB}$
Active–Low Enable Input (Pin 2)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When ENB is in an inactive high state, shifting is inhibited, D_{out} is forced to the high–impedance state, and the port is held in the initialized state. To transfer data to and from the device, ENB (which must start inactive high) is taken low, a serial transfer is made via D_{in}, D_{out}, and CLK, and ENB is taken back high. The low–to–high transition on ENB transfers data to the C, N, or R write–only registers depending on the data stream length per Table 1.

To minimize standby current, $\overline{ENB}$ must be high.

$\overline{\quad}$CAUTION

Transitions on ENB must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when ENB is high and CLK is low.

This input is also Schmitt–triggered and switches near 45% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

D_{out}
Three–State Serial Data Output (Pin 5)

Data is transferred out of the 24–1/2 stage shift register through D_{out} on the high–to–low transition of CLK. The bit stream begins with the MSB. The bit pattern is 1 byte, 9 bits, or 2 bytes long to read the A register. The F register's data is contained in 3 bytes. (See Table 2.)

Before the A register can be read, the Read A bit must be set in the C register. Likewise, the Read F bit must be set to read the F register.

To minimize supply current during the standby state, the D_{out} pin should not be floated. A pull–down resistor to V_{SS} or pull–up resistor to V_{DD} should be used. The value can be 50 kΩ to 100 kΩ.

GENERAL–PURPOSE DIGITAL I/O PINS

Input C
Digital Input (Pin 7)

Input C is a general–purpose digital input which may be used for MCU port expansion. The state of this input is indicated by the In C bit in the A register. (See Figure 21.)

The switch point is precisely controlled by use of a comparator. The reference for the comparator is internally set to approximately 33% of V_{DD}. The input has a small amount of hysteresis voltage (approximately 50 mV).

If not used, this pin should be tied to V_{DD} or V_{SS}.

Input D
Digital Input (Pin 6)

Input D is a general–purpose digital input which may be used for MCU port expansion. The state of this input is indicated by the In D bit in both the A and F registers. That is, the state of the pin may be read from either register. (See Figures 21 and 22.)

This pin is a standard CMOS input with a switch point at approximately 50% of V_{DD}. Input D has a hysteresis voltage of approximately 600 mV.

If not used, this pin should be tied to V_{DD} or V_{SS}.

Output A
Open–Drain Digital Output (Pin 12)

Output A is a general–purpose digital output which may be used for MCU port expansion. An N–channel MOSFET tied to V_{SS} is used to drive this open–drain output. Thus, an external pull–up device is required at this pin. The state of this output is determined by the Out A bit in the C register. (See Figure 17.)

Upon power–up, this pin is low. If not used, Output A should be tied to V_{SS} or floated.

Output B
Digital Output (Pin 13)

Output B is a general–purpose digital output which may be used for MCU port expansion. This is a standard totem–pole (push–pull) CMOS output. The state of this output is determined by the Out B bit in the C register. (See Figure 17.)

Upon power–up, this pin is low. If not used, Output B should be floated.

Output C
Digital Output (Pin 14)

Output C is a general–purpose digital output which may be used for MCU port expansion. This is a standard totem–pole (push–pull) CMOS output. The state of this output is determined by the Out C bit in the C register. (See Figure 17.)

Upon power–up, this pin is low. If not used, Output C should be floated.

Output D
Digital Output (Pin 22)

Output D is a general–purpose digital output which may be used for MCU port expansion. This is a standard totem–pole (push–pull) CMOS output. The state of this output is determined by the Out D bit in the R register. (See Figure 18.)

Upon power–up, this pin is low. If not used, Output D should be floated.

ADC INPUT PINS

Input A, Input B
Analog Inputs (Pins 9, 8)

These are inputs to the 2–channel multiplexer which feeds the 6–bit analog–to–digital converter (ADC). The selected channel is determined by the Chan bit in the C register.

Each pin is a high–impedance input which appears as a mostly–capacitive load of approximately 6 pF.

If not used, these pins should be tied to V_{SS} or V_{DD}.

REFERENCE PINS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 1, 24)

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1 to 10 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The MC145173 is designed to operate with crystals from 2 to 15 MHz. However, frequencies are restricted to 9.5 to 10.4 MHz when the ADC is utilized. (See Figure 13.)

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01 μF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. The input capacitance of the OSC_{in} pin is approximately 6 pF. An external feedback resistor of approximately 10 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac–coupled case. (See Figure 12.) *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads in the HF mode.

The external signal level must be at least 1 V p–p; the minimum and maximum frequencies are given in the **AC Electrical Characteristics** table. These frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 1 MHz (Reason: the phase/frequency detectors are limited to a maximum input frequency of 1 MHz).

If an external source is available which swings from at least the V_{IL} to V_{IH} levels listed in the **DC Electrical Characteristics** table, then dc coupling can be used. In the dc–coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the MC145173, as noted above. For frequencies below 2 MHz, a signal level of at least V_{IL} and V_{IH} is needed, and dc coupling must be used. The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin at these low frequencies.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one. In the standby mode, OSC_{in} is pulled low by an on–chip FET.

REF_{out}
Open–Drain Reference Frequency Output (Pin 23)

This output is the buffered output of the crystal–generated reference frequency or externally provided reference source.

A P–channel MOSFET tied to V_{DD} is used to drive this open–drain output. Thus, an external pull–down device is required at this pin. This output is disabled and assumes the high–impedance state in the VHF mode per bit HF/VHF in the R register. (See Figure 18.)

REF_{out} is capable of operation to 10.4 MHz; see the **AC Electrical Characteristics** table.

If unused, the pin may be floated or tied to V_{DD}.

FREQUENCY COUNTER INPUT PINS

HF IF_{in}
HF Intermediate–Frequency Input (Pin 10)

This pin feeds an on–chip amplifier. The amp drives the F counter when the HF/VHF bit in the R register is low. (See Figure 18.) The signal driving this pin is normally sourced from the IF (intermediate frequency) circuit in the radio and is ac coupled. The input capacitance is approximately 6 pF.

This input is optimized for use with frequencies around 450 kHz. An on–chip low–pass filter is employed to roll off response above 1 MHz. In addition, for further suppression of high–frequency signals, the Kuligowski Acceptor Circuit may be engaged via the K bit in the R register. This is a digital integrator which allows acceptance of frequencies only below the frequency at the OSC_{in} pin divided by 8.

In the standby mode, HF IF_{in} is pulled low by an on–chip FET. If not used, this pin should be tied to V_{SS}.

VHF IF_{in}
VHF Intermediate–Frequency Input (Pin 11)

This pin feeds an on–chip amplifier. The amp drives the F counter when the HF/VHF bit in the R register is high. (See Figure 18.) The signal driving this pin is normally sourced from the IF circuit in the radio and is ac coupled. The input capacitance is approximately 6 pF. Usually, the frequency of the signal driving this pin is about 10.7 MHz.

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **DC Electrical Characteristics** table, dc coupling may be used. Also, for signals less than the minimum frequencies in the **AC Electrical Characteristics** table, dc coupling with at least V_{IL} and V_{IH} levels is a requirement. The F counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the VHF IF_{in} pin.

In the standby mode, VHF IF_{in} is forced to a high–impedence state. If not used, this pin should be tied to V_{SS}.

LOOP PINS

HF_{in}, VHF_{in}
High Frequency Input,
Very High Frequency Input (Pins 16, 15)

These pins feed on–chip amplifiers which drive the N counter; the HF/VHF bit in the R register determines which input is selected. (See Figure 18.) These signals are normally sourced from external voltage–controlled oscillators (VCOs), and are ac–coupled. (See Figures 10 and 11.) The input capacitance is approximately 6 pF. For small divide ratios, the maximum frequency is limited to the divide ratio times 1 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 1 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **DC Electrical Characteristics** table, dc coupling may be used. Also, for signals less than the minimum frequencies in the **AC Electrical Characteristics** table, dc coupling with at least V_{IL} and V_{IH} levels is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the HF_{in} and VHF_{in} pins.

Each rising edge on these pins cause the N counter to decrement by one.

In the standby mode, HF_{in} is forced to a high–impedence state, and VHF_{in} is pulled low by an on–chip FET. If not used, these pins should be tied to V_{SS}.

HF PD_{out}
Single–Ended Phase/Frequency Detector Output
(Pin 18)

This is a three–state output for use as a loop error signal when combined with an external low–pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (R23) in the R register = low (see Figure 18)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

POL bit (R23) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

This output is enabled and disabled via the HF/VHF bit in the R register. HF PD_{out} is forced to the high–impedance state when disabled. This pin should be floated when it is not used.

VHF PD_{out}
Single–Ended Phase/Frequency Detector Output
(Pin 21)

This is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (R23) in the R register = low (see Figure 18)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (R23) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state

Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output is enabled and disabled via the HF/VHF bit in the R register. VHF PD_{out} is forced to the floating state when disabled.

If not used, this pin should be a no connect.

Rx
External Resistor (Pin 20)

A resistor is tied between this pin and V_{SS}. This sets a reference current which determines the current delivered (I_{PDout}) at the current source/sink phase/frequency detector output, VHF PD_{out}. For a nominal current of 2.2 mA at the VHF PD_{out} pin, a 15 kΩ resistor is utilized.

In addition, the Rx pin must be bypassed to V_{DD} with a low–inductance 0.1 μF capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

If the VHF PD_{out} pin is not used, the Rx pin may be floated.

POWER SUPPLY

V_{DD}
Most–Positive Supply Potential (Pin 17)

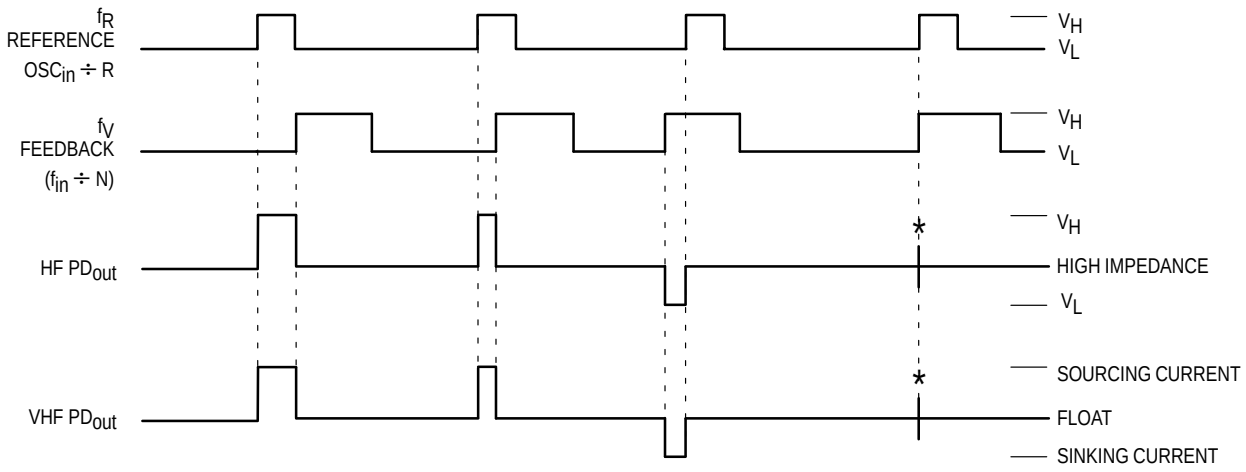
This pin may range from 4.5 to 5.5 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low–inductance capacitor(s) mounted very close to the MC145173. Lead lengths and traces to the capacitor(s) should be minimized. (The very fast switching speed of the device can cause excessive current spikes on the power leads if they are improperly bypassed.)

Power supply ramp up time should be less than 20 ms from 0 to 4.5 V. If the ramp up time exceeds 20 ms, the POR circuit may not function and the outputs will be in an unknown state. The RST bit must be used in this case.

V_{SS}
Most–Negative Supply Potential (Pin 19)

This pin is usually ground.



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, both the source and sink drivers are turned on for a short duration. For exceptions, see Figure 19.
NOTE: HF PD_{out} and VHF PD_{out} are shown with the polarity bit (POL) = low; see Figure 18 for POL.

Figure 16. Phase/Frequency Detectors Output Waveforms

C REGISTER BITS

I SMPL
Input Sample (C7)

When the input sample bit is cleared low, the ADC is held in the initialized state. When I SMPL is set high, the ADC converts the input channel selected by bit C4, and holds the conversion value. When the ADC is read via the serial port, I SMPL must remain high. Otherwise, the EOC bit is reset low. The previous converison value is not lost, however.

I SMPL may be set at any time, even if the F SMPL bit in the R register is already set. That is, an A/D conversion may be initiated during an F count. The state of C4 may not be changed simultaneously with C7 being set high.

I SMPL is cleared low upon power up. However, this bit is not automatically cleared low after a conversion and read sequence.

READ A
Read A Register (C6)

Setting the Read A register bit high causes the ADC's value and the states of Inputs C and D to be parallel loaded into the serial port's shift register. ENB is then taken low and either 8, 9, or 16 bits are shifted from the D_{out} pin. If only 8 bits are shifted, the state of Input D is not read. To read Input D, use either a 9 or 16 bit shift. (See Figure 21.) Alternatively, Input D may be read from the F Register.

While the Read A bit is set, writing to any register is inhibited. After the read occurs (A register data shifted out), C6 is automatically cleared low. When C6 is low, the shift register is not parallel loaded and any of the registers of Table 1 may be written.

Read A should not be set when Read F is set. If both Read A and Read F are set simultaneously, a *Read A Register* operation is performed and the *Read F Register* request is ignored.

Read A is cleared low at power up.

RESERVED
Reserved Bit (C5)

This bit must be kept low.

CHAN
Channel Select for ADC (C4)

When the channel bit is low, Input A is selected to be converted by the ADC. When the bit is high, Input B is selected. The state of C4 may not be changed simultaneously with the I SMPL bit being set high.

READ F
Read F Register (C3)

Setting the Read F register bit high causes the frequency counter's value and the state of Input D to be parallel loaded into the serial port's shift register. ENB is then taken low and 24 bits are shifted from the D_{out} pin. (See Figure 22.)

While the Read F bit is set, writing to any register is inhibited. After the read occurs (F register data shifted out), C3 is automatically cleared low. When C3 is low, the shift register is not parallel loaded and any of the registers of Table 1 may be written.

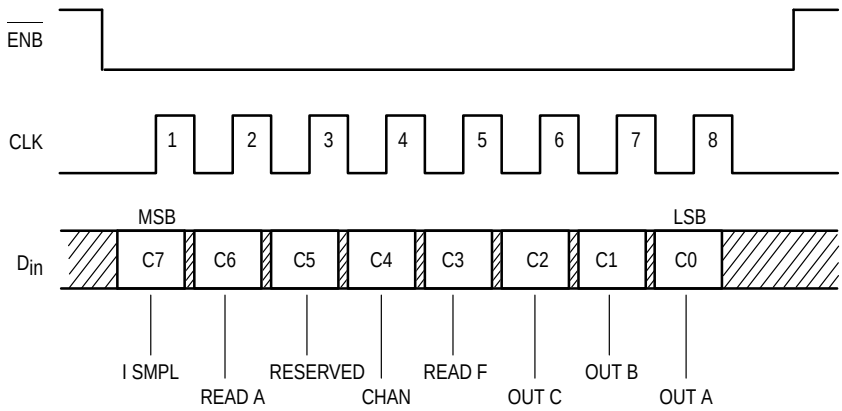
Read F should not be set when Read A is set. If both Read F and Read A are set simultaneously, a *Read A Register* operation is performed and the *Read F Register* request is ignored.

Read F is cleared low at power up.

OUT C, OUT B, OUT A
Output C, Output B, Output A Control (C2, C1, C0)

When Out A, Out B, or Out C is cleared low, the Output A, Output B, or Output C pins are forced low, respectively. When set high, the associated output is forced high, except for Output A which is forced to the high–impedance state.

These bits are cleared low at power up.



NOTE: This is a write–only register.

Figure 17. C Register Access and Format (8 Clock Cycles are Used)

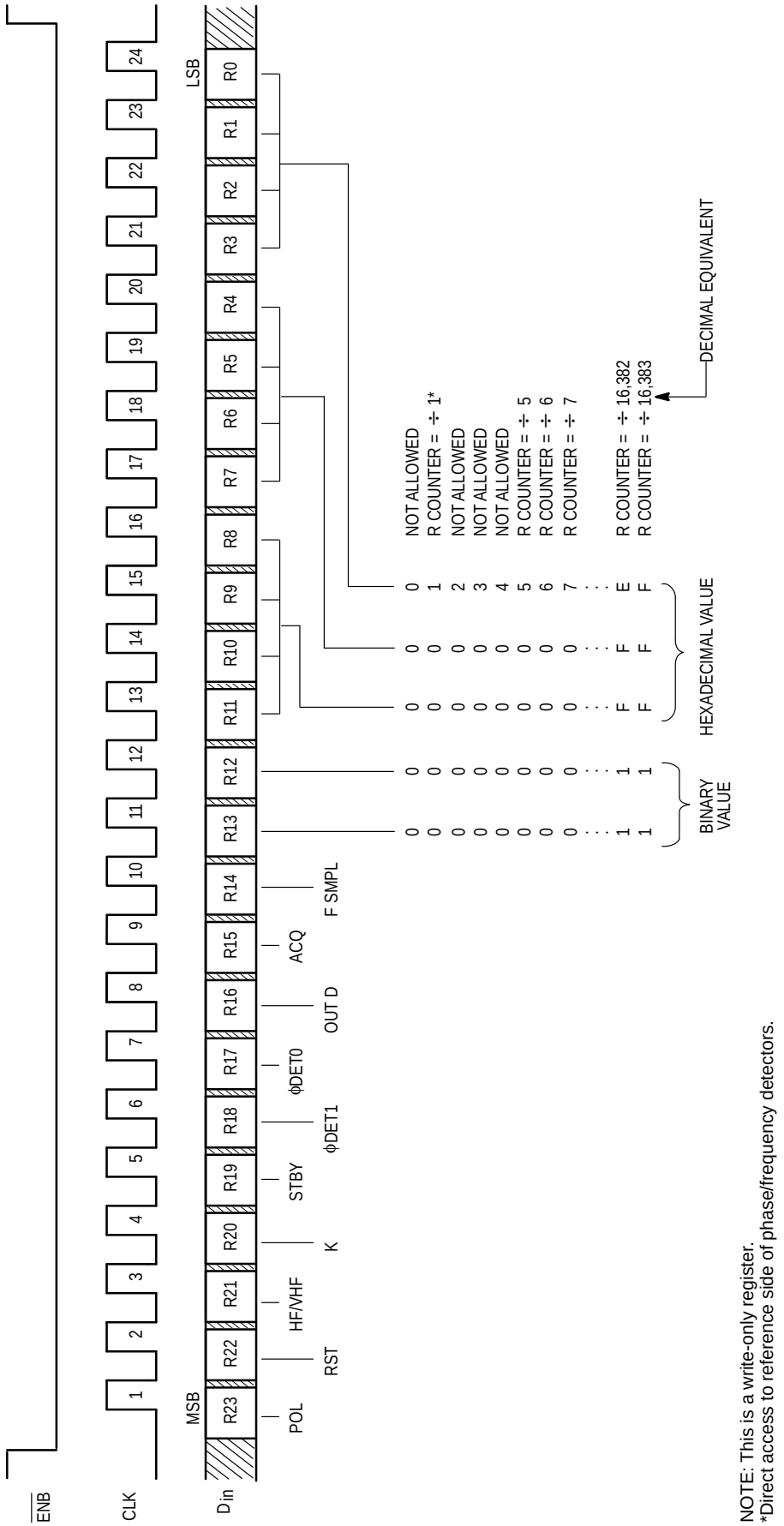


Figure 18. R Register Access and Format (24 Clock Cycles Are Used)

Do not attempt to write to the R register when both the F counter and A/D converter are simultaneously active.

POL
Polarity (R23)

The polarity bit controls both phase/frequency detector outputs. When low, the detector outputs are per Figure 16. When R23 is high, the output polarity of both phase/frequency detectors is inverted.

Upon power up, this bit is forced low.

RST
Reset (R22)

When high, this bit resets the device except for the serial port. RST is kept low for normal operation. However, if a power glitch occurs which does not reduce the power supply voltage to 0 volts, the R register should be written twice with the RST bit set high. Also, if the CLK pin is floating upon power up, the RST bit should be written high twice for initialization.

NOTE

The on–chip POR (power–on reset) circuit resets the device during a cold start, if the CLK pin is not floating or toggled during supply ramp up to 4.5 V.

This bit is automatically cleared low after the chip is reset.

HF/VHF
HF/VHF Band Selection (R21)

When this bit is low, the HF_{in} and HF IF_{in} inputs are enabled, along with the HF PD_{out} pin. The VHF PD_{out} pin is forced to the float condition and VHF_{in} is pulled low with an on–chip FET.

When this bit is high, the VHF_{in} and VHF IF_{in} inputs are enabled, along with the VHF PD_{out} pin. Both the HF PD_{out} and HF_{in} pins are forced to the high–impedance state, and REF_{out} is disabled (high–impedance).

K
HF IF_{in} Response (R20)

This bit is used to control the input response of the HF IF_{in} pin.

When the K bit is high, the Kuligowski acceptor circuit is engaged, which allows acceptance of signals only below the frequency at the OSC_{in} pin divided by 8. Use of this digital integrator allows further suppression of high–frequency signals into the HF IF_{in} pin.

In the VHF mode, the K bit should be kept low.

STBY
Standby (R19)

If STBY is low, the chip is in the normal mode of operation.

When this bit is high, the device is placed in the standby state for reduced power consumption. In standby, both phase/frequency detector outputs and the REF_{out} pin are forced to the high–impedance state, the Rx reference current is shut off, and the oscillator is stopped (via an on–chip FET pulling the OSC_{in} pin low). The HF_{in}, VHF_{in}, HF IF_{in}, and VHF IF_{in} inputs are shut off, which inhibits the counters from toggling. Finally, the comparator and ADC are turned off. Data is retained in the C, N, and R registers during standby.

CAUTION

Setting the STBY bit high aborts any frequency count or A/D conversion which may be in progress.

STBY is forced high upon power up.

ϕdet1, ϕdet0
Phase/Frequency Detector Response (R18, R17)

Controls the VHF phase/frequency detector response per Table 3. The HF phase/frequency detector is unaffected.

These bits also control several test modes as shown in Table 4.

Out D
Output D Control (R16)

When cleared low, the Output D pin is forced low. When high, Output D is high.

This bit is cleared low upon power up.

ACQ
Acquisition Window (R15)

This bit determines the frequency counter (F counter) acquisition window. A low level is for a narrow window, and a high is for a wide window.

The formula to determine the window is

$$t = \frac{2^{(19 + 2a)}}{f}$$

where t is the acquisition window in seconds, a is the logic level of the ACQ bit (0 or 1), and f is the frequency at the OSC_{in} pin in hertz.

F SMPL
Frequency Sample (R14)

When this bit is low, the frequency counter (F counter) is initialized to all highs (ones).

When F SMPL is set high, the frequency counter “rolls over” to zero, increments for one acquisition window, and then holds the count. When the frequency counter is read via the serial port, R14 must remain high; otherwise, the frequency counter is initialized and outputs all ones.

F SMPL must not be set high if I SMPL is already high. That is, a frequency count cannot be initiated if an A/D conversion is in progress.

This bit is cleared low upon power up. However, this bit is not automatically cleared low after a frequency count and read sequence.

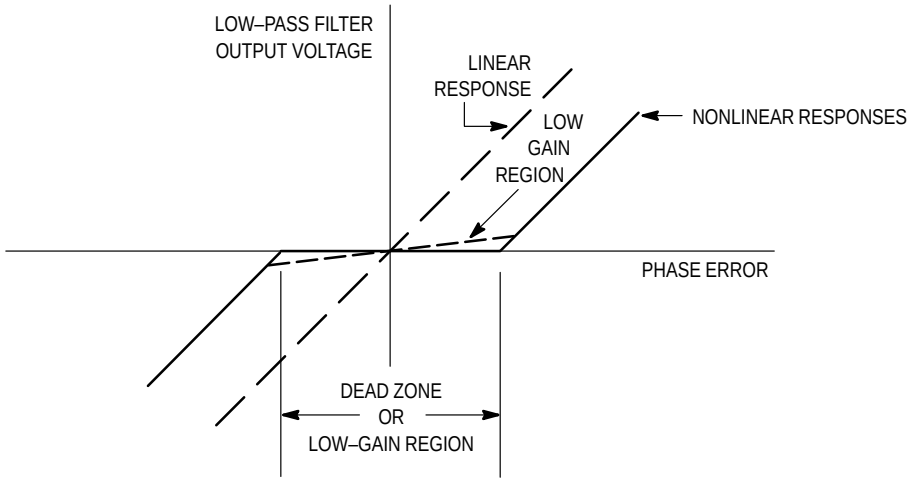
R13 to R0
R Counter Divide Ratio

These bits control the divide ratio of the R counter per Figure 18.

Table 3. VHF PD_{out} Response

N Register Bit	R Register Bits		
N15	R18	R17	VHF Phase Detector Response (Nominal)
L	L	L	Linear response, no low–gain region
L	L	H	Low–gain region, 5 ns wide
L	H	L	Low–gain region, 10 ns wide
L	H	H	Low–gain region, 15 ns wide
H	L	L	Linear response, no dead zone
H	L	H	Dead zone, 5 ns wide
H	H	L	Dead zone, 10 ns wide
H	H	H	Dead zone, 15 ns wide

NOTES:
1. L = Low Level, H = High Level.
2. See Figure 19.



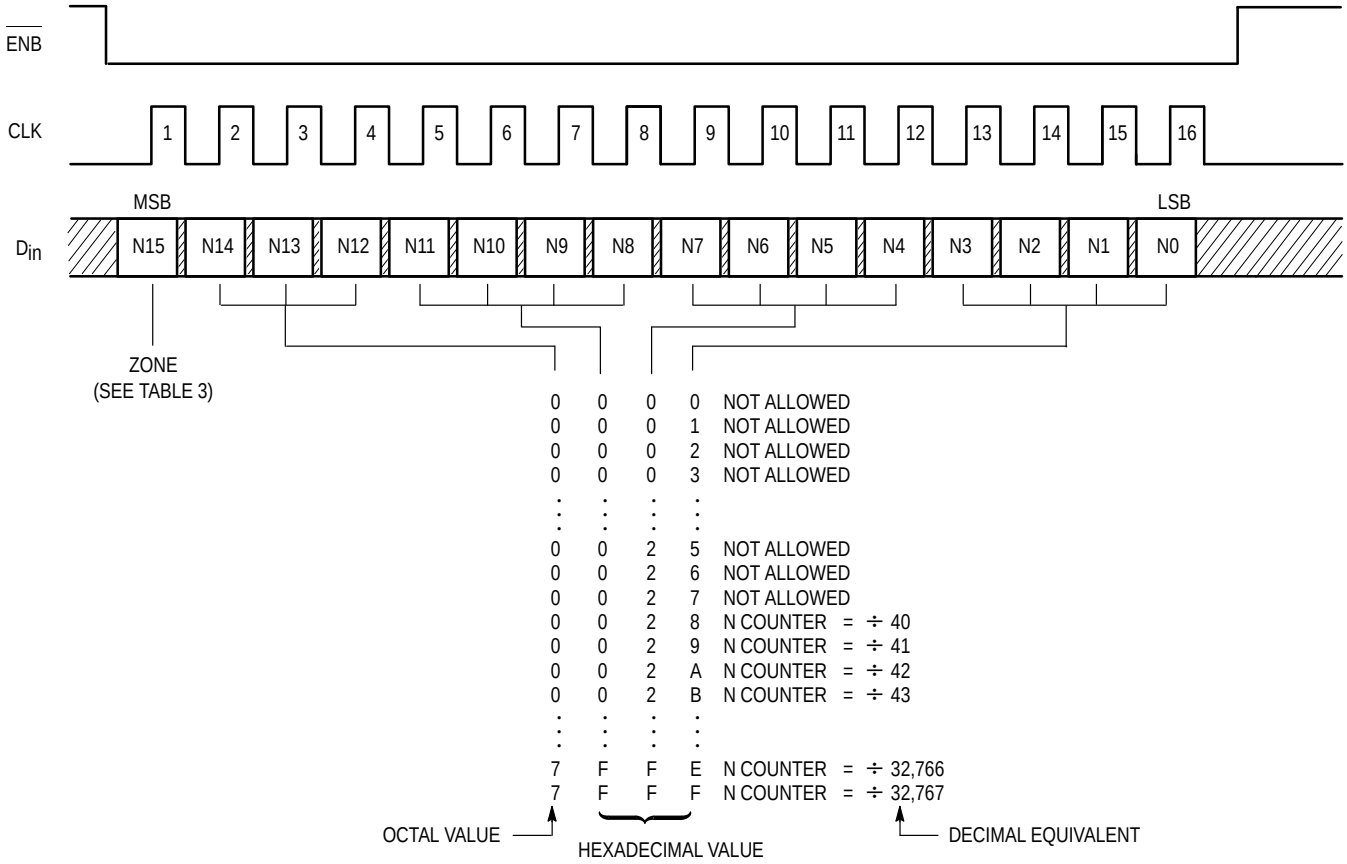
NOTES:
1. Output HF PD_{out} always has a linear transfer characteristic. Therefore, for HF PD_{out}, the Dead Zone = 0 ns.
2. Output VHF PD_{out} has a response which is programmable via bits ϕdet1 (R18), ϕdet0 (R17), and Zone (N15). See Table 3.
3. The gain in the “low–gain region” is reduced to 7% of the gain in the other region.

Figure 19. VHF PD_{out} Transfer Characteristic

Table 4. Test Modes

R Register Bits			Pin Configurations	
R21	R18	R17	Pin 12 — OUTPUT A	Pin 13 — OUTPUT B
L	L	L	OUTPUT A, normal configuration	OUTPUT B, normal configuration
L	L	H	f_V, N counter output — HF_{in} feeds the counter input	OUTPUT B, normal configuration
L	H	L	f_V, N counter output — VHF_{in} feeds the counter input	OUTPUT B, normal configuration
L	H	H	OUTPUT A, normal configuration	f_R, R counter output
H	X	X	OUTPUT A, normal configuration	OUTPUT B, normal configuration

NOTE: L = Low Level, H = High Level, X = Don’t Care.



NOTE: This is a write–only register.

Figure 20. N Register Access and Format (16 Clock Cycles Are Used)

A REGISTER BITS

EOC
End of Conversion (A7)

The end of conversion bit is set high when the analog–to–digital conversion is complete. This high level indicates that the A/D conversion value read via the serial port is valid.

EOC is cleared low when the I SMPL bit in the C register is cleared low.

IN C
Input C Level (A6)

In C indicates the state of the Input C pin. A high level on the Input C pin causes the In C bit to be high. A low level on the pin causes a low level to be read on In C. The digital value is stored at the falling edge of ENB on the read cycle.

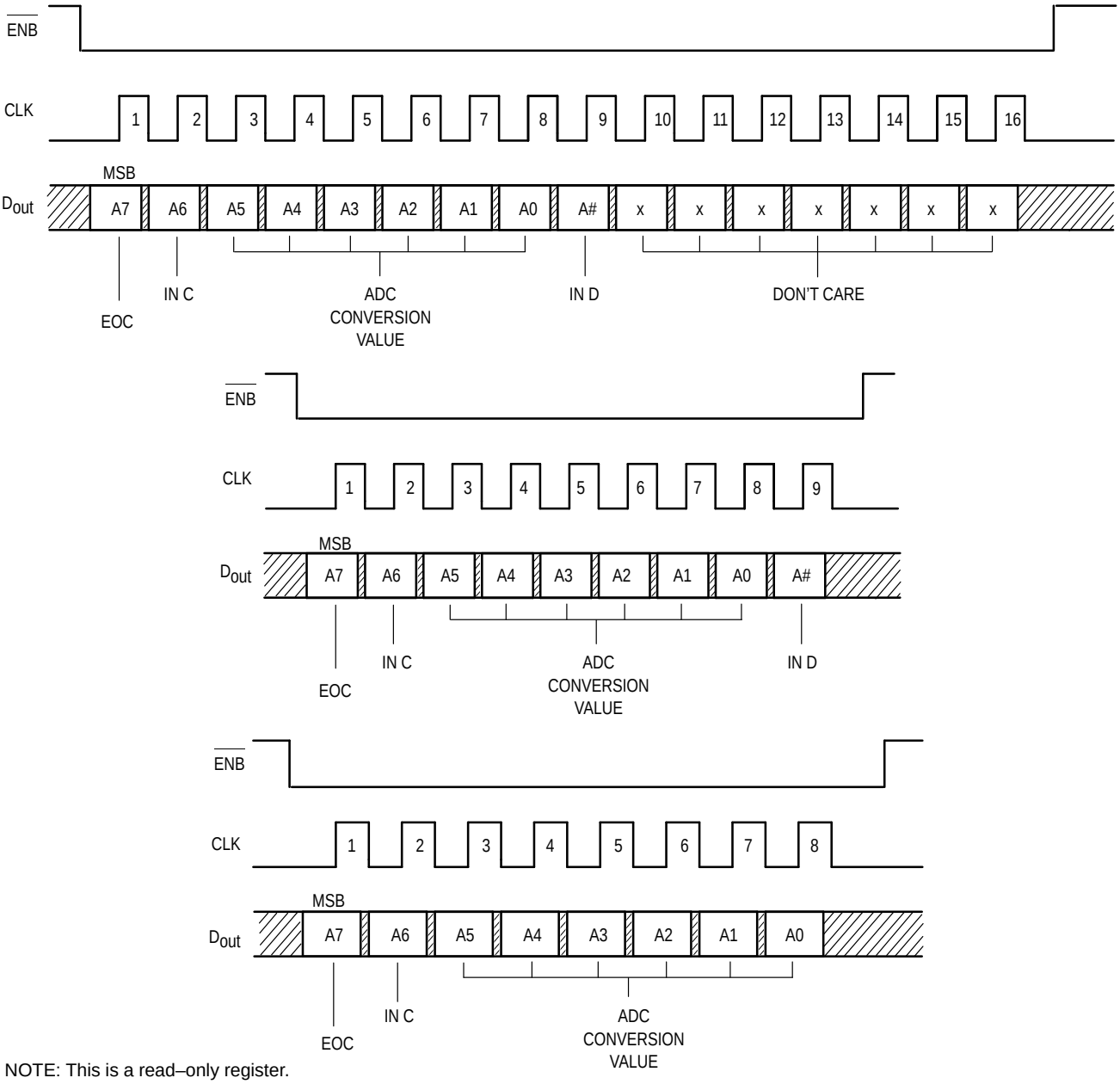
ADC CONVERSION VALUE
A/D Conversion Value (A5 – A0)

These bits contain the analog–to–digital conversion result in binary format. A5 is the MSB of the value; A0 is the LSB.

IN D
Input D Level (A#)

In D indicates the state of the Input D pin. A high level on the Input D pin causes the In D bit to be high. A low level on the pin causes a low level to be read on In D. The digital value is stored at the falling edge of ENB on the read cycle.

A 9– or 16–bit shift must be used to read the In D bit from the A register. Optionally, the In D bit may be read from the F register.



NOTE: This is a read–only register.

Figure 21. A Register Formats (8, 9, or 16 Clock Cycles May Be Used)

F REGISTER BITS

CC
Count Complete (F23)

The count complete bit is set high when the frequency counter has gone through a count cycle for a complete acquisition window. This high level indicates that the count read via the serial port is valid.

CC is cleared low when the F SMPL bit in the R register is cleared low.

IN D
Input D Level (F22)

In D indicates the state of the Input D pin. A high level on the Input D pin causes the In D bit to be high. A low level on the pin causes a low level to be read on In D.

Optionally, the In D bit may be read from the A register.

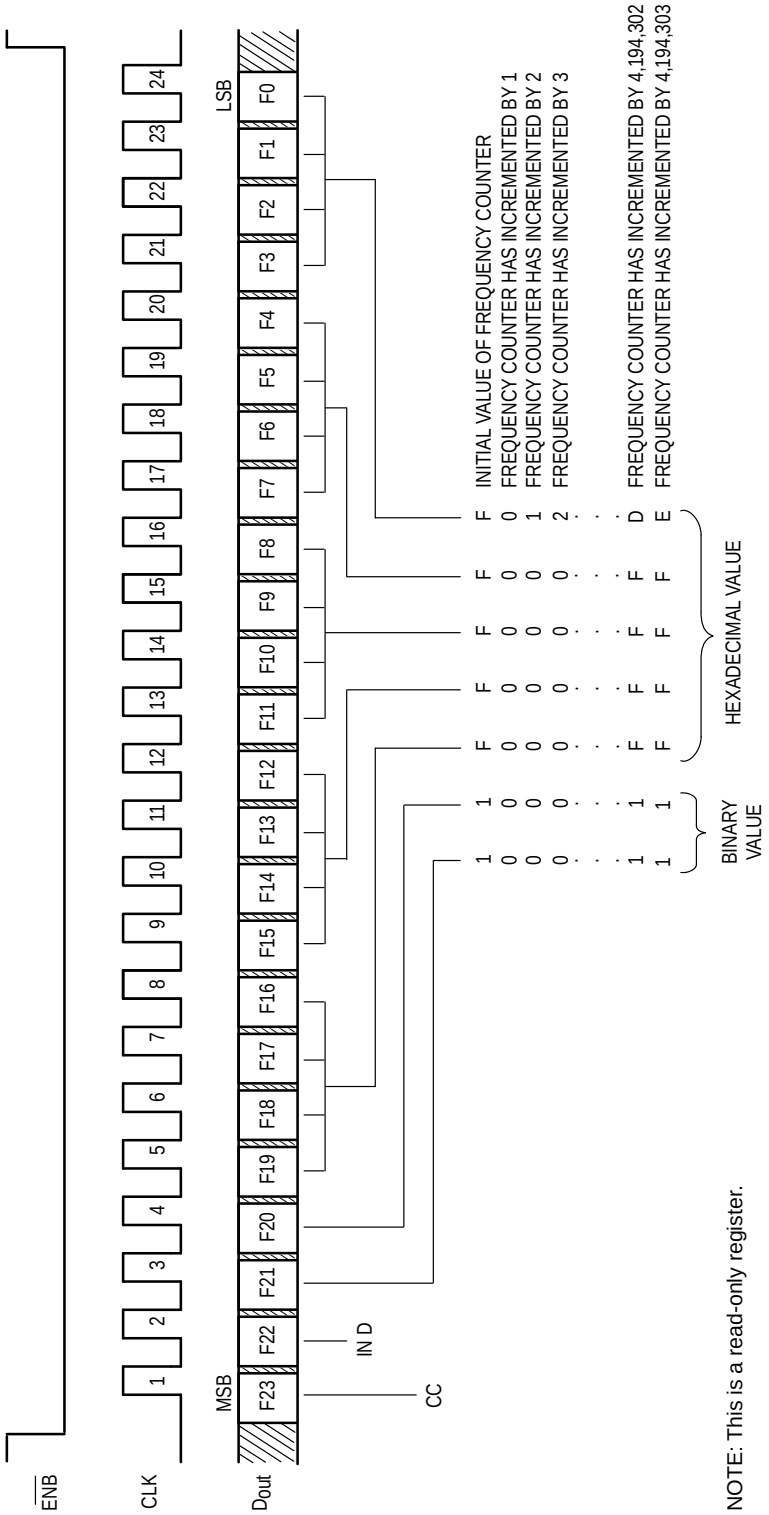


Figure 22. F Register Format (24 Clock Cycles Are Used)

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} must be used. (See Figure 12.)

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. (See Figure 12.) For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 23.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequency. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

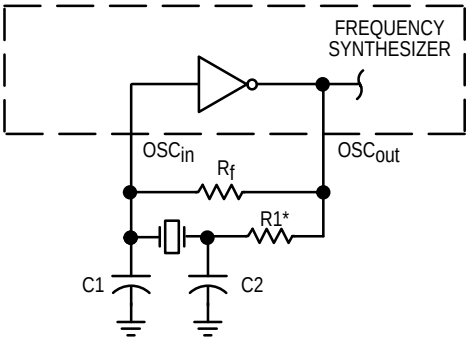
C_{in} = 6 pF (see Figure 24)
C_{out} = 6 pF (see Figure 24)
C_a = 1 pF (see Figure 24)
C1 and C2 = external capacitors (see Figure 23)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals (see Figure 24)

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 25. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 23 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the OSC_{out} pin. An active probe should be used to minimize loading. The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. (See Table 5)



*May be needed in certain cases. See text.

Figure 23. Pierce Crystal Oscillator Circuit

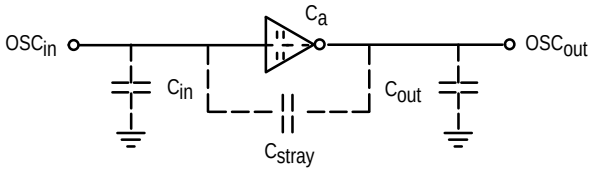
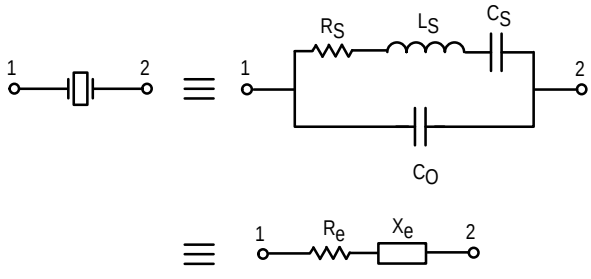


Figure 24. Parasitic Capacitances of the Amplifier and C_{stray}



Note: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 25. Equivalent Crystal Networks

Recommended Reading

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, “The Piezoelectric Crystal Unit–Definitions and Method of Measurement”, *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, “Quartz Crystals for Frequency Control”, *Electro–Technology*, June 1969.

P. J. Ottowitz, “A Guide to Crystal Selection”, *Electronic Design*, May 1966.

D. Babin, “Designing Crystal Oscillators”, *Machine Design*, March 7, 1985.

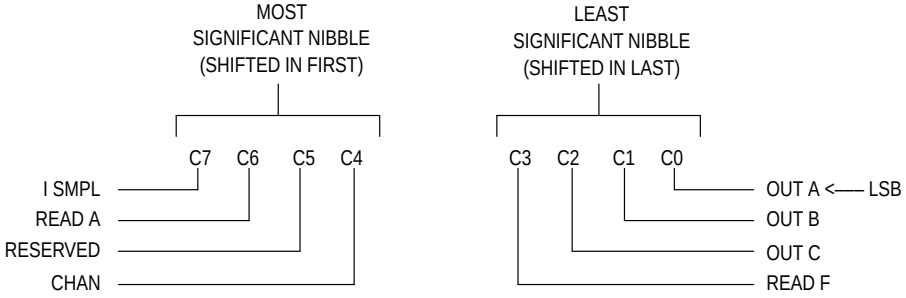
D. Babin, “Guidelines for Crystal Oscillator Design”, *Machine Design*, April 25, 1985.

Table 6. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693–0099

Note: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

C REGISTER
Write Only



I SMPL = Analog Input Sample Command
- 0 = Initialize the ADC
- 1 = Sample the voltage on the Input A or B pins (see Chan bit)

Read A = Read A Register Command
- 0 = Allow writes to any registers, normal state
- 1 = Read the Input A or B analog value* and the Input C and D digital values

Reserved = Reserved Bit
- 0 = (Must be in this state)
- 1 = (This state not allowed at this time, reserved)

Chan = Analog Channel Address
- 0 = Input A
- 1 = Input B

*6–bit analog–to–digital converter output value.

Out A = Output A Pin Logic State
- 0 = Pin is forced to a 0 (default)
- 1 = Pin is forced to the high–impedance state

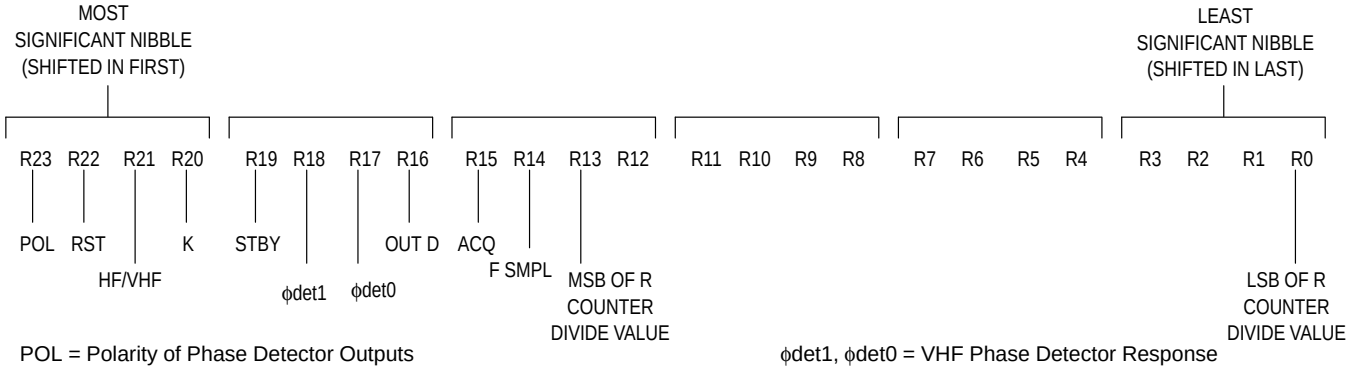
Out B = Output B Pin Logic State
- 0 = Pin is forced to a 0 (default)
- 1 = Pin is forced to a 1

Out C = Output C Pin Logic State
- 0 = Pin is forced to a 0 (default)
- 1 = Pin is forced to a 1

Read F = Read F Register
- 0 = Allow writes to any registers, normal state
- 1 = Read the Frequency Counter's value and Input D state

PROGRAMMER'S GUIDE (continued)

R REGISTER
Write Only



POL = Polarity of Phase Detector Outputs
0 = Normal (default)
1 = Inverted

RST = Reset
0 = Normal
1 = Reset the chip (automatically cleared low)
Suggestion: set to 1 after power glitch

HF/VHF = HF or VHF Band Select
0 = HF_{in}, HF IF_{in}, and HF PD_{out} pins are activated (default)
1 = VHF_{in}, VHF IF_{in}, and VHF PD_{out} pins are activated

K = HF IF_{in} Input Response
0 = Normal (must be 0 when VHF band is selected)
1 = Engage Acceptor Circuit

STBY = Standby
0 = Normal
1 = Low–Power Standby State

ϕdet1, ϕdet0 = VHF Phase Detector Response
0, 0 = Linear Response
0, 1 = Low–Gain Region or Dead Zone – 5 ns wide
1, 0 = Low–Gain Region or Dead Zone – 10 ns wide
1, 1 = Low–Gain Region or Dead Zone – 15 ns wide

Out D = Output D Pin Logic State
0 = Pin is forced to a 0 (default)
1 = Pin is forced to a 1

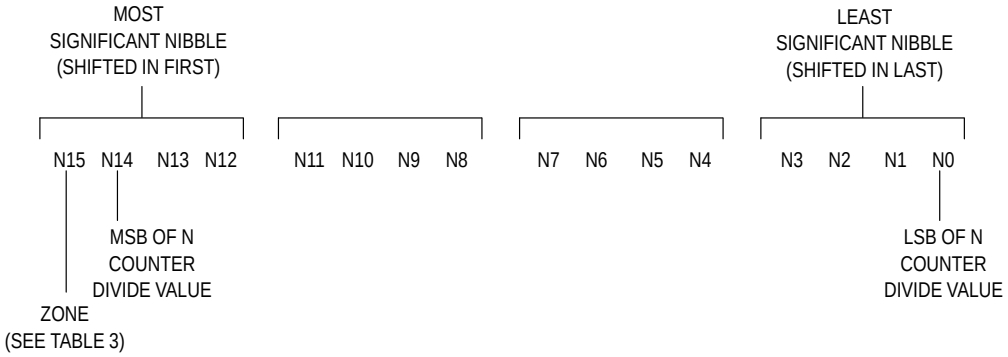
ACQ = Acquisition Window
0 = Narrow Sample Window
1 = Wide Sample Window

F SMPL = Frequency Counter Sample Command
0 = Initialize Counter to all 1's (default)
1 = Sample the Frequency at HF IF_{in} or VHF IF_{in} pins

Example:
To program the R Counter to divide by 1000 in decimal, first convert to hexadecimal: $3E8. Then, add leading bits to form 3 bytes (6 nibbles). The leading bits should be adjusted to control the above functions. Finally, load the R Register.

CAUTION:
When both the A/D converter and F Counter are simultaneously active, a write to the R Register causes the F Counter operation to abort.

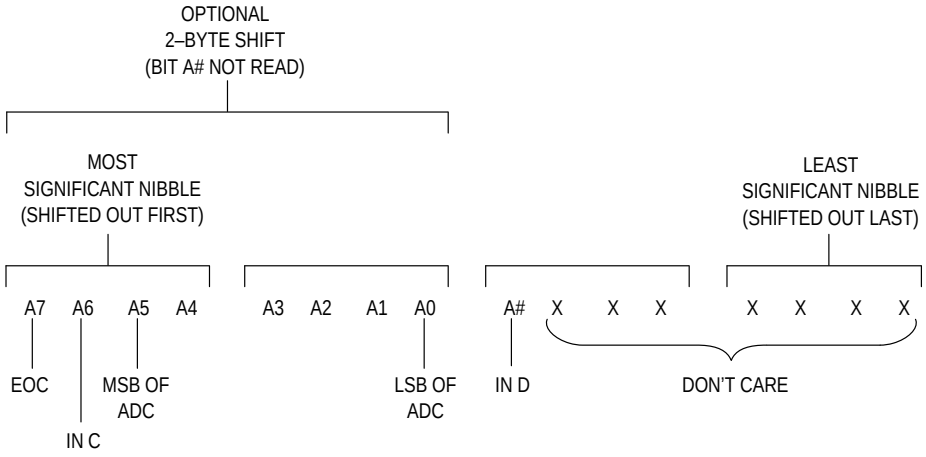
N REGISTER
Write Only



Example:
To program the N Counter to divide by 1000 in decimal, first convert to hexadecimal: $3E8. Then, add leading zeroes to form 2 bytes (4 nibbles): $03E8. Finally, Load the N Register with $03E8.

NOTE:
The chip's VHF PD_{out} is controlled by bit N15 as follows: low = low–gain region, high = dead zone. See Figure 19.

A REGISTER
Read Only



EOC = End of Conversion
0 = Invalid ADC Results (also, this bit is 0 when the ADC is in the initialized state)
1 = A/D Conversion Complete, Results are Valid

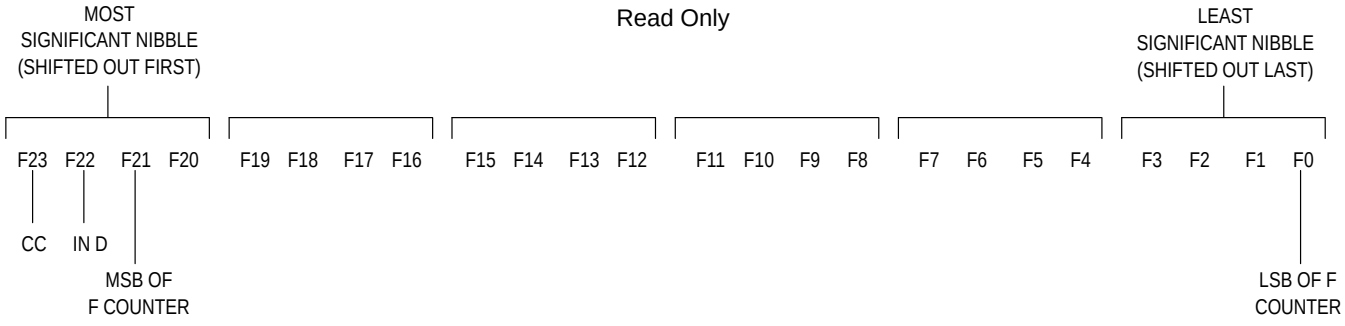
IN C = Input C Pin Status
0 = Pin is a Logic 0
1 = Pin is a Logic 1

MSB to LSB of ADC = Binary Representation of the 6–Bit Conversion value
For example, zero is 000000, full scale is 111111 in binary.

IN D = Input D Pin Status
0 = Pin is a Logic 0
1 = Pin is a Logic 1

Example:
To read just the ADC value, the user may shift out 1 byte. The ADC value is contained in the 6 LSBs. If the MSB is a 1, this indicates that the conversion is complete and the results are valid. The MSB – 1 is the Input C pin value.
A 2–byte shift allows reading the In D bit in addition to the above. (In D is also contained in the F Register.) As illustrated above, the MSB is the EOC bit, and the 7 LSBs are don't care bits. A 9–bit shift also allows reading the In D bit.

F REGISTER
Read Only

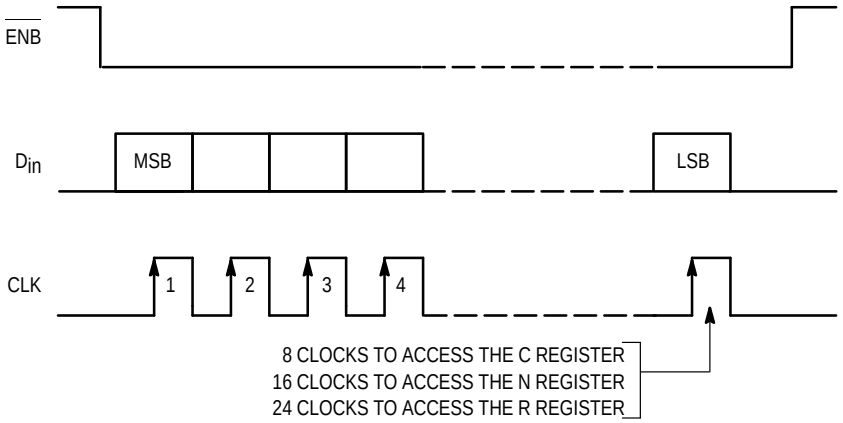


CC = Count Complete Bit
0 = Count NOT Complete, invalid F Count data (also, this bit is 0 when the F Counter is in the initialized state)
1 = Count Complete, valid F Count data

IN D = Input D Pin Status
0 = Pin is a Logic 0
1 = Pin is a Logic 1

MSB to LSB of F Counter = Binary Representation of the Frequency Counter's Value.
For Example, if the Frequency Counter counts to 10,000 in decimal, this is $2710 in hexadecimal. Therefore, the value read, when Input D is at a logic low level, is $802710. Note for this example that the CC bit is set to a 1 which indicates a valid count.

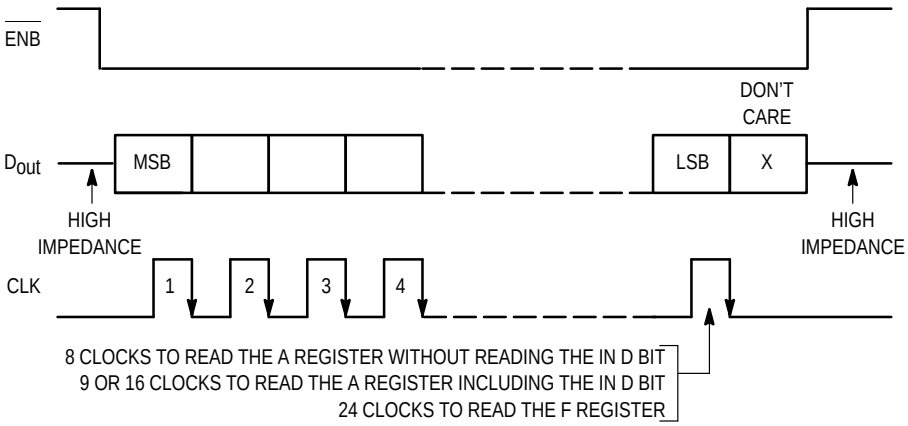
ACCESSING THE WRITE–ONLY REGISTERS



↑ = when the PLL frequency synthesizer loads the data bit.

ACCESSING THE READ–ONLY REGISTERS

The Read F Bit or Read A Bit in the C Register must be set to a 1 prior to the following operation



↓ = when the PLL frequency synthesizer changes the data bit.

CONFIGURING FOR HF AND MF OPERATION

HF = HIGH FREQUENCY: 3 TO 30 MHZ
MF = MEDIUM FREQUENCY 500 kHZ TO 3 MHZ

The write–only registers retain data indefinitely as long as power is applied to the device. Therefore, they do not need to be re–written with the same data when tuning across the band. These registers only need to be written if the contents need to be changed.

Step 1: Load the C Register

The Out A, Out B, and Out C bits must be properly programmed to configure the Output A, Output B, and Output C pins. These outputs switch a few nanoseconds after the C Register is loaded, i.e., after ENB makes a low–to–high transition on a C Register access.

Step 2: Load the R Register

This register determines the tuning resolution of the radio by setting the divide ratio of the R Counter. Also, the HF/VHF bit must be cleared low for HF and MF operation.

As an example, assume that the external crystal connected to pins 1 and 24 is 10.25 MHz. Also, assume that the tuning resolution is 10 kHz. Then, the divide ratio needed is 10.25 MHz divided by 10 kHz; this is 1025 decimal. In hexadecimal, this is $401.

Loading the R Register is accomplished with 3 bytes. Therefore, if all other bits are low, the serial data is $000401. For HF and MF operation, the ACQ bit is usually set high for a wide acquisition window. Therefore, it is more likely the data is: $008401.

Tuning the HF or MF Band

To tune across the HF or MF band, the N Register needs to be changed.

For example, if the first I.F. is 10.7 MHz, and 530 kHz needs to be tuned, then the L.O. needs to be running at 10.7 MHz plus 530 kHz for high–side injection; this is 11.23 MHz. The resolution is 10 kHz. Therefore, the ratio required for the N Counter is 11.23 MHz divided by 10 kHz; this is 1123 decimal. In hexadecimal, this is $463.

Loading the N register requires 2 bytes. Therefore, the serial data is $0463.

To tune 1000 kHz, use 1170 decimal or $0492.

To tune 1710 kHz, use 1241 decimal or $04D9.

CONFIGURING FOR VHF OPERATION

VHF = VERY HIGH FREQUENCY: 30 TO 130 MHz

The write–only registers retain data indefinitely as long as power is applied to the device. Therefore, they do not need to be re–written with the same data when tuning across the band. These registers only need to be written if the contents need to be changed.

Step 1: Load the C Register

The Out A, Out B, and Out C bits must be properly programmed to configure the Output A, Output B, and Output C pins. These outputs switch a few nanoseconds after the C Register is loaded; i.e., after ENB makes a low–to–high transition on a C Register access.

Step 2: Load the R Register

This register determines the tuning resolution of the radio by setting the divide ratio of the R Counter. Also, the HF/VHF bit must be set high for VHF operation.

As an example, assume that the external crystal connected to pins 1 and 24 is 10.35 MHz. Also, assume that the tuning resolution is 50 kHz. Then, the divide ratio needed is 10.35 MHz divided by 50 kHz; this is 207 decimal. In hexadecimal, this is $CF.

Loading the R Register is accomplished with 3 bytes. Therefore, if all other bits are low, the serial data is $0000CF. For VHF operation, the ACQ bit is usually cleared low for a narrow acquisition window.

Tuning the VHF Band

To tune across the VHF Band, the N Register needs to be changed.

For example, if the I.F. is 10.7 MHz, and 87.5 MHz needs to be tuned, then the L.O. needs to be running at 10.7 MHz plus 87.5 MHz for high–side injection; this is 98.2 MHz. The resolution is 50 kHz. Therefore, the ratio required for the N Counter is 98.2 MHz divided by 50 kHz; this is 1964 decimal. In hexadecimal, this is $7AC.

Loading the N Register requires 2 bytes. Therefore, the serial data is $07AC.

To tune 98.5 MHz, use 2184 decimal or $0888.

To tune 107.9 MHz, use 2372 decimal or $0944.

READING THE A REGISTER

The A Register contains the binary representation of the Analog–to–Digital Converter's value plus the End of Conversion bit (EOC). The EOC bit must be a 1 to indicate a valid conversion. Also, the A Register has bits which indicate the logic levels on the Input C and D pins.

Reading the Logic Levels on the Input C and D Pins

Step 1: Store the Values in the Shift Register

To store the value, set the Read A bit in the C Register to a 1. The digital value present at the Input C and D pins during the falling edge of ENB on the read cycle is stored in the shift register.

Step 2: Read the Serial Data

To read the Input C value only, take the $\overline{\text{ENB}}$ pin low and shift out 8 bits. The Input C value is contained in the In C bit.

To read both the Input C and D values, take the ENB pin low and shift out 9 or 16 bits. The values are in the In C and In D bits.

NOTE: In D may also be read from the F Register.

Reading the Analog–to–Digital Converter Value

Step 1: Initialize

To initialize the converter, clear the I SMPL bit in the C Register to a 0. At this time, the Read A bit in the C Register must be 0. The Chan bit must be 0 to select Input A or 1 to select Input B. The state may not be changed simultaneously with the I SMPL bit being set high.

Step 2: Acquire the Value

To sample the analog input selected, set the I SMPL bit in the C Register to a 1. The Read A bit must not be changed; it must be a 0.

NOTE: I SMPL may be set high, even if F SMPL is already set high. I SMPL is not automatically cleared low.

The length of time required to acquire the data is dependent on the crystal frequency (tied to pins 1 and 24) or OSC_{in} frequency. The formula is: T = 3584/f; where T is the acquisition time in seconds and f is the frequency at OSC_{in} in hertz. After the I SMPL bit is set, the EOC bit is set high after the acquisition time T above, and data is available to be read.

Step 3: Read the Serial Data

To read the ADC value, set the Read A bit in the C Register to a 1. I SMPL must not be changed; it must be a 1.

Take the ENB pin low and shift out 8 bits. The value is contained in the least–significant 6 bits. In addition, the EOC bit should be checked to ensure it is a 1; this indicates that the conversion was complete before the data was read. If EOC is a 0, the conversion result is not valid.

The In C bit is valid and indicates the logic level present on the Input C pin. (Alternatively, 9 or 16 bits could be shifted out if the user desires to read both the In C and In D bits.)

NOTE: When the Read A bit is set to a 1, writing to any register is inhibited. After the serial shift which reads the A Register occurs, Read A is automatically cleared to a 0.

CAUTION

If both Read A and Read F are set simultaneously, a *Read A Register* operation is performed and the *Read F Register* request is ignored.

READING THE F REGISTER

The F Register contains the binary representation of the Frequency Counter's value plus the Count Complete flag (CC). The CC bit must be a 1 to indicate a valid count. Also, the F Register has a bit which indicates the logic level on the Input D pin.

Reading the Logic Level on the Input D Pin

Step 1: Store the Value in the Shift Register

To store the value, set the Read F bit in the C Register to a 1. The digital value present at the Input D pin during the falling edge of ENB on the read cycle is stored in the shift register.

Step 2: Read the Serial Data

To read the Input D value, take the $\overline{ENB}$ pin low and shift out 24 bits. The Input D value is contained in the In D bit.

NOTE: In D may also be read from the A Register.

Reading the Frequency Counter Value

Step 1: Initialize

To initialize the counter, clear the F SMPL bit in the R Register to a 0. At this time, the Read F bit in the C Register must be 0. The HF/VHF bit in the R Register must be a 0 for HF–MF operation or 1 for VHF operation. The ACQ (Acquisition Window) bit must be a 0 for a narrow acquisition window or a 1 for a wide window. The formula for the window:

$$t = \frac{2^{(19 + 2a)}}{f}$$

where t = acquisition window (in seconds), a = logic level of acquisition bit (0 or 1), f = crystal frequency or OSC_{in} frequency in hertz.

Step 2: Acquire the Count

To sample the frequency, set the F SMPL bit in the R Register to a 1. The Read F bit must not be changed; it must be a 0.

CAUTION

F SMPL must not be set if I SMPL is already set high.

The data is available to be read after the acquisition window time above. The CC bit is set high immediately after the acquisition is complete.

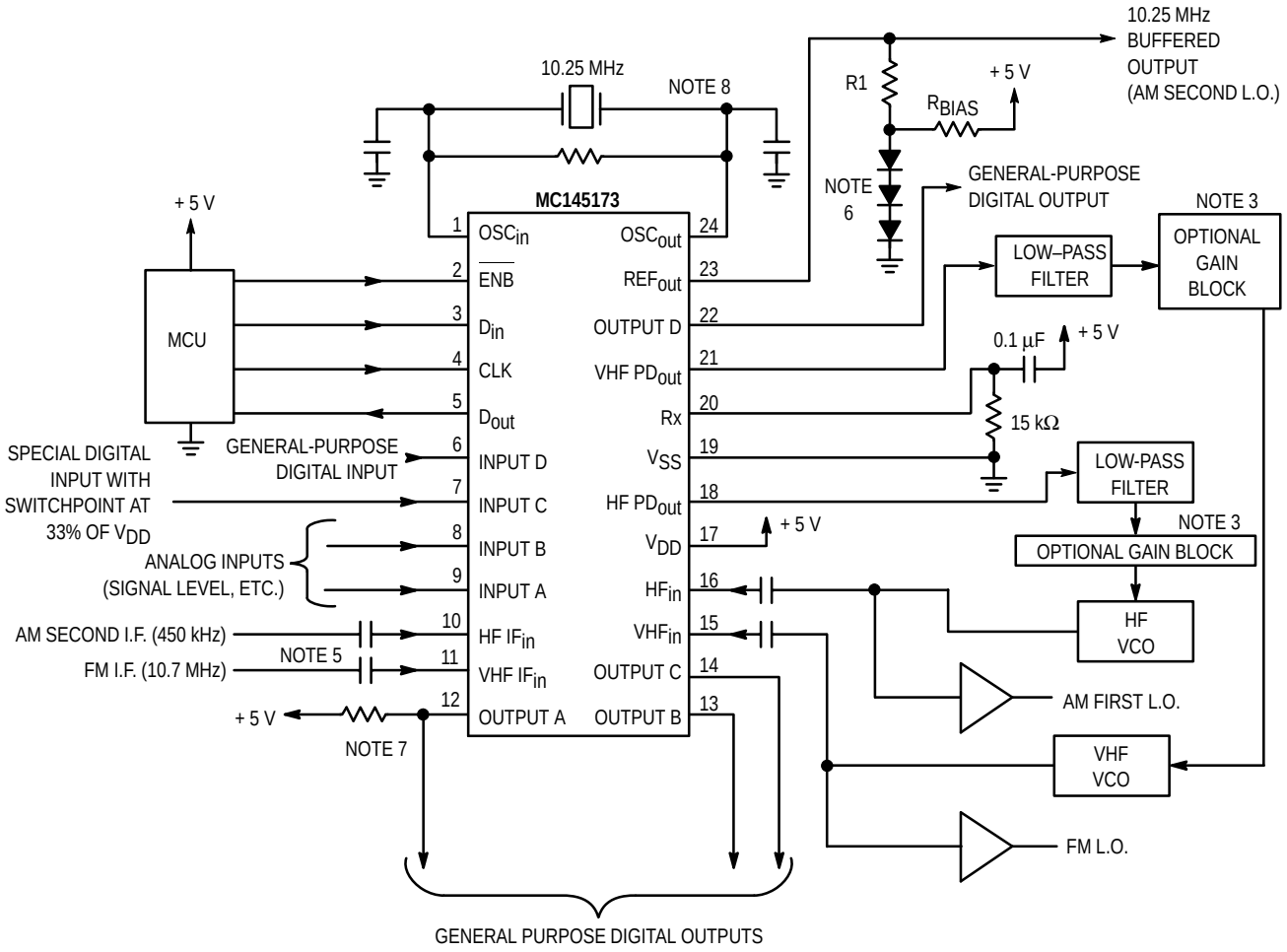
Step 3: Read the Serial Data

To read the F Counter value, set the Read F bit in the C Register to a 1. F SMPL must not be changed; it must be a 1. Take the ENB pin low and shift out 24 bits. The value is contained in the least–significant 22 bits. In addition, the CC bit should be checked to ensure it is a 1; this indicates that the count was complete before the data was read. If CC is a 0, the count is not valid. The In D bit is valid and indicates the logic level present on the Input D pin.

NOTE: When the Read F bit is set to a 1, writing to any register is inhibited. After the serial shift which reads the F Register occurs, Read F is automatically cleared to a 0.

CAUTION

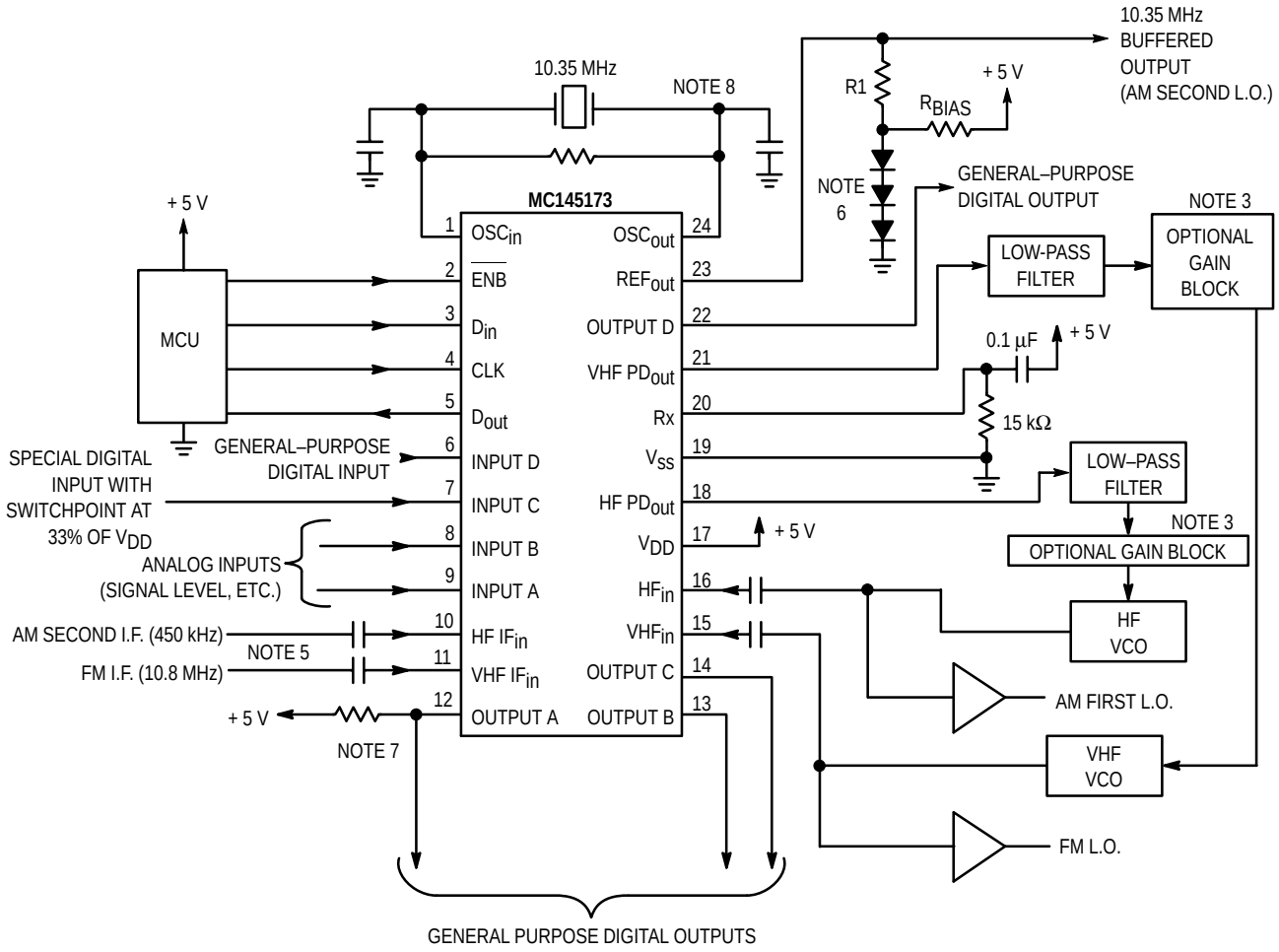
If both Read A and Read F are set simultaneously, a *Read A Register* operation is performed and the *Read F Register* request is ignored.



NOTES:

1. The HF PD_{out} and VHF PD_{out} pins require different low-pass filters. See the Phase-Locked Loop – Low-Pass Filter Design page for more information.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} with a low-inductance capacitor.
3. The gain blocks can be simple one-transistor circuits. See Figures 28 and 29.
4. For the AM band, an R counter divide ratio of 1,025 is used for 10 kHz tuning resolution. The FM band uses an R counter ratio of 205 for 50 kHz tuning resolution.
5. I.F. (intermediate frequency) signals are fed to pins 10 and 11 only if seek or scan feature is included in radio.
6. Diode string is used to limit voltage swing at pin 23; additional or fewer diodes may be used. For full rail-to-rail swing, tie R1 to V_{SS} (GND) and delete the diodes and the R_{BIAS} resistor. **Caution:** this large signal swing may cause a high level of EMI (electromagnetic interference).
7. Pull-up voltage must be at the same potential as the V_{DD} pin or less. Pull-up device other than a resistor may be used.
8. A 10.25 MHz crystal facilitates design of the AM upconversion scheme shown. This results in double conversion for the AM receiver. Optionally, single-conversion designs may be used which offer more flexibility on reference crystal values. For example, a 10.0 MHz crystal could be used which would allow higher-performance 200 kHz tuning resolution for FM.

Figure 26. AM-FM Broadcast Receiver Subsystem — USA

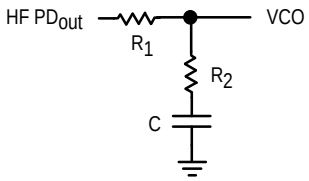


NOTES:

1. The HF PD_{out} and VHF PD_{out} pins require different low–pass filters. See the Phase–Locked Loop – Low–Pass Filter Design page for more information.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} with a low–inductance capacitor.
3. The gain blocks can be simple one–transistor circuits. See Figures 28 and 29.
4. For the AM band, an R counter divide ratio of 1,150 is is used for 9 kHz tuning resolution. The FM band uses an R counter ratio of 207 for 50 kHz tuning resolution.
5. I.F. (intermediate frequency) signals are fed to pins 10 and 11 only if seek or scan feature is included in radio.
6. Diode string is used to limit voltage swing at pin 23; additional or fewer diodes may be used. For full rail–to–rail swing, tie R1 to V_{SS} (GND) and delete the diodes and the R_{BIAS} resistor. **Caution:** this large signal swing may cause a high level of EMI (electromagnetic interference).
7. Pull–up voltage must be at the same potential as the V_{DD} pin or less. Pull–up device other than a resistor may be used.
8. A 10.35 MHz crystal facilitates design of the AM upconversion scheme shown. This results in double conversion for the AM receiver. Optionally, single–conversion designs may be used which offer more flexibility on reference crystal values. For example, a 10.0 MHz crystal could be used which would allow higher–performance 100 kHz tuning resolution for FM.

Figure 27. AM–FM Broadcast Receiver Subsystem — Europe

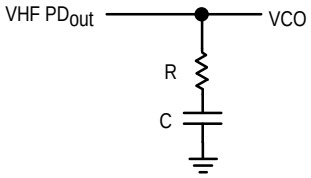
PHASE–LOCKED LOOP — LOW PASS FILTER DESIGN



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO}C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:

For VHF PD_{out}, using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/ filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ volts per radian for HF PD_{out}

K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for VHF PD_{out}

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

The filters shown above are frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

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Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

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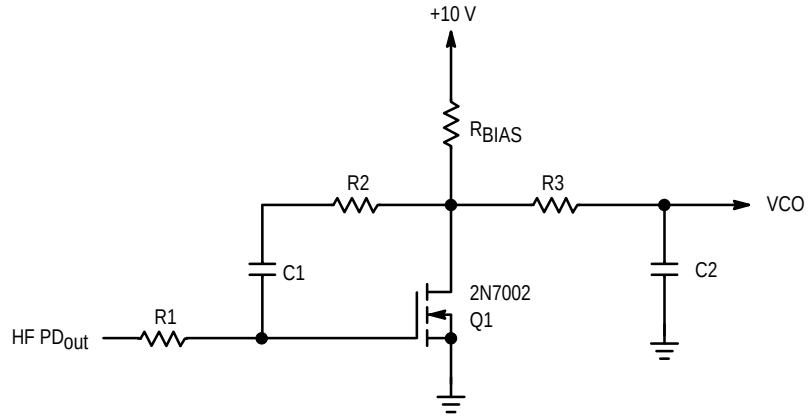
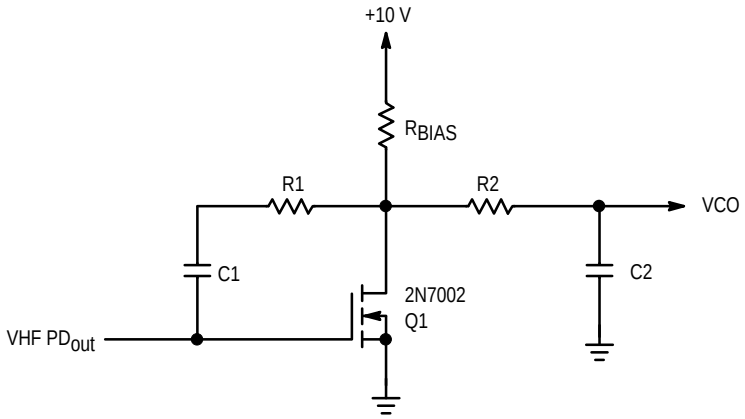
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design* 1987.



NOTES:
1. R1, C1, and R2 form the main filter (determine the loop bandwidth).
2. R3 and C2 are extra filtering; set above loop bandwidth.
3. R1/C1/R2 and R3/C2 are isolated due to Q1. Therefore, there should be minimal interaction.

Figure 28. Active Low–Pass Filter with Gain for HF PD_{out}

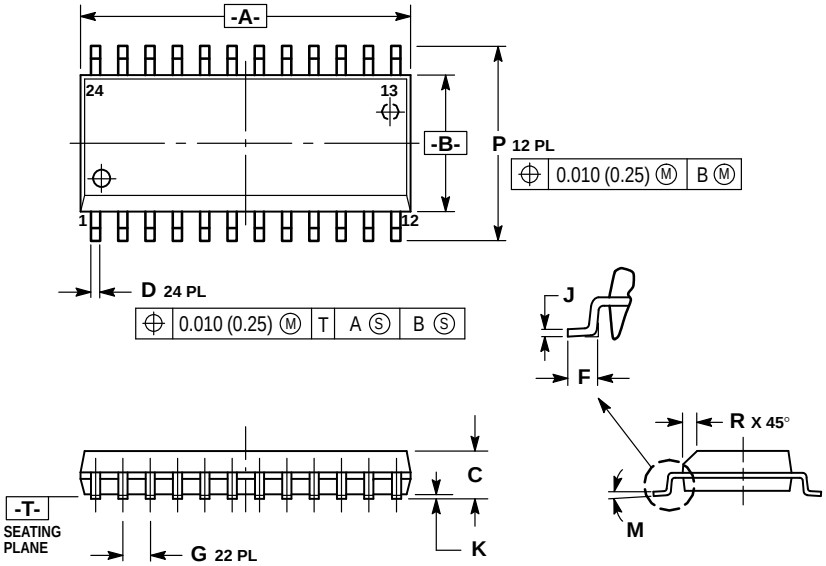


NOTES:
1. R1 and C1 form the main filter (determine the loop bandwidth).
2. R2 and C2 are extra filtering; set above loop bandwidth.
3. R1/C1 and R2/C2 are isolated due to Q1. Therefore, there should be minimal interaction.
4. This filter configuration is a concept and has not been examined in the laboratory.

Figure 29. Active Low–Pass Filter with Gain for VHF PD_{out}

PACKAGE DIMENSIONS

DW SUFFIX
SOG (SMALL–OUTLINE GULL–WING) PACKAGE
CASE 751E–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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