HM-65162/883

2K x 8 Asynchronous CMOS Static RAM

March 1997

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Fast Access Time. . . . . 70/90ns Max**
- **Low Standby Current. . . . . .50μA Max**
- **Low Operating Current . . . . . 70mA Max**
- **Data Retention at 2.0V. . . . . .20μA Max**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Pinout (2716, 6116 Type)**
- **No Clocks or Strobes Required**
- **Wide Temperature Range . . . . . -55^{O}C to +125^{O}C**
- **Equal Cycle and Access Time**
- **Single 5V Supply**
- **Gated Inputs**
  - **No Pull-Up or Pull-Down Resistors Required**

Description

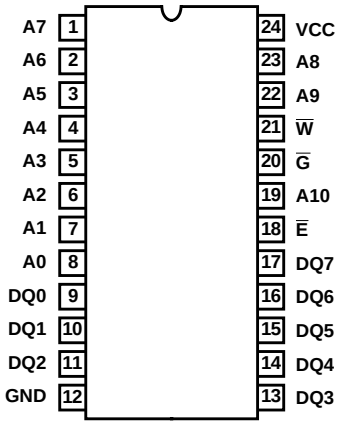
The HM-65162/883 is a CMOS 2048 x 8 Static Random Access Memory manufactured using the Intersil Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 24 pin DIP, and 32 pad 8-bit wide standard which allows easy memory board layouts flexible to accommodate a variety of industry standard PROMs, RAMs, ROMs and EPROMs. The HM-65162/883 is ideally suited for use in microprocessor based systems with its 8-bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors.

Ordering Information

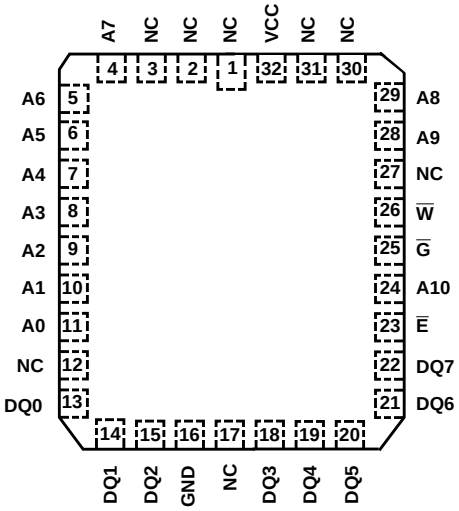
70ns/20μA	90ns/40μA	90ns/300μA	TEMP. RANGE	PACKAGE	PKG. NO.
HM1-65162B/883	HM1-65162/883	HM1-65162C/883	-55^{O}C to 125^{O}C	CERDIP	F24.6
HM4-65162B/883	HM4-65162/883	-	-55^{O}C to 125^{O}C	CLCC	J32.A

Pinouts

HM-65162/883 (CERDIP)
TOP VIEW



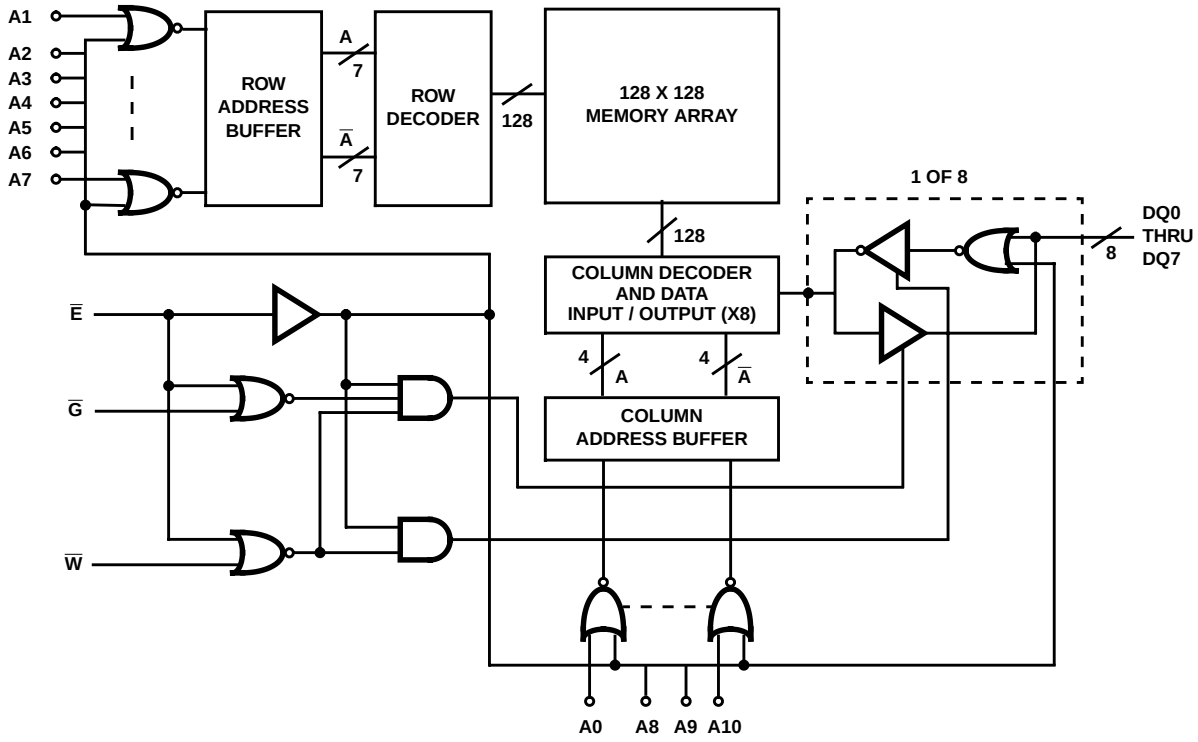
HM-65162/883 (CLCC)
TOP VIEW



PIN	DESCRIPTION
NC	No Connect
A0 - A10	Address Input
$\overline{E}$	Chip Enable/Power Down
VSS/GND	Ground
DQ0 - DQ7	Data In/Data Out
VCC	Power (+5V)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

File Number **3001.1**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
Typical Derating Factor . . . . . 1.5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	$48^oC/W$	$8^oC/W$
CLCC Package	$66^oC/W$	$12^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Input Low Voltage . . . . . 0V to +0.8V
Chip Enable High/Low Time . . . . . 40ns (Min)
Input High Voltage . . . . . -2.2V to VCC
Data Retention Supply Voltage . . . . . 2.0V to 4.5V
Input Rise and Fall Time . . . . . 40ns Max

TABLE 1. 65162/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 2.2V, or $\overline{E}$ = 2.2V, VI/O = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	1.0	µA
Standby Supply Current	ICCSB1	HM-65162B/883, IO = 0mA, VCC = 5.5V, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	50	µA
		HM-65162/883, IO = 0mA, VCC = 5.5V, $\overline{E}$ = VCC - 0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	100	µA
		HM-65162C/883, IO = 0mA, VCC = 5.5V, $\overline{E}$ = VCC - 0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	900	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	8	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 2), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	70	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	70	mA
Data Retention Supply Current	ICCDR	HM-65162B/883, IO = 0mA, VCC = 2.0V, $\overline{E}$ = VCC - 0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	20	µA
		HM-65162/883, IO = 0mA, VCC = 2.0V, $\overline{E}$ = VCC - 0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	40	µA
		HM-65162C/883, IO = 0mA, VCC = 2.0V, $\overline{E}$ = VCC - 0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	300	µA
Functional Test	FT	VCC = 4.5V (Note 3)	7, 8A, 8B	$-55^oC \le T_A \le +125^oC$	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC - 2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 2. HM-65162/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS						UNITS
					HM-65162B /883		HM-65162 /883		HM-65162C /883		
					MIN	MAX	MIN	MAX	MIN	MAX	
Read/Write/ Cycle Time	(1) TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	70	-	90	-	90	-	ns
Address Access Time	(2) TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	70	-	90	-	90	ns
Chip Enable Access Time	(3) TELQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	70	-	90	-	90	ns
Output Enable Access Time	(5) TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	50	-	65	-	65	ns
Chip Selection to End of Write	(11) TELWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	45	-	55	-	55	-	ns
Address Setup Time	(12) TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	10	-	ns
Write Enable Pulse Write	(13) TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	55	-	55	-	ns
Write Enable Read Setup Time	(14) TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	10	-	ns
Data Setup Time	(17) TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	30	-	30	-	30	-	ns
Data Hold Time	(18) TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	15	-	15	-	ns
Write Enable Pulse Setup Time	(20) TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	55	-	55	-	ns
Chip Enable Data Setup Time	(21) TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	30	-	30	-	30	-	ns
Address Valid to End of Write	(22) TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	65	-	65	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC -2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-65162/883 ELECTRICAL PERFORMANCE SPECIFICATIONS, AC AND DC

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS						UNITS
					HM-65162B/883		HM-65162/883		HM-65162C/883		
					MIN	MAX	MIN	MAX	MIN	MAX	
Input Capacitance	CIN	VCC = Open, F = 1MHz, All Measurements Referenced To Device Ground	1, 2	+25°C	-	10	-	10	-	10	pF
			1, 3	+25°C	-	8	-	8	-	8	pF
I/O Capacitance	CI/O	VCC = Open, F = 1MHz, All Measurements Referenced To Device Ground	1, 2	+25°C	-	12	-	12	-	12	pF
			1, 3	+25°C	-	10	-	10	-	10	pF
Chip Enable to Output ON	(4) TELQX	VCC = 4.5V and 5.5V	1	$-55^{o}C \le T_A \le +125^{o}C$	5	-	0	-	5	-	ns
Output Enable to Output ON	(6) TGLQX	VCC = 4.5V and 5.5V	1	$-55^{o}C \le T_A \le +125^{o}C$	5	-	5	-	5	-	ns
Chip Enable High to Output In High Z	(7) TEHQZ	VCC = 4.5V and 5.5V	1	$-55^{o}C \le T_A \le +125^{o}C$	-	35	-	50	-	50	ns
Output Disable to Output in High Z	(8) TGHQZ	VCC = 4.5V and 5.5V	1	$-55^{o}C \le T_A \le +125^{o}C$	-	35	-	40	-	40	ns
Output Hold from Address Change	(9) TAVQX	VCC = 4.5V and 5.5V	1	$-55^{o}C \le T_A \le +125^{o}C$	5	-	5	-	5	-	ns
Write Enable to Output in High Z	(16) TWLQZ	VCC = 4.5V and 5.5V	1	$-55^{o}C \le T_A \le +125^{o}C$	-	40	-	50	-	50	ns
Write Enable High to Output ON	(19) TWHQX	VCC = 4.5V and 5.5V	1	$-55^{o}C \le T_A \le +125^{o}C$	0	-	0	-	0	-	ns
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	1	$-55^{o}C \le T_A \le +125^{o}C$	VCC - 0.4V	-	VCC - 0.4V	-	VCC - 0.4V	-	V

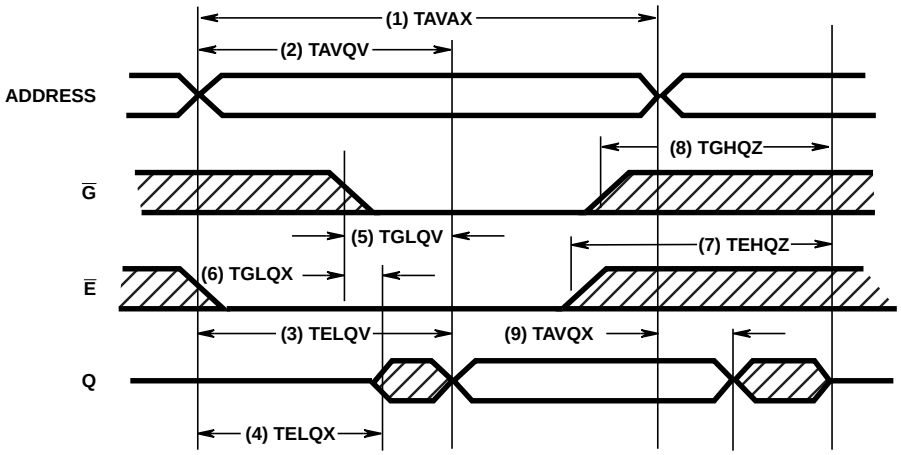
NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 7, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

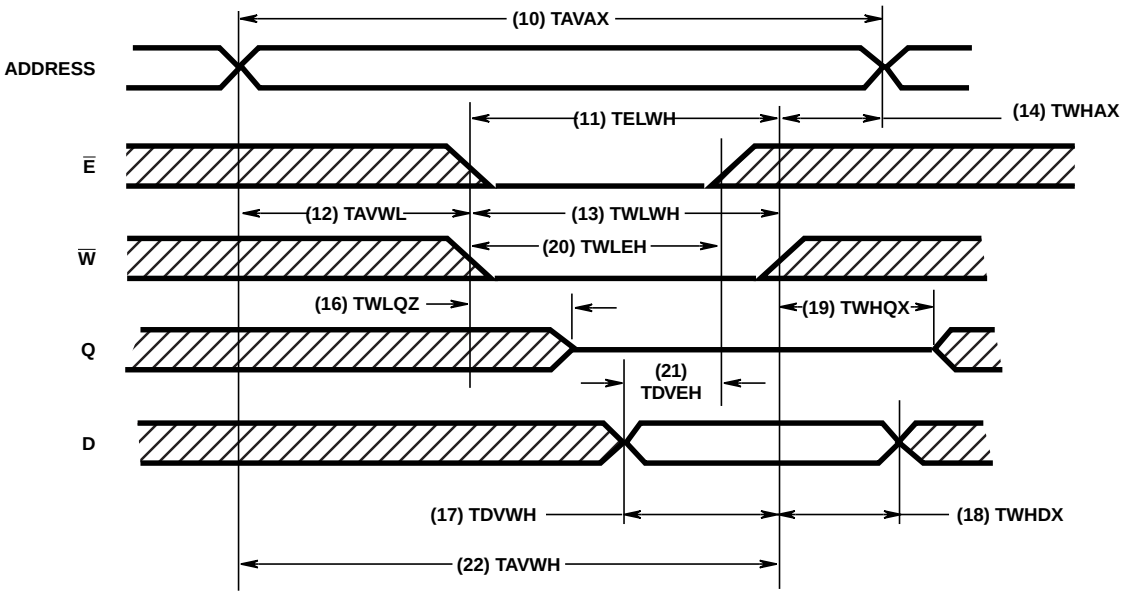


NOTE:

1. $\overline{W}$ is High for a Read Cycle.

FIGURE 1. READ CYCLE

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be ≤ VIL and $\overline{W}$ ≥ VIH. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.



NOTE:

1. $\overline{G}$ is Low throughout Write Cycle.

FIGURE 2. WRITE CYCLE I

To write, addresses must be stable, $\overline{E}$ low and $\overline{W}$ falling low for a period no shorter than TWLWH. Data in is referenced with the rising edge of $\overline{W}$, (TDVWH and TWHDX). While addresses are changing, $\overline{W}$ must be high. When $\overline{W}$ falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied, (Bus contention). If $\overline{E}$ transitions low simultaneously with the $\overline{W}$ line transitioning low or after the $\overline{W}$ transition, the output will remain in a high impedance state. $\overline{G}$ is held continuously low.

Timing Waveforms (Continued)

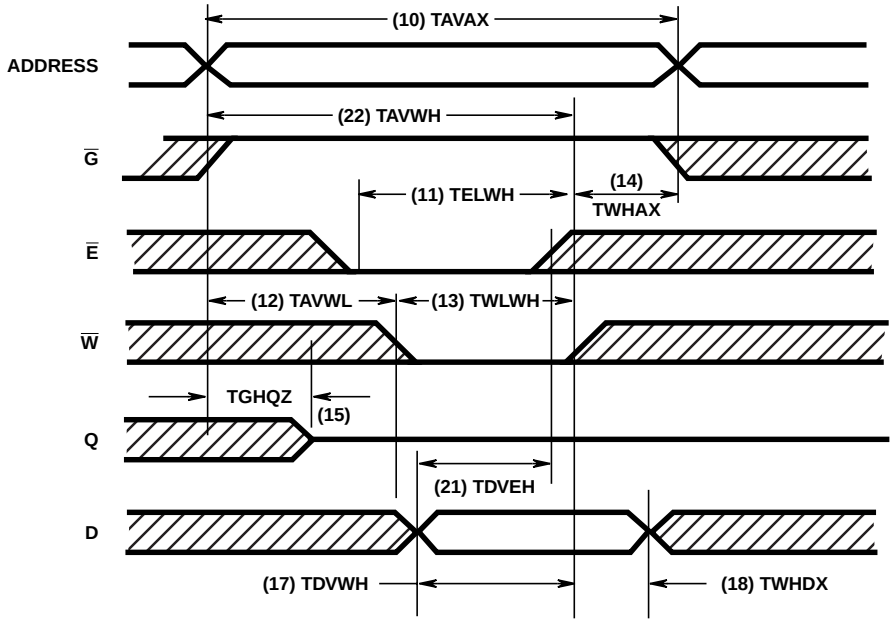


FIGURE 3. WRITE CYCLE II

In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

Low Voltage Data Retention

Intersil CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaran teed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC -0.3V to VCC +0.3V.
2. On RAMs which have selects or output enables (e.g., S, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between VCC +0.3V and 70% of VCC during the power up and down transitions.
4. The RAM can begin operation > 55ns after VCC reaches the minimum operating voltage (4.5V).

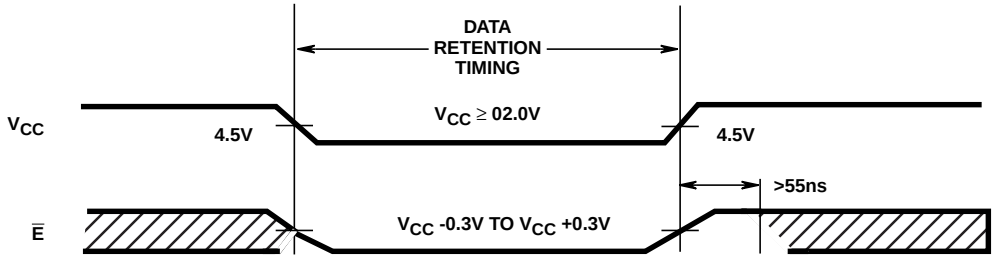
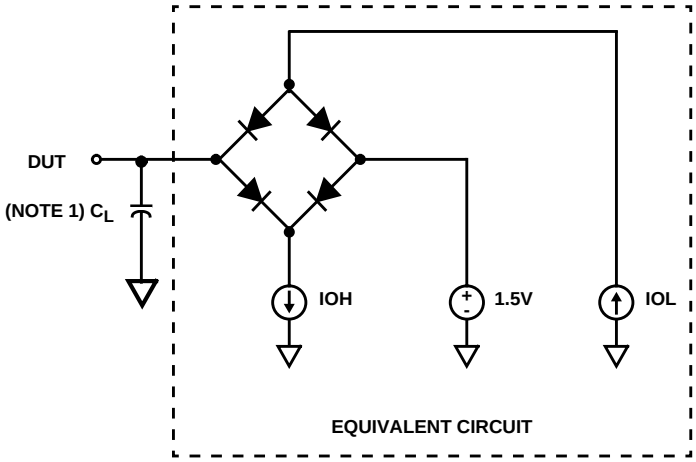


FIGURE 4. DATA RETENTION TIMING

Test Circuit

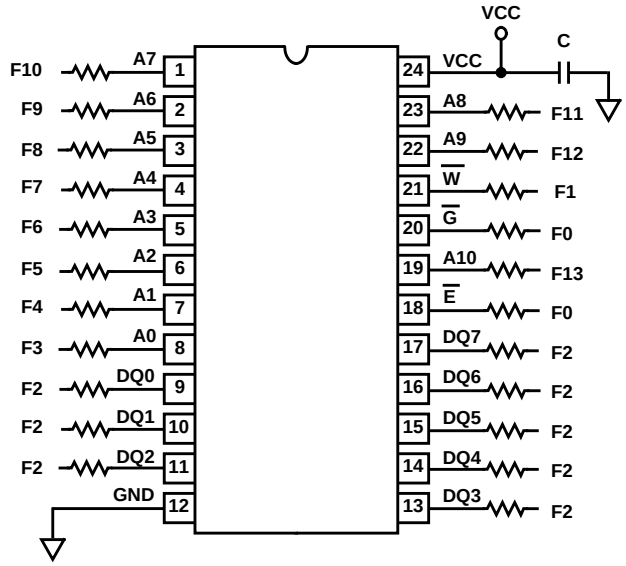


NOTE:

1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuits

HM-65162/883
CERDIP
TOP VIEW



NOTES:

All resistors 47kW ±5%.

F0 = 100kHz ±10%.

F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F13 = F12 ÷ 2.

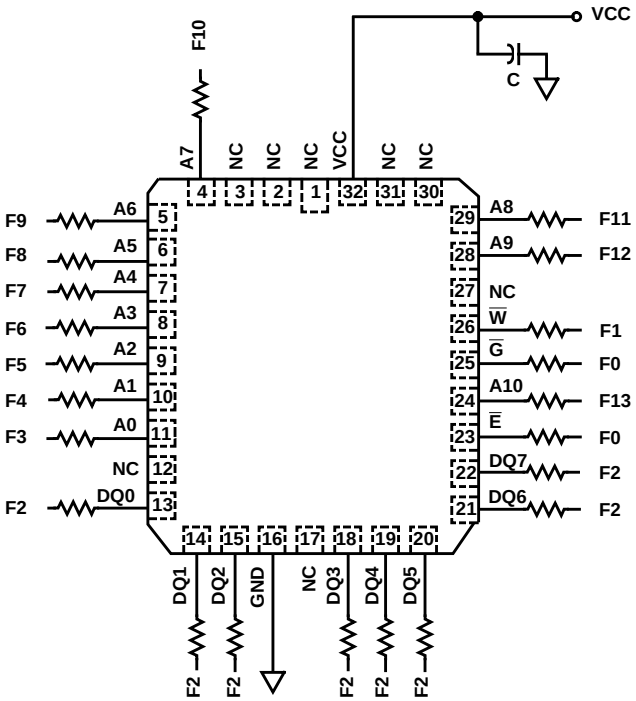
VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

C = 0.01µF Min.

HM-65162/883
CLCC
TOP VIEW



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F0 = 100kHz ±10%.

F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F13 = F12 ÷ 2.

VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

C = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
180.3 x 194.9 x 19 ±1mils

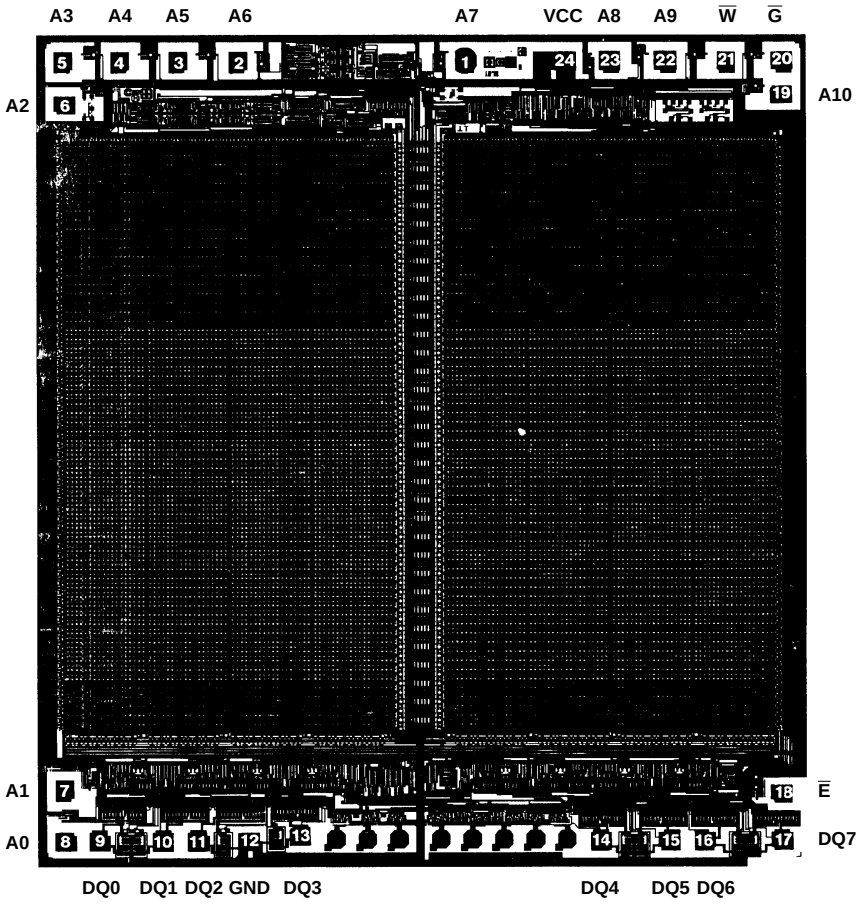
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.7 x 10^5 A/cm^2

Metallization Mask Layout

HM-65162/883



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.