PM4351

PM4351™
COMET

COMET

Combined E1/T1/J1 Transceiver/Framer

Device Errata

Released

Issue 5: June, 2001

Legal Information

Copyright

Disclaimer

None of the information contained in this document constitutes an express or implied warranty by PMC-Sierra, Inc. as to the sufficiency, fitness or suitability for a particular purpose of any such information or the fitness, or suitability for a particular purpose, merchantability, performance, compatibility with other parts or systems, of any of the products of PMC-Sierra, Inc., or any portion thereof, referred to in this document. PMC-Sierra, Inc. expressly disclaims all representations and warranties of any kind regarding the contents or use of the information, including, but not limited to, express and implied warranties of accuracy, completeness, merchantability, fitness for a particular use, or non-infringement.

In no event will PMC-Sierra, Inc. be liable for any direct, indirect, special, incidental or consequential damages, including, but not limited to, lost profits, lost business or lost data resulting from any use of or reliance upon the information, whether or not PMC-Sierra, Inc. has been advised of the possibility of such damage.

Trademarks

COMET is an unregistered trademark of PMC-Sierra, Inc. Other product and company names mentioned herein may be the trademarks of their respective owners.

Patents

The technology discussed is protected by one or more of the following Patents:

U.S. Patent No. 2,242,152

Relevant patent applications and other patents may also exist.

Contacting PMC-Sierra

PMC-Sierra
8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000
Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Technical Support: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

Revision History

Issue No.	Issue Date	ECN #	Details of Change
1	Sept 2000	2968	Notification of additional information and errors to COMET Data Sheet Issue R9
2	Nov 2000	3075	Added information on HDLC in E1 mode
3	Nov 2000	3382	Updated information on PRGD and transmit timing options.
4	Jan 2001	3506	Updated XPLG table and information on E1 75 ohm table
5	Jun 2001	4045	Updated information on RSYNC, RJAT, TJAT and SIGX.

Table of Contents

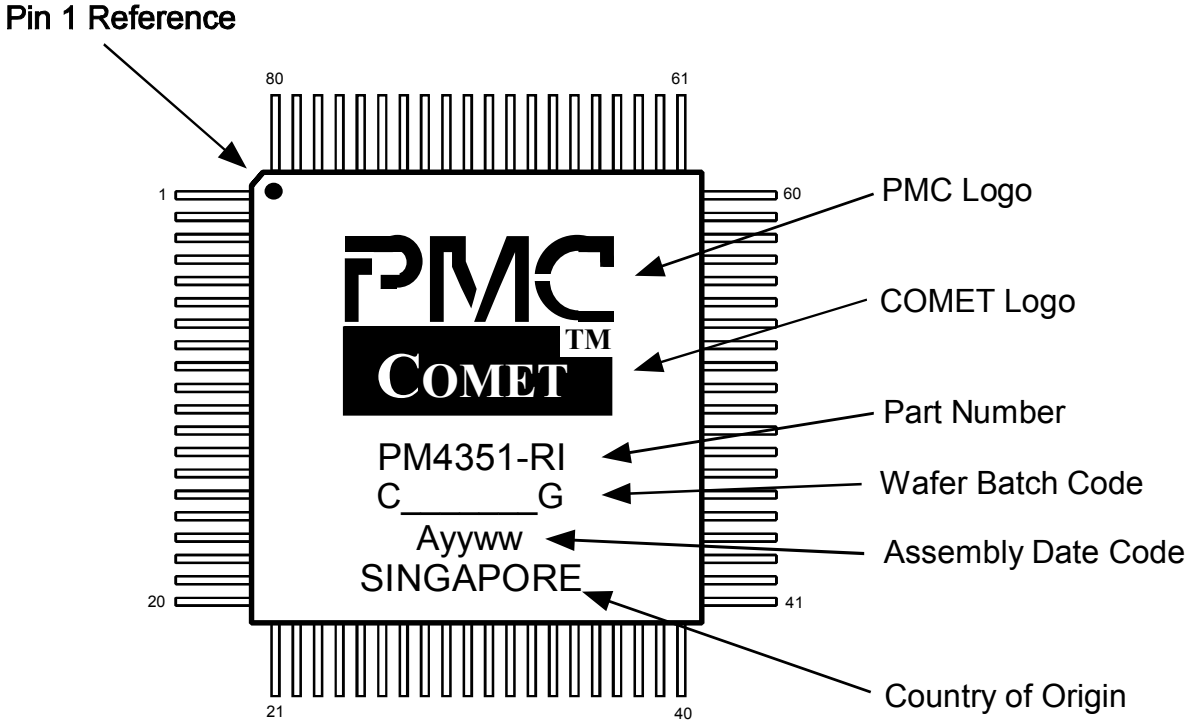
1 Introduction

In this document:

- Section 2 lists the known functional errata for Revisions E, F and G of the PM4351 Device.
- Section 3 lists documentation errors found in Issue 10 of the Data Sheet (PMC-1990315).

1.1 Device Identification

The information contained in Section 2 relates to Revisions E, F and G of the PM4351 Device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device.



SCALE = 3.2:1 (Approx.)

Figure 1 PM4351-RI COMET Branding Format

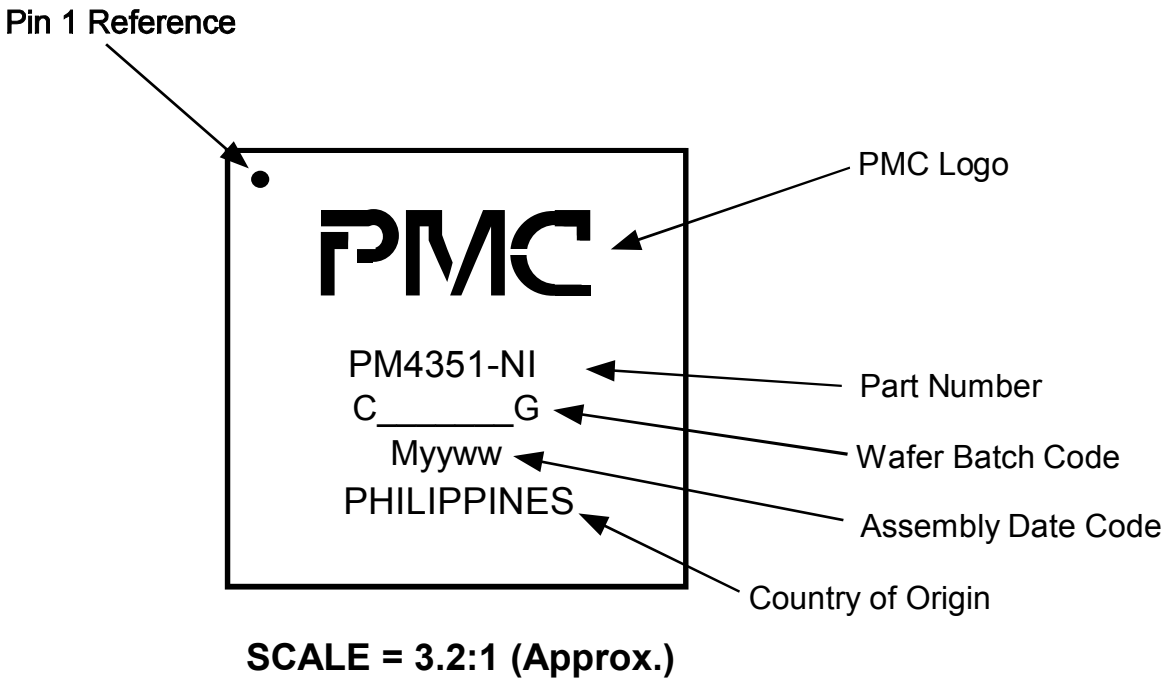


Figure 2 PM4351-NI COMET Branding Format

1.2 References

- Issue 10 of the COMET Data Sheet (PMC-1990315).

2 Device Functional Deficiency List

This section lists the known functional deficiencies for Revisions E, F and G of the COMET as of the publication date of this document. For each deficiency, the known workaround and the operating constraints, with and without the workaround, are also described.

Please report any functional deficiencies not covered in this errata to PMC-Sierra.

2.1 Duplication of APRM Messages

2.1.1 Description:

Forcing the manual load of a performance report can intermittently cause the generation of two identical 13-byte performance reports.

2.1.2 Workarounds:

This is not an issue when the COMET device is configured to automatically generate performance reports, which is its normal operational mode.

2.1.3 Performance with workaround:

Normal operation.

2.1.4 Performance without workaround:

Occasionally, the forced generation of a performance report will create two identical performance reports.

2.2 Internal HDLC Controller and Idle Code Insertion (E1 Mode)

2.2.1 Description:

The two least significant bits of timeslot N, where N is a number between 0 and 31, can be corrupted when any of the below statements are true:

1. Timeslot N+1 is configured for HDLC transmission (via the TDPR) and timeslot N is configured for idle code insertion (via the TPSC).

2. Timeslot N is configured for both HDLC transmission and idle code insertion.

3. Timeslot 31 (N = 31) is configured for idle code insertion and the Si-bit of timeslot 0 is configured for HDLC transmission.

2.2.2 Workarounds:

The following workarounds apply to the above statements respectively:

1. External insertion of idle codes or the use of an external HDLC controller will prevent idle code data corruption. It is recommended to utilize an external HDLC controller should it be necessary to insert idle codes in a timeslot immediately preceding HDLC data.

2. It is recommended to disable idle code insertion for timeslots that are also configured to transmit HDLC data.

3. External insertion of idle codes or the external insertion of HDLC data in the Si-bit position will prevent idle code data corruption.

2.2.3 Performance with workaround:

Normal operation.

2.2.4 Performance without workaround:

The two least significant bits of timeslot N may be corrupted.

NOTE: *This does not impact operation in T1 or J1 modes.*

2.3 Internal HDLC Controller and Timeslot One (E1 Mode)

Description:

If data is inserted into timeslot 1 via the internal HDLC controller and the Sa8-bit is configured to be externally inserted via the backplane, the Sa8-bit can be corrupted.

Workarounds:

The Sa8 bit is not corrupted when insertion is done via COMET's E1-TRAN National Bits Codeword register. The use of the internal HDLC Controller for timeslot one is not recommended.

Performance with workaround:

Normal operation.

Performance without workaround:

Potential corruption of the Sa8 bit.

NOTE: *This does not impact operation in T1 or J1 modes.*

2.4 Internal HDLC Controller and Data in Sa-bit Positions (E1 Mode)

2.4.1 Description:

If the internal HDLC controller is used to insert HDLC data in the Sa8, Sa7, Sa6 or Sa5 bit positions, the more significant bit adjacent to the inserted bit can be corrupted. In other words, HDLC data inserted in Sa8 can corrupt Sa7 and likewise data inserted in Sa5 can corrupt Sa4.

2.4.2 Workarounds:

National Use Bits (Sa-bits) inserted using the internal E1-TRAN block are always inserted correctly. Use of the internal HDLC controller to insert data into the Sa8, Sa7, Sa6, and Sa5 bit positions should be avoided.

2.4.3 Performance with workaround:

Normal operation.

2.4.4 Performance without workaround:

Potential corruption of a National Use (Sa) bit.

NOTE: *This does not impact operation in T1 or J1 modes.*

3 Documentation Deficiency List

This section lists the known documentation deficiencies for Issue 10 of the Data Sheet (PMC-1990315) as of the publication date of this document.

Please report any documentation deficiencies not covered in this errata to PMC-Sierra.

3.1 Description of NmNI

The description of NmNI bit in Register 07FH: T1 APRM One Second Content LSB (Octet 6) may be misleading. The most recent second "t" report should not always be associated with NmNI = "00" as the table seems to indicate. Since the value of NmNI updates every second, the most recent APRM report can contain any combination of NmNI bits. The previous APRM report would contain this value of NmNI decremented by one.

3.2 CSU_LOCK Bit

The CSU_LOCK bit as described in Register 0D6H: CSU Configuration states that a persistent logic 0 in this bit position may indicate a mismatch between the actual and expected XCLK frequency or a problem with the analog supplies (TAVS4 and TAVD4). More clearly stated, the CSU_LOCK bit will reliably read a persistent zero when there is a mismatch between the actual and expected XCLK frequency. It is possible, however, that this bit may read a persistent zero even when lock has been acquired. Problems with the analog supplies (TAVS4 and TAVD4) can also lead to a persistent zero.

3.3 Transmit Timing Options

In Table 19: Transmit Timing Options Summary, the row containing the heading, "Transmit data ignored. Receive data is looped back", should be changed. The bit setting of "PLLREF1" in this row should read "PLLREF1=0" instead of "PLLREF1=X".

3.4 Repetitive Pattern Detection

Sections on the PRGD should be changed to reflect that the COMET provides repetitive pattern detection in addition to pseudo random pattern detection. It is, however, recommended to utilize pseudo random detection instead of fixed pattern detection for diagnostic purposes. Pseudo random sequences provide a more reliable indication of line continuity since they are not susceptible to matching fixed patterns that may exist in normal data traffic. This recommendation is reinforced by the following standards ITU-T O.151, O.152 and O.153.

To implement repetitive pattern detection, the PS bit (Reg 0E0H) should be set to 1. The COMET will then lock on to any repetitive pattern of the length specified in the PL register (Reg 0E2H). After observing that the receiver has locked to the incoming data stream, a specific pattern can be verified by comparing against the received pattern in the PD history registers.

3.5 XPLG RAM Table for Short Haul (0 – 110 ft.)

The XPLG RAM table for Short Haul (0-110 ft.) should be replaced by the following table. The actual changes to the table are highlighted. Note that this change does not apply to the TR62411 Short Haul table (0-110 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	45	00	00	00
2	0A	44	00	00	00
3	**1F**	43	00	00	00
4	**3E**	43	00	00	00
5	3F	42	00	00	00
6	3F	42	00	00	00
7	3C	41	00	00	00
8	3B	41	00	00	00
9	3A	00	00	00	00
10	39	00	00	00	00
11	39	00	00	00	00
12	38	00	00	00	00
13	37	00	00	00	00
14	36	00	00	00	00
15	34	00	00	00	00
16	**28**	00	00	00	00
17	**49**	00	00	00	00
18	**50**	00	00	00	00
19	50	00	00	00	00
20	4D	00	00	00	00
21	4A	00	00	00	00
22	48	00	00	00	00
23	46	00	00	00	00
24	46	00	00	00	00

3.6 Transmit Waveform Values for E1 75 Ohm

It should be noted that the transmit waveform values for E1 75 Ohm operation listed in Table 105 apply to both the 12.7 Ohm and 8.06 Ohm termination resistor options listed in Table 14, "Termination Resistors, Transformer Ratios and TRL."

3.7 RSYNC Operation

The datasheet incorrectly describes the interaction between RJAT and RSYNC. The description of RJATBYP in the Receive Options Register (002H) should state that RSYNC is always jitter attenuated by the RJAT, regardless of the RJATBYP bit.

3.7.1 Location

The Receive Options Register (002H) is located on page 80 in Section 11.

3.7.2 Original Wording

The RJATBYP bit disables jitter attenuation in the receive direction. When receive jitter attenuation is not being used, setting RJATBYP to logic 1 will reduce the latency through the receiver section by typically 40 bits. When RJATBYP is set to logic 0, the RSYNC output and the BRCLK output (if BRCLK is configured to be an output by setting the CMODE bit of the Receive Backplane Configuration register to logic 0), are jitter attenuated. When the RJAT is bypassed, RSYNC and BRCLK are not jitter attenuated.

3.7.3 Replacement Wording

The RJATBYP bit disables or enables jitter attenuation of BRCLK when BRCLK is configured as an output (CMODE bit of the Receive Backplane Configuration register is set to logic 0.) Bypassing the RJAT will reduce the latency through the receiver section by typically 40 bits. Setting RJATBYP to logic 1 disables RJAT. When RJATBYP is set to logic 0, RJAT is enabled. RSYNC is always jitter attenuated regardless of the setting of RJATBYP.

3.8 RJAT and TJAT Configuration

The description of the "Divider N2 Control" registers (016H and 019H) for the RJAT and TJAT jitter attenuators should indicate that N2 must be progammed to a value greater than 15D (0FH) for normal operation. Furthermore, it should also be noted that minimizing the values of N1 and N2 while keeping N1=N2, minimizes intrinsic jitter.

3.9 PCCE Bit Description

The current description of the PCCE bit under reset conditions is confusing. Clearly stated, the PCCE bit is set to logic 0 after device reset. Logic 0 is the default status of this bit which is already indicated in the register description. The statement regarding reset is therefore unneccessary and should be deleted from the bit description.

3.9.1 Location

The PCCE bit description is part of the SIGX Configuration Register (050H) on page 178 of Section 11.

3.9.2 Original Wording

The per-timeslot/per-channel configuration enable bit, PCCE, enables the configuration data in the per-timeslot/per-channel registers to affect the BRSIG and BRPCM data streams. A logic 1 in the PCCE bit position enables the Per-Timeslot/Per-Channel Configuration Register bits in the indirect registers 40H through 5FH; a logic 0 disables the Per-Timeslot/Per-Channel Configuration Register bits in those registers. Please refer to the Per-timeslot/Per-Channel Configuration descriptions for configuration bit details. When the TSB is reset, the PCCE bit is set to logic 0, disabling the Per-Timeslot/Per-Channel Configuration Register bits.

3.9.3 Replacement Wording

The per-timeslot/per-channel configuration enable bit, PCCE, enables per-timeslot/per-channel configuration of the BRSIG and BRPCM data streams. A logic 1 enables per-timeslot/per-channel configuration and a logic 0 disables per-timeslot/per-channel configuration. Please refer to the Per-Timeslot/Per-Channel Configuration Register bits of the indirect registers 40H through 5FH for configuration details. ~~When the TSB is reset, the PCCE bit is set to logic 0, disabling the Per-Timeslot/Per-Channel Configuration Register bits.~~

4 Information

4.1 SLC®96 Signaling and Data Link Extraction

As noted in the datasheet, while the PM4351 COMET device frames to a SLC®96 T1 signal, external logic is required to process the nine state SLC®96 signaling and to process the data link. Please talk to PMC-Sierra's applications engineers for further information on this topic. Contact: apps@pmc-sierra.com

4.2 Software Identification of COMET Rev. G

COMET Rev E, Rev F and Rev G share the same JTAG and device ID. In order to uniquely identify Rev G using software, the following routine can be executed:

i. Read Register 00DH: Revision/Chip ID/Global PMON Update. Revision F or Revision G will contain "00100101".

ii. Read Register 00AH: Master Diagnostics. In Revision F, bit 6 will read logic 0. In Revision G, bit 6 will read logic 1.

NOTE: For this two step sequence to work, step (ii) must follow immediately after step (i) without any intervening microprocessor accesses. Any intervening accesses could invalidate step (ii).

Notes