NETWORK CONVERGENCE OF VOICE, DATA AND VIDEO

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CONTENTS

1 CONVERGENCE OF VOICE, DATA AND VIDEO

Network infrastructures of telecommunications service providers are evolving, driven by the need for cost-effective deployment and management of new and existing services such as public and private telephony, leased line, Frame Relay and ATM. The carrier's separate voice, leased line and packet networks are transitioning from a large collection of different equipment including Narrowband, Broadband and Wideband Digital Cross Connects, ADMs, ATM and Frame Relay switches towards a single network of ATM Multi-service switches. The net result is twofold. Firstly, the convergence of voice, leased line and packet networks results in reduced total operating costs attributed to lower network management and overall equipment requirements. Secondly, carriers can capitalize on ATM's inherent capabilities of supporting multiple services, guaranteed QoS, bandwidth on demand, scaleability and reliability.

As Digital Cross Connects are upgraded to support ATM or are replaced by ATM Multi-service switches, TDM traffic which includes voice, data and private leased line services must be circuit emulated across the ATM network. The ATM Forum has defined the Circuit Emulation Service (CES) Interoperability Specification to enable the transport of Constant Bit Rate (CBR) voice, data and leased line traffic over ATM networks using the ATM Adaptation Layer 1 (AAL1) protocol.

The AAL1 protocol provides the ability to transfer constant bit rate traffic, timing information and structure information between source and destination. To achieve this AAL1 uses the ATM CBR service category and defines the information payload within each cell to support these capabilities.

Circuit emulation is also used in next generation Customer Premise Equipment (CPE) and Customer Located Equipment (CLE) applications such as in Optical Network Units for ATM Passive Optical Networks (APON) and in Integrated Access Devices (IADs) where TDM traffic, for example from a PBX, is converted into ATM cells.

This white paper describes how the transport of TDM traffic over ATM, compliant to CES and AAL1, is realized using the AAL1gator AAL1 Segmentation and Reassembly (SAR) processors from PMC-Sierra.

2 AAL1GATOR PRODUCT FAMILY OVERVIEW

The AAL1gator product family satisfies a wide range of system level requirements for enabling high density ATM CES/DBCES in Central Office applications and lower density CES/DBCES in CPE and CLE applications.

The AAL1gator products are highly integrated and flexible monolithic single chip devices that provide DS1, E1, J1, DS3, E3, J2, STS-1 or STM-0 line interface access to an ATM Adaptation Layer 1 (AAL1) Constant Bit Rate (CBR) ATM network. The AAL1gator products enable a variety of circuit emulation services, ranging from structured DS1/E1/J1 for carrying voice traffic, unstructured DS1/E1/J2 for private line consolidation to unstructured DS3/E3/J2/STS-1/STM-0.

The AAL1gator product family comprises five products: AAL1gator-I, PM73121 AAL1gator-II, PM73122 AAL1gator-32, PM73123 AAL1gator-8 and PM73124 AAL1gator-4 as shown in Figure 1.

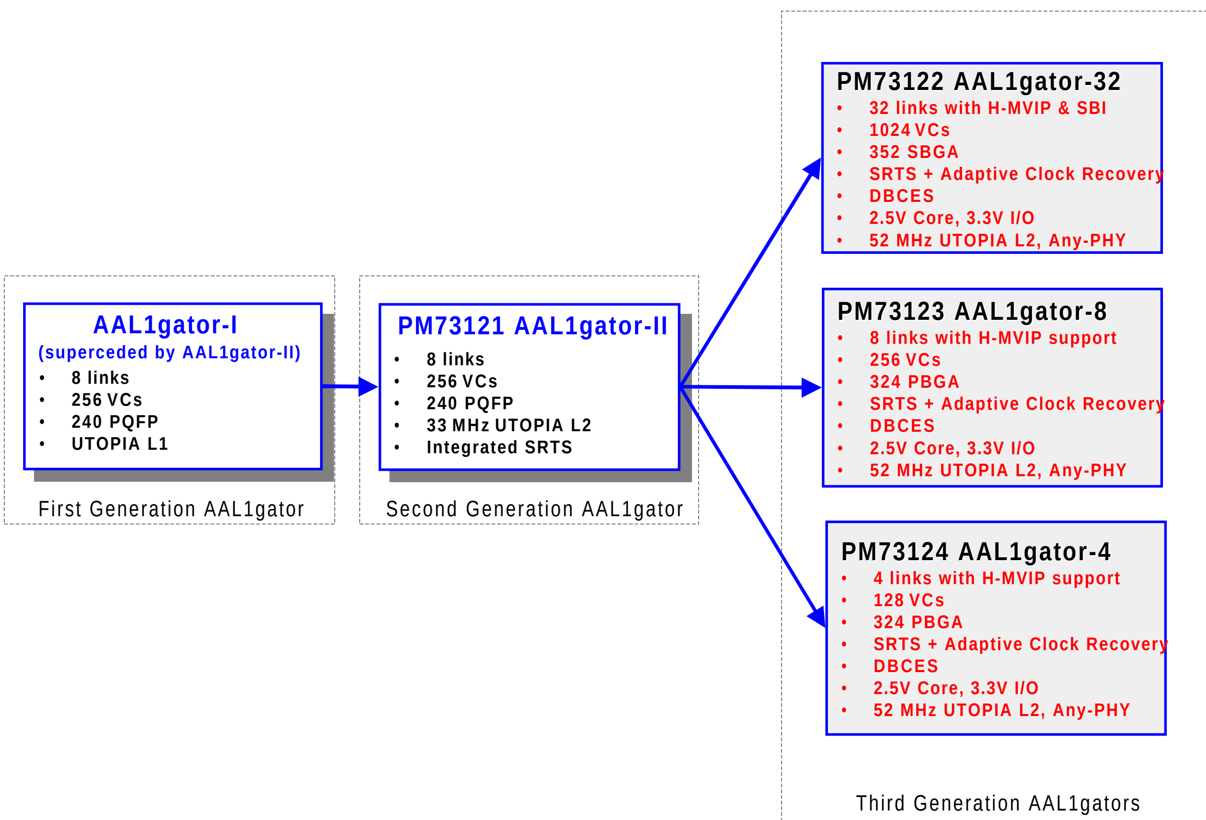

Figure 1. AAL1gator Product Family.

2.1 AAL1gator-I and AAL1gator-II

The AAL1gator-I and PM73121 AAL1gator-II, provide circuit emulation of eight T1/E1 links or a single DS3/E3 link over an ATM network. The AAL1gator-II is the second generation AAL1gator device and supercedes the AAL1gator-I with key enhancements such as increased UTOPIA L2 bandwidth from 25 MHz to 33 MHz and integrated SRTS timing recovery. For a complete list of enhancements see the AAL1gator-II datasheet.

A typical T1/E1 channelized DS3 design using the AAL1gator-II is shown on the left side of Figure 2. The AAL1gator-II design comprises a DS3 Line Interface Unit (LIU), an M13 multiplexer such as PMC's PM8313 D3MX, 28 T1 Framers implemented as seven PMC PM4344 TQUADs and four AAL1gator-IIs. This design provides transport of 28 T1s over ATM.

However, as carriers migrate more and more TDM traffic onto their ATM backbones, the demand for circuit emulation services is driving networking equipment architects to design next generation systems with:

- higher link density for accommodating more TDM traffic per port card
- lower power per link
- Dynamic Bandwidth CES (DBCES) which reduces network bandwidth through intelligent suppression of ATM cell transmission when TDM links are idle. The freed up bandwidth from the idle channels can be used by other traffic classes such as Available Bit Rate (ABR) and Unspecified Bit Rate (UBR).

PMC-Sierra introduces the third generation AAL1gator products, PM73122 AAL1gator-32, PM73123 AAL1gator-8 and PM73124 AAL1gator-4 to address these new requirements.

2.2 AAL1gator-32

The AAL1gator-32 enables the design of low power, high density, DBCES-capable circuit emulation port cards for a wide range of network equipment including ATM Multi-service switches and Digital Cross Connects. The AAL1gator-32 in combination with the PM8315 TEMUX provides over four times the density as compared to previous channelized DS3 designs as illustrated in Figure 2.

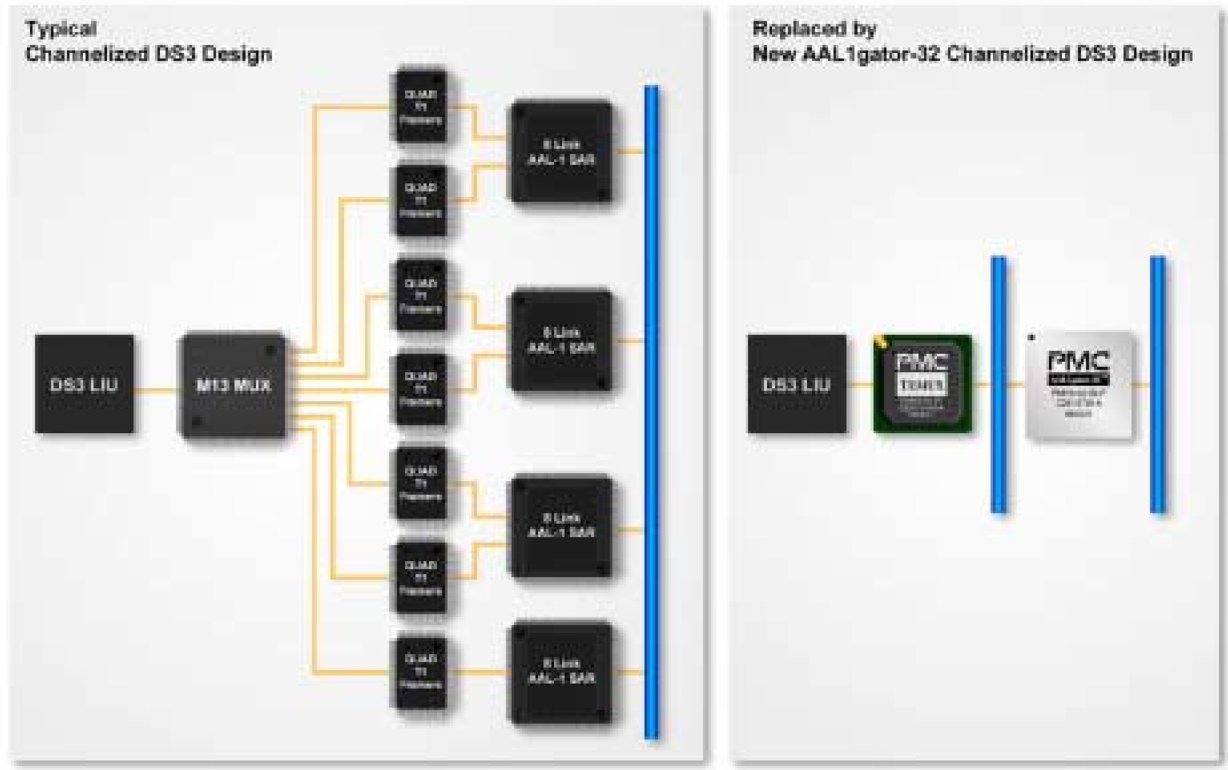

Figure 2. Channelized DS3 Design Comparing the AAL1gator-II with the AAL1gator-32 / TEMUX.

The TEMUX integrates a DS3 Framer, M13 Multiplexer and 28 T1/E1 Framers. Each of the 28 clock, sync, signaling and data signals is communicated to the AAL1gator-32 across the Scalable Bandwidth Interconnect (SBI™) bus. The SBI bus is an 8-bit, 19.44 MHz time-division multiplexed bus capable of transferring both synchronous and asynchronous data up to OC-3 rates. Over the SBI bus, each of the 28 clock signals can be completely independent or common.

The AAL1gator-32 provides AAL1 CES/DBCES processing for up to 32 DS1/E1 links; in this example 28 DS1 links are processed. Each DS1 link can be independently configured as either unstructured or structured, with or without CAS and with or without DBCES. On the ATM side of the AAL1gator-32 device, a UTOPIA / Any-PHY interface is used to interconnect to an ATM Physical Layer chip, Traffic Management device or other ATM component.

The two-chip AAL1gator-32 / TEMUX design in Figure 2 replaces twelve individual components providing lower power per link, lower cost per link and a significant savings in board space. With the reduction in board space and power, the optimized AAL1gator-32 / TEMUX solution enables a new generation of high density circuit emulation port cards such as channelized OC-3 and OC-12 as shown in Figure 3 and Figure 4.

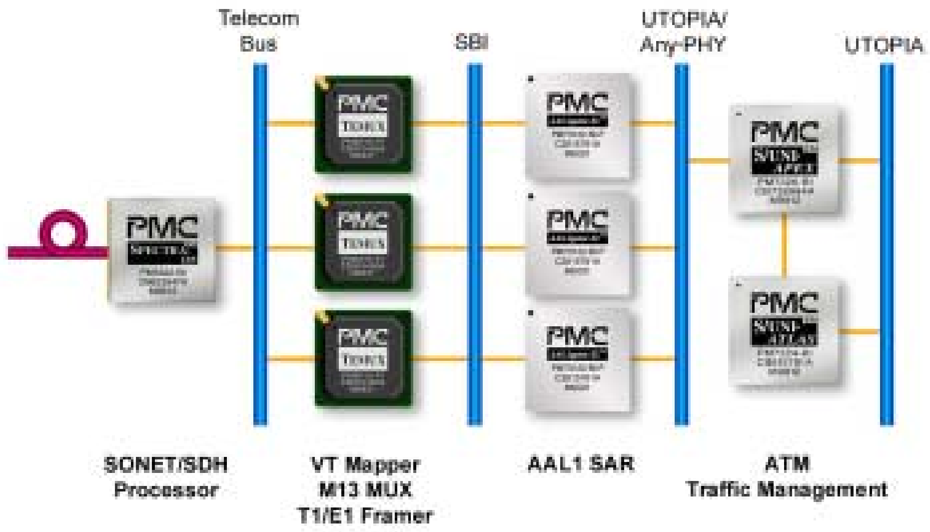

Figure 3. T1/E1 Channelized OC-3 Application.

For the T1/E1 channelized OC-3 application shown in Figure 3 a PM5342 SPECTRA-155 provides SONET/SDH overhead processing at the OC-3 rate of 155.52 Mbps. The Telecom Bus which is an 8-bit parallel bus running at 19.44 MHz interface is used to directly interface the SPECTRA-155 to the TEMUX. The TEMUX provides a VT/TU Mapper in addition to the DS3 Framer, M13 Multiplexer and T1/E1 Framers. In this example three TEMUXs, configured in VT mapper mode, and three AAL1gator-32s share a common SBI bus to support 84 T1 links.

In this example, the ATM side of each AAL1gator-32 is configured for either UTOPIA Level 2 or Any-PHY for interconnecting to the PM7326 S/UNI-APEX ATM Traffic Manager and Switch device. The PM7324 S/UNI-ATLAS performs policing and address translation functions.

With the densities afforded by the AAL1gator-32 and TEMUX devices a single port card can provide an OC-12 worth of T1 links (336 T1 links) as shown in Figure 4. In this example the PM5313 SPECTRA-622 provides SONET/SDH overhead processing at the OC-12 rate of 622 Mbps. As the Telecom and SBI Buses support OC-3 rates, separate buses are required to interconnect each of four groups of three TEMUX and AAL1gator-32 devices.

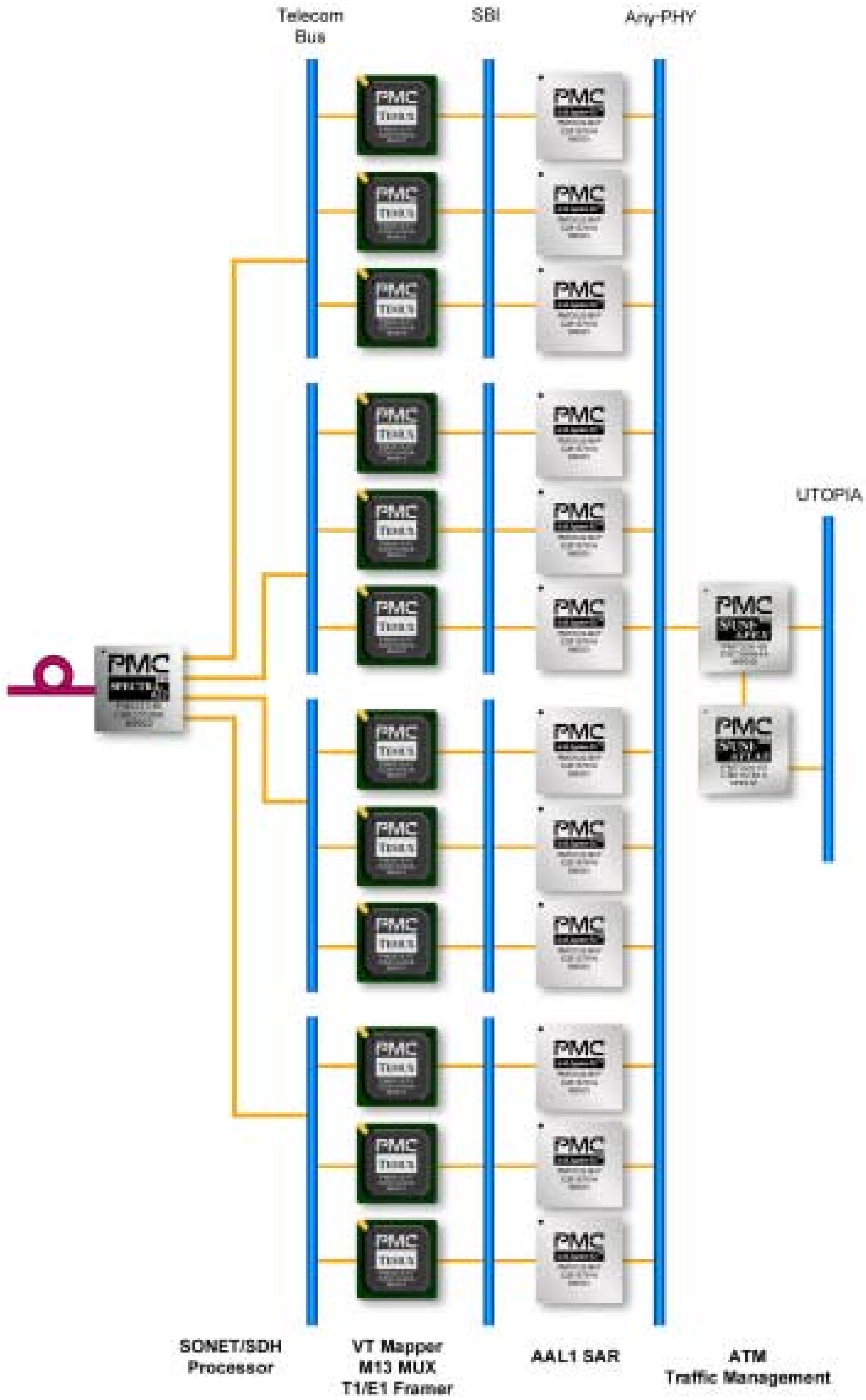

Figure 4. T1/E1 Channelized OC-12 Application.

In addition to providing high link density, the AAL1gator-32 provides significantly lower power per link than previous solutions.

2.3 AAL1gator-8 and AAL1gator-4

The other two new members of the AAL1gator family, the AAL1gator-8 and AAL1gator-4, address CPE and CLE applications where support for a small number of links is required. The AAL1gator-8 and AAL1gator-4 provide low power, DBCES-capable, eight and four link circuit emulation, respectively, for applications such as Integrated Access Devices (IADs), ATM Multi-service Access Switches, Optical Networking Units and base stations in wireless networks.

Like the AAL1gator-II, the AAL1gator-8 provides circuit emulation of eight DS1/E1 links or a single DS3/E3 link; key enhancements provided by the AAL1gator-8 over the AAL1gator-II include:

- Lower power: AAL1gator-8 has 2.5V with 3.3V, 5V tolerant I/O
- DBCES support
- Both SRTS and Adaptive Clock recovery modes are supported internally for T1/E1 rates
- Robust Sequence Number Processing
- Increased UTOPIA L2 bandwidth from 33 MHz to 52 MHz with parity support
- UTOPIA loopback support
- Support for 2 H-MVIP lines
- Support for unstructured STS-1/STM-0 over ATM
- The RAM interface is now decoupled from the microprocessor interface for ease of system design
- Improved OAM cell processing, interrupt processing and DS3 AIS support

The AAL1gator-4 is pin-compatible with the AAL1gator-8 with support for four DS1/E1 links or a single DS3 /E3 link. The AAL1gator-4 is targeted for low link applications such as Optical Networking Units and base stations in wireless networks.

2.4 AAL1gator Product Family Comparison

Table 1 compares the features of the AAL1gator product family (features are described in later sections of the document). Note that the AAL1gator-32, AAL1gator-8 and AAL1gator-4 are recommended for new designs over the AAL1gator-II.

Feature	AAL1gator-32	AAL1gator-8	AAL1gator-4	AAL1gator-II
VCs Supported	1024	256	128	256
DBCES	Yes	Yes	Yes	No
Internal SRTS & Adaptive Clock Timing Recovery	Yes	Yes	Yes	SRTS only
Sequence Number Processing	Fast and Robust	Fast and Robust	Fast and Robust	Fast
Line Interface				
SBI Mode				
DS1/E1	32	N/A	N/A	N/A
DS3	2	N/A	N/A	N/A
DS3 & 16 DS1/E1 Support	Yes	No	No	No
H-MVIP Mode				
TX / RX Lines	8 / 8	2 / 2	1/ 1	N/A
DS1/E1	32	8	4	N/A
High Speed Mode (AAL1gator-32)				
DS3/E3	2	See Direct Mode	See Direct Mode	See Direct Mode
STS-1/STM-0	2	See Direct Mode	See Direct Mode	See Direct Mode
Direct Low Speed Mode (AAL1gator-32)				
DS1/E1	16	See Direct Mode	See Direct Mode	See Direct Mode
MVIP-90	16	See Direct Mode	See Direct Mode	See Direct Mode
Unstructured J2	6	See Direct Mode	See Direct Mode	See Direct Mode
Direct Mode (AAL1gator-8 and AAL1gator-4)				
DS3/E3	See High Speed Mode	1	1	1
STS-1/STM-0	See High Speed Mode	1	1	1
DS1/E1	See High Speed Mode	8	4	8

MVIP-90	See High Speed Mode	8	4	N/A
Unstructured J2	See High Speed Mode	3	3	N/A
System Side Loopback	Yes	Yes	Yes	No
UTOPIA Interface				
UTOPIA L2	52 MHz 16-bit with parity / Any-PHY Option to respond as a 4-port device.	52 MHz 16-bit with parity / Any-PHY Responds as a single port device only.	52 MHz 16-bit with parity / Any-PHY Responds as a single port device only.	33 MHz
General				
RAM	Two 256k x 16 (18) 10 ns Synchronous SRAM or ZBT RAM	One 128k x 16 (18) 10 ns Synchronous SRAM or ZBT RAM	One 128k x 16 (18) 10 ns Synchronous SRAM or ZBT RAM	128kx 16 SRAM
Supply Voltage	2.5V core 3.3V I/O	2.5V core 3.3V I/O	2.5V core 3.3V I/O	5V
Power, Typical, Max	1.7W typical 2.3W max: • 0.5W (3.3V) • 1.8W (2.5V)	0.75W typical 1W max: • 0.4W (3.3V) • 0.6W (2.5V)	0.75W typical 1W max: • 0.4W (3.3V) • 0.6W (2.5V)	2.15W typical 2.53W max
Package Type & Size	352 SBGA (35mm x 35mm)	324 PBGA (23 mm x 23mm)	324 PBGA (23 mm x 23mm)	240 PQFP (32mm x 32mm)

Table 1. AAL1gator Product Family Comparison.

3 SYSTEM APPLICATIONS

The AAL1gator products have been optimized for various applications. The high link density of the AAL1gator-32 makes it ideal for Central Office applications such as ATM Multi-service Switches, DACS and Optical Line Termination units for ATM Passive Optical Networks (APON).

Using the AAL1gator-8 and AAL1gator-4 with T1/E1 framers and integrated LIUs such as the PM4351 COMET, enables ATM transport of up to 8 and 4 T1/E1 circuits, respectively, for applications such as Integrated Access Devices (IADs), ATM Multi-service Access Switches, Optical Networking Units and base stations in wireless networks. Table 2 summarizes the various system applications where the AAL1gator devices are used.

AAL1gator Application	AAL1gator-32	AAL1gator-8	AAL1gator-4
ATM Multi-service Switch	√	√	
DACS with an ATM Interface	√	√	
Access Service Concentrator	√	√	
Unstructured DS3/E3/STS-1/STM-0 over ATM	√	√	
Optical Line Termination (OLT) Unit in an ATM Passive Optical Network (APON)	√		
Integrated Access Device (IAD), PBX		√	√
Optical Network Unit (ONU) in APON			√
LMDS			√

Table 2. AAL1gator System Applications.

3.1 ATM Multi-service Switch

An ATM Multi-service Switch is typically located at the edge of the wide area network. It interfaces to Frame Relay, ATM as well as TDM services and consolidates these different services to ATM cells for transport over a single high-bandwidth ATM core network.

Figure 5 shows a reference design that uses PMC's SPECTRA-155, TEMUX, FREEDM-84A672 and AAL1gator-32 in a multi-service port adapter design that supports channelized DS3 and channelized OC-3 densities.

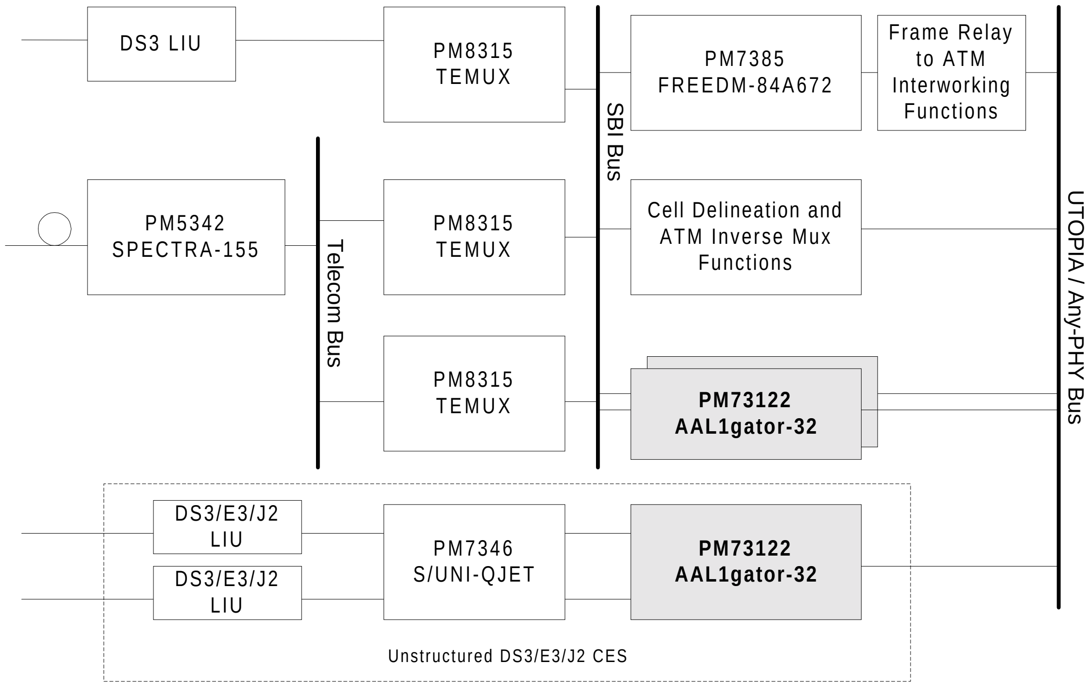

Figure 5. Multi-service Switch Application

3.2 Digital Access Cross Connect (DACS)

Narrowband, wideband or broadband Digital Access Cross Connects (DACS) that need to support ATM uplink interfaces to a core ATM switch can use one or more AAL1gator-32s to emulate a TDM service over an ATM network. DACs with CES capabilities allow service providers to consolidate legacy private line services onto a high speed ATM backbone network and reduce the number of network elements and physical connections that need to be managed. Figure 6 shows the AAL1gator-32 in a DACS application.

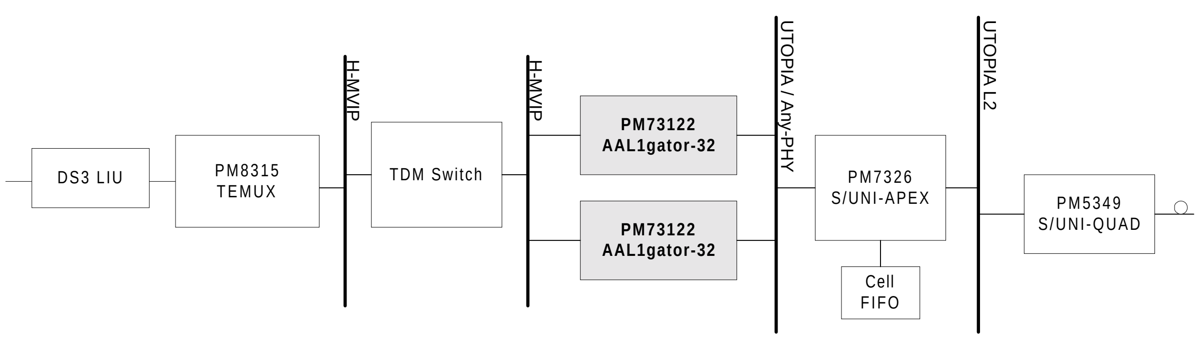

Figure 6. Using the AAL1gator-32 in a DACS application.

3.3 Integrated Access Device

An Integrated Access Device (IAD) consolidates voice, data, Internet, and video wide-area network services using ATM over shared T1/E1 lines. IADs can also unify the functions of many different types of equipment including CSUs, DSUs and multiplexers. Figure 7 shows the AAL1gator-4 connected to four PM4351 COMETs, a PM7326 S/UNI-APEX Traffic Manager, an Inverse Multiplexing over ATM device, the PM7344 S/UNI-MPH and eight PM4351 COMETs for the WAN uplink.

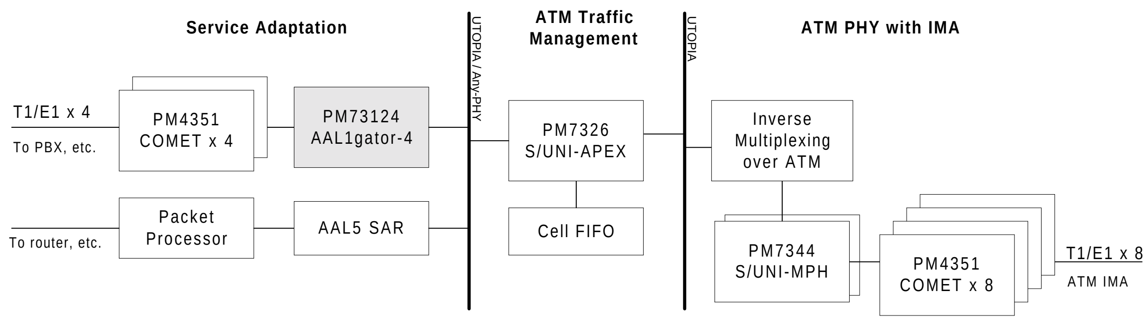

Figure 7. Using the AAL1gator-4 in an Integrated Access Device (IAD) Application.

4 GLOSSARY

A32/A8/A4	AAL1gator-32 / AAL1gator-8 / AAL1gator-4
AIS	Alarm Indication Signal
CAS	Channel Associated Signaling
CCS	Common Channel Signaling
CES	Circuit Emulation Service
CPE	Customer Premise Equipment
CLE	Customer Located Equipment
DBCES	Dynamic Bandwidth Circuit Emulation Service
DS0	Digital Service, level 0: There are 24 DS0 channels in a DS1. Each DS0 channel has a bandwidth of 64 Kbps full duplex.
DS1	Digital Service, level 1. 1.544 Mbps
DS3	Digital Service, level 3. 44.736 Mbps
E1	E1 carries information at the transmission rate of 2 Mbps. This is the rate used by European CEPT carriers to transmit 30, 64 Kbps digital channels for voice or data calls, plus a 64 Kbps channel for signaling and a 64 Kbps channel for framing.
E3	E3 carries information at the transmission rate of 34.368 Mbps. This is the rate used by CEPT to transmit 512 simultaneous voice conversations.
H-MVIP	High Speed Multi-Vendor Integration Protocol: A synchronous time division multiplexed bus of Nx64 Kbps constant bit rate data stream. The H-MVIP standards are defined by the GO-MVIP organization.
ISO	International Standards Organization: An international standards-setting organization.
J2	The Japanese version of the T Carrier system of North America. 6.312 Mbps used to carry 96 voice channels.
LIU	Line Interface Unit
MAN	Metropolitan Area Network: A term used to describe a data network covering an area larger than a local area network, but less than a wide area network. A MAN may carry voice, video and multimedia data.
MIB	Management Information Base
OAM	Operations, Administration and Maintenance
OC-12	Optical Carrier 12. SONET channel of 622.08 Mbps.
OC-3	Optical Carrier 3. A SONET channel that has a bandwidth of 155.52 Mbps

OSI	Open Systems Interconnect: A standard that defines seven independent layers of communication protocols. Each layer enhances the communication services of the layer just below it and shields the layer above it from the implementation details of the lower layer.
SBI	Scaleable Bandwidth Interconnect: A synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links.
SDH	Synchronous Digital Hierarchy: A set of standard fiber-optic transmission standards used outside North America.
SONET	Synchronous Optical NETwork: A family of fiber optic transmission standards used in North America.
SPE	Synchronous Payload Envelope
SRTS	Synchronous Residual Timestamp Timing Recovery
STM-0	Synchronous Transport Module - 0
STS-1	Synchronous Transport Signal Level 1. Basic transmission rate used in SONET – equivalent to 51.84 Mbps.
T1	Trunk Level 1: A digital transmission link with a total signaling speed of 1.544 Mbps.
TSI	Time-Slot Interchanger
UTOPIA	Universal Test and Operations Interface: Refers to an electrical interface between the TC and PMD sublayers of the physical layer. UTOPIA is the interface for devices connecting to an ATM network.
VT	Virtual Tributary: A structure designed for transport and switching of sub-DS3 payloads. A unit of sub-SONET bandwidth that can be combined or concatenated, for transmission through the network. VT1.5 is equivalent to 1.544 Mbps and VT2 equals 2.048 Mbps
WAN	Wide Area Network: A data network that is used to interconnect remote LANs or users over leased lines, packet or cell switch services

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