

## TC55257BPL/BFL/BSPL/BFTL/BTRL-85L/10L(LV)

### SILICON GATE CMOS

### 32,768 WORD x 8 BIT STATIC RAM

#### Description

The TC55257BPL is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns.

When  $\overline{CE}$  is a logical high, the device is placed in a low power standby mode in which the standby current is 2 $\mu$ A at room temperature. The TC55257BPL has two control inputs. Chip enable ( $\overline{CE}$ ) allows for device selection and data retention control, while an output enable input ( $\overline{OE}$ ) provides fast memory access. The TC55257BPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC55257BPL is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

#### Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2 $\mu$ A (max.) at Ta = 25°C
- Single 5V power supply
- Access time (max.)

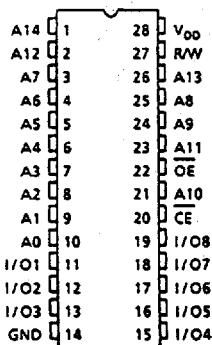
	TC55257BPL/BFL/BSPL/BFTL/BTRL	
	-85L(LV)	-10L(LV)
Access Time	85ns	100ns
Chip Enable Access Time	85ns	100ns
Output Enable Time	45ns	50ns

- Power down feature:  $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
  - TC55257BPL : DIP28-P-600
  - TC55257BFL : SOP28-P-450
  - TC55257BSPL : DIP28-P-300B
  - TC55257BFTL : TSOP28-P
  - TC55257BTRL : TSOP28-P-A

#### Pin Names

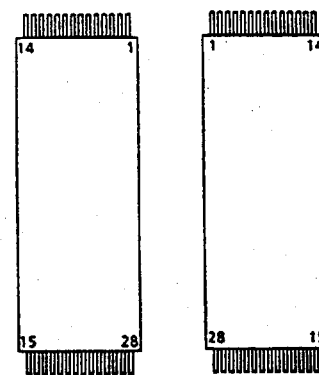
A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground

#### Pin Connection (Top View)



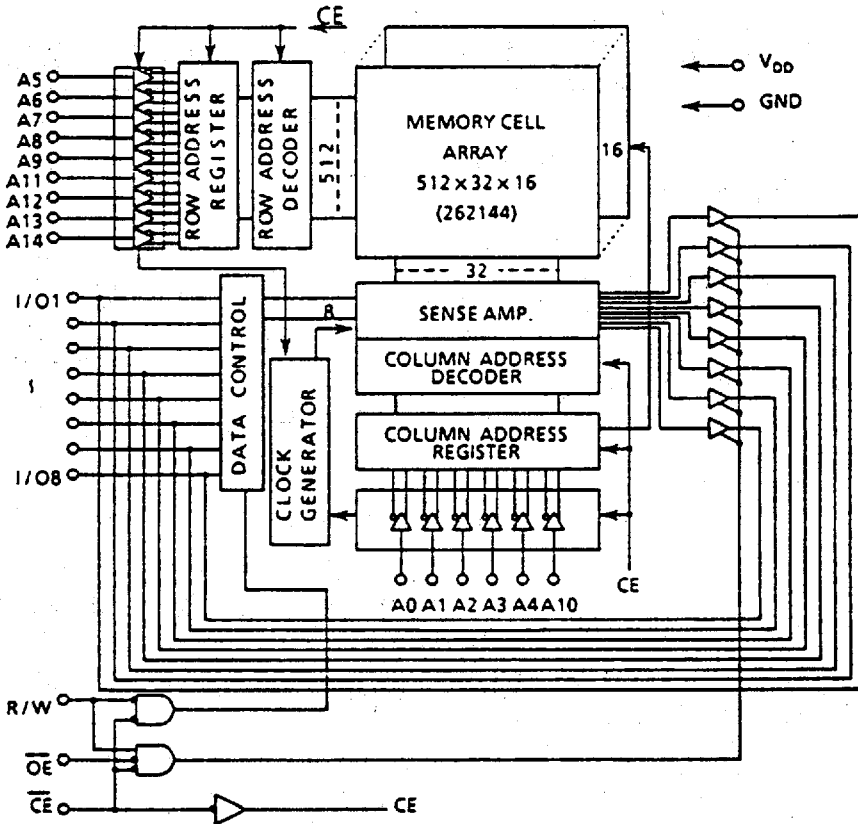
(forward type)

(reverse type)



PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A <sub>11</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>13</sub>	R/W	V <sub>DD</sub>	A <sub>14</sub>	A <sub>12</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A <sub>10</sub>

Block Diagram



Operating Mode

MODE	PIN	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write		L	*	L	D <sub>IN</sub>	I <sub>DDO</sub>
Output Deselect		L	H	H	High-Z	I <sub>DDO</sub>
Standby		H	*	*	High-Z	I <sub>DDs</sub>

\* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-0.3* ~ 7.0	V
V <sub>I/O</sub>	Input and Output Voltage	-0.5* ~ V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	1.0/0.8/0.6**	W
T <sub>SOLDER</sub>	Soldering Temperature • Time	260 • 10	°C • sec
T <sub>STRG</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>OPR</sub>	Operating Temperature	0 ~ 70	°C

\* -3.0V with a pulse width of 50ns

\*\* Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

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**DC Recommended Operating Conditions**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> + 0.3	
V <sub>IL</sub>	Input Low Voltage	-0.3*	-	0.8	
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	

\* -3.0V with a pulse width of 50ns

**DC Characteristics (Ta = 0 ~ 70°C, V<sub>DD</sub> = 5V±10%)**

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = 0 ~ V <sub>DD</sub>	-	-	±1.0	μA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V <sub>IL</sub> or $\overline{OE} = V_{IH}$ V <sub>OUT</sub> = 0 ~ V <sub>DD</sub>	-	-	±1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-1.0	-	-	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	4.0	-	-	mA	
I <sub>DDO1</sub>	Operating Current	$\overline{CE} = V_{IL}$ R/W = V <sub>IH</sub> Other Input = V <sub>IH</sub> /V <sub>IL</sub> I <sub>OUT</sub> = 0mA	t <sub>cycle</sub> = 1μs	-	10	-	mA
			t <sub>cycle</sub> = Min. cycle	-	-	70	
I <sub>DDO2</sub>	Operating Current	$\overline{CE} = 0.2V$ R/W = V <sub>DD</sub> - 0.2V Other Input = V <sub>DD</sub> - 0.2V/0.2V I <sub>OUT</sub> = 0mA	t <sub>cycle</sub> = 1μs	-	5	-	mA
			t <sub>cycle</sub> = Min. cycle	-	-	60	
I <sub>DDS1</sub>	Standby Current	$\overline{CE} = V_{IH}$		-	-	3	mA
I <sub>DDS2</sub>		$\overline{CE} = V_{DD} - 0.2V$ V <sub>DD</sub> = 2.0V ~ 5.5V	Ta = 0 ~ 70°C	-	-	30	μA
		Ta = 25°C	-	-	2		

**Capacitance\* (Ta = 25°C, f = 1MHz)**

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	

\*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V<sub>DD</sub> = 5V±10%)

## Read Cycle

SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85L(LV)		-10L(LV)		
		MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	85	—	100	—	ns
t <sub>ACC</sub>	Address Access Time	—	85	—	100	
t <sub>CO</sub>	$\overline{CE}$ Access Time	—	85	—	100	
t <sub>OE</sub>	Output Enable to Output in Valid	—	45	—	50	
t <sub>COE</sub>	Chip Enable ( $\overline{CE}$ ) to Output in Low-Z	10	—	10	—	
t <sub>OEE</sub>	Output Enable to Output in Low-Z	5	—	5	—	
t <sub>OD</sub>	Chip Enable ( $\overline{CE}$ ) to Output in High-Z	—	30	—	50	
t <sub>ODO</sub>	Output Enable to Output in High-Z	—	30	—	40	
t <sub>OH</sub>	Output Data Hold Time	10	—	10	—	

## Write Cycle

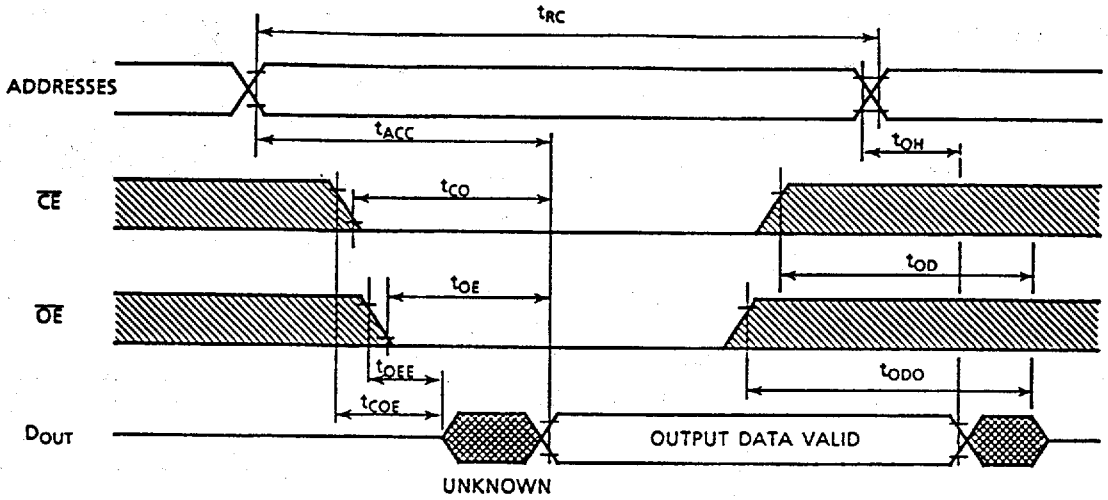
SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85L(LV)		-10L(LV)		
		MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	85	—	100	—	ns
t <sub>WP</sub>	Write Pulse Width	60	—	70	—	
t <sub>CW</sub>	Chip Selection to End of Write	65	—	90	—	
t <sub>AS</sub>	Address Setup Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	5	—	5	—	
t <sub>ODW</sub>	R/W to Output in High-Z	—	30	—	50	
t <sub>OEW</sub>	R/W to Output in Low-Z	5	—	5	—	
t <sub>DS</sub>	Data Setup Time	40	—	40	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

## AC Test Conditions

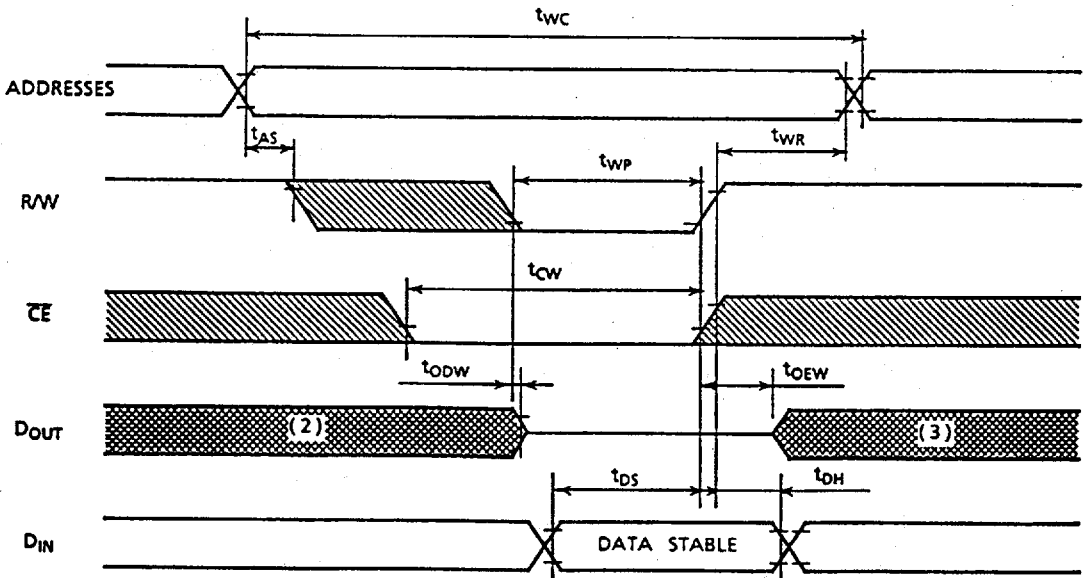
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.2V/0.8V
Output Load	1 TTL Gate and C <sub>L</sub> = 100pF

Timing Waveforms

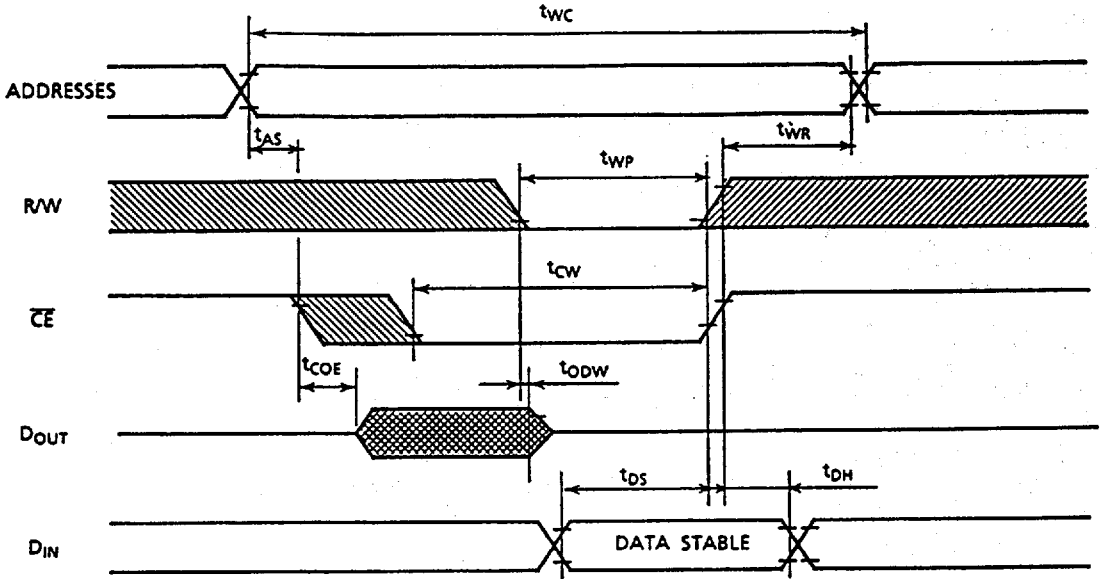
Read Cycle <sup>(1)</sup>



Write Cycle 1 <sup>(4)</sup> (R/W Controlled Write)



Write Cycle 2 <sup>(4)</sup> ( $\overline{CE}$  Controlled Write)



Notes:

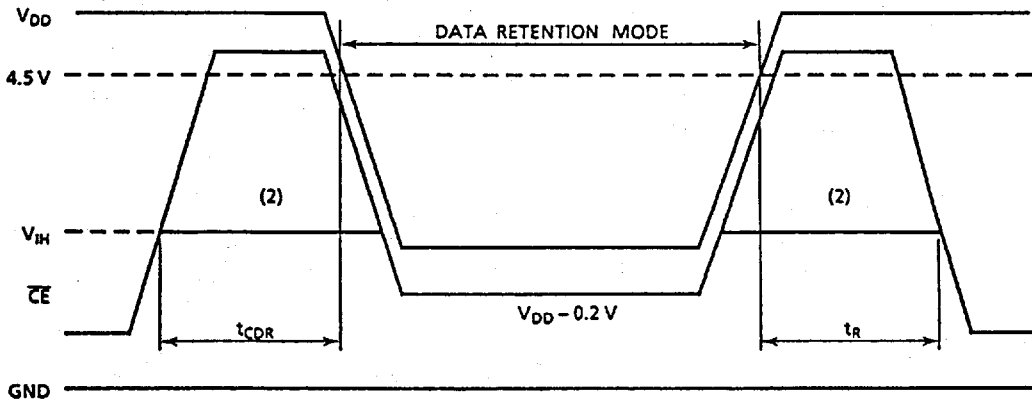
1. R/W is high for read cycles.
2. If the  $\overline{CE}$  low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the  $\overline{CE}$  high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If  $\overline{OE}$  is high during a write cycle, the outputs are in a high impedance state during this period.

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	V
I <sub>DDS2</sub>	Standby Current	V <sub>DH</sub> = 3.0V	-	20	μA
		V <sub>DH</sub> = 5.5V	-	30	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode	0	-	-	μs
t <sub>R</sub>	Recovery Time	t <sub>RC(1)</sub>	-	-	

Note (1): Read Cycle Time

$\overline{CE}$  Controlled Data Retention Mode



Note (2): If the V<sub>IH</sub> of  $\overline{CE}$  is 2.2V in operation, I<sub>DDs1</sub> current flows during the period that the V<sub>DD</sub> voltage is going down from 4.5V to 2.4V.

3V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	2.7	3.0	3.3	V
V <sub>IH</sub>	Input High Voltage	V <sub>DD</sub> - 0.2	-	V <sub>DD</sub> + 0.3	
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.2	

DC Characteristics (Ta = 0 ~ 70°C, V<sub>DD</sub> = 3V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = 0 ~ V <sub>DD</sub>	-	-	±1.0	μA		
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V <sub>IL</sub> or $\overline{OE} = V_{IH}$ , V <sub>OUT</sub> = 0 ~ V <sub>DD</sub>	-	-	±1.0	μA		
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.2V	-0.1	-	-	mA		
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.2V	0.1	-	-	mA		
I <sub>DDO2</sub>	Operating Current	$\overline{CE} = 0.2V$ R/W = V <sub>DD</sub> - 0.2V I <sub>OUT</sub> = 0mA Other Inputs = V <sub>DD</sub> - 0.2V/0.2V	t <sub>cycle</sub>	Min.	-	-	20	mA
				1μs	-	-	5	
I <sub>DDs2</sub>	Standby Current	$\overline{CE} = V_{DD} - 0.2V$	Ta = 0 ~ 70°C		-	-	20	μA
			Ta = 25°C		-	1	2	

Capacitance\* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	

\*This parameter is periodically sampled and is not 100% tested.



**3V Operation**DC Characteristics ( $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{DD} = 3V \pm 10\%$ )**Read Cycle**

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{RC}$	Read Cycle Time	200	—	ns
$t_{ACC}$	Address Access Time	—	200	
$t_{CO}$	$\overline{CE}$ Access Time	—	200	
$t_{OE}$	Output Enable to Output in Valid	—	100	
$t_{COE}$	Chip Enable ( $\overline{CE}$ ) to Output in Low-Z	10	—	
$t_{OEE}$	Output Enable to Output in Low-Z	5	—	
$t_{OD}$	Chip Enable ( $\overline{CE}$ ) to Output in High-Z	—	100	
$t_{ODO}$	Output Enable to Output in High-Z	—	80	
$t_{OH}$	Output Data Hold Time	10	—	

**Write Cycle**

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{WC}$	Write Cycle Time	200	—	ns
$t_{WP}$	Write Pulse Width	150	—	
$t_{CW}$	Chip Selection to End of Write	180	—	
$t_{AS}$	Address Setup Time	0	—	
$t_{WR}$	Write Recovery Time	5	—	
$t_{ODW}$	R/W to Output in High-Z	—	100	
$t_{OEW}$	R/W to Output in Low-Z	5	—	
$t_{DS}$	Data Setup Time	90	—	
$t_{DH}$	Data Hold Time	0	—	

**AC Test Conditions**

Input Pulse Levels	$V_{DD} - 0.2V/0.2V$
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	$C_L = 100\text{pF}$