
LDO Regulators with a Watchdog Timer

R5102V SERIES

APPLICATION MANUAL

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OUTLINE

The R5102V Series are Voltage Regulators with a watchdog timer (WDT) ICs with high accuracy output voltage and low supply current by CMOS process. Each of these ICs consists of an LDO regulator, VR1, and a regulator with ultra low supply current, VR2, and a watchdog timer.

Thus, the R5102V Series have the integrated function of a power source for a system and a system supervisor.

One of the built-in voltage regulators is a LDO type regulator, VR1, used with an external driver transistor.

VR1 has excellent electrical characteristics of high ripple rejection rate, high output voltage accuracy and low supply current. VR1 is appropriate for the condition that the voltage difference between input and output is small and output current is within several hundreds mA.

The output voltage of regulators can be set internally and individually with high accuracy for each IC by laser-trim.

Furthermore, when a system works incorrectly, the watchdog timer checks over microprocessor and generates a reset signal intermittently to prevent a whole system from being malfunction.

The time period for watching and holding a reset signal of the watchdog timer can also be set individually by an external capacitor (C_{TW}).

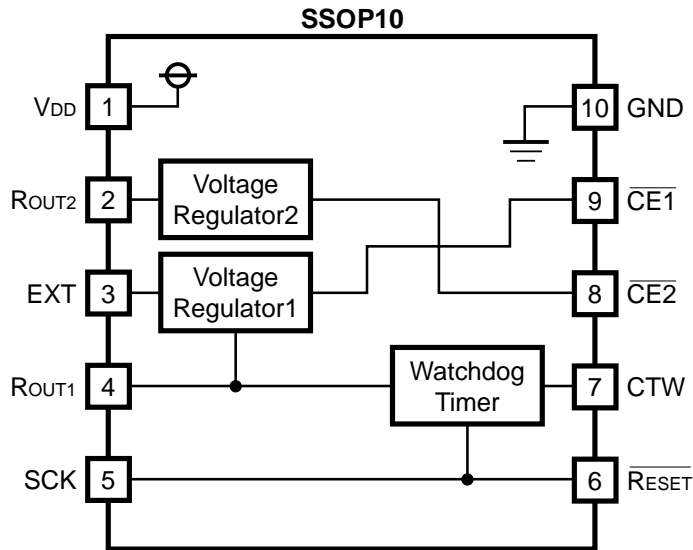
FEATURES

- Built-in a watchdog timer
- Time period for monitoring and generating a reset signal of the watchdog timer can be set by an external capacitor
- Regulators can be stopped individually by $\overline{CE1}$ pin and $\overline{CE2}$ pin.
- Low supply current(Operating Mode) TYP. $28\mu A$ (VR1), TYP. $5\mu A$ (VR2), TYP. $3\mu A$ (WDT) (Standby Mode) TYP. $0.1\mu A$ (VR1), TYP. $0.1\mu A$ (VR2)
- The output voltage of VR1 and VR2 can be set individually for each IC by laser trim
- High Accuracy of Output Voltage $\pm 2.0\%$
- Time period for system monitoring and reset can be set by an external capacitor
- Output Current TYP. $1A$ (VR1), MIN. $30mA$ (VR2) (at $V_{IN} - V_{OUT} = 1V$)
- Small Package SSOP-10 (0.5mm pitch) Refer to Package Dimensions

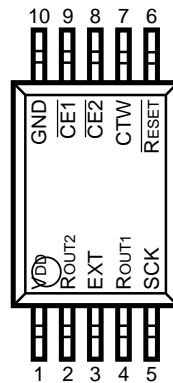
APPLICATION

- Power source for GSM

BLOCK DIAGRAMS



PIN CONFIGURATION



PIN DESCRIPTION

| Symbol | Description |
|---------------------------|---|
| V _{DD} | Power Supply Pin |
| ROUT2 | Output Pin for Voltage Regulator 2 |
| EXT | Driver Pin for External Transistor |
| ROUT1 | Output Pin for Voltage Regulator 1 |
| SCK | Clock Input Pin |
| $\overline{\text{RESET}}$ | Output Pin for Reset signal of Watchdog timer |
| CTW | External Capacitor Pin for Watchdog Timer |
| $\overline{\text{CE2}}$ | Control Switch Pin for Voltage Regulator 2 ("L" Active) |
| $\overline{\text{CE1}}$ | Control Switch Pin for Voltage Regulator 1 ("L" Active) |
| GND | Ground Pin |

ABSOLUTE MAXIMUM RATINGS

 $T_{opt}=25^{\circ}\text{C}, V_{SS}=0\text{V}$

| Symbol | Item | Input Voltage | Rating | Unit |
|------------------------|-----------------------------|-----------------------------------|------------------------------|--------------------|
| V_{IN} | Input Voltage | | 9 | V |
| V_{CE1} | Input Voltage | Voltage of $\overline{CE1}$ Pin | $V_{SS}-0.3$ to $V_{IN}+0.3$ | V |
| V_{CE2} | | Voltage of $\overline{CE2}$ Pin | $V_{SS}-0.3$ to $V_{IN}+0.3$ | V |
| V_{SCK} | | Voltage of V_{SCK} Pin | $V_{SS}-0.3$ to $V_{IN}+0.3$ | V |
| R_{OUT1} | Output Voltage | Voltage of R_{OUT1} Pin | $V_{SS}-0.3$ to $V_{IN}+0.3$ | V |
| R_{OUT2} | | Voltage of R_{OUT2} Pin | $V_{SS}-0.3$ to $V_{IN}+0.3$ | |
| V_{CTW} | | Voltage of CTW Pin | $V_{SS}-0.3$ to $V_{IN}+0.3$ | V |
| $V_{\overline{RESET}}$ | | Voltage of \overline{RESET} Pin | $V_{SS}-0.3$ to 9 | V |
| EXT | EXT Output Voltage | | $V_{SS}-0.3$ to $V_{IN}+0.3$ | V |
| I_{OUT2} | Output Current2 | | 150 | mA |
| I_{EXT} | EXT Current | | 50 | mA |
| P_D | Power Dissipation | | 300 | mW |
| T_{opt} | Operating Temperature Range | | -40 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | -55 to +125 | $^{\circ}\text{C}$ |

ELECTRICAL CHARACTERISTICS

• Overall

T_{opt}=25°C

| Symbol | Item | Conditions | MIN. | TYP. | MAX. | Unit |
|------------------|---|---|------|------|-----------------|------|
| V _{IN} | Input Voltage | | | | 8 | V |
| I _{SS1} | Supply Current | V _{IN} =4.2V, V _{CE1} =V _{CE2} =0V | | 30 | 60 | μA |
| R _{UP} | $\overline{\text{CE}}$ Pull-up Resistance | | 2.5 | 5 | 10 | MΩ |
| V _{CEH} | $\overline{\text{CE}}$ Input Voltage “H” | | 1.5 | | V _{IN} | V |
| V _{CEL} | $\overline{\text{CE}}$ Input Voltage “L” | | 0 | | 0.25 | V |

• VR1

T_{opt}=25°C

| Symbol | Item | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------------------|--|---|-------|--------|-------|--------|
| V _{OUT} | Output Voltage | V _{IN} -V _{OUT} =1.0V I _{OUT} =50mA | 2.744 | 2.800 | 2.856 | V |
| I _{OUT} | Output Current | V _{IN} -V _{OUT} =1.0V | | 1*NOTE | | A |
| I _{EXT} | EXT Current | V _{IN} =4.0V, V _{EXT} =2.0V | 5 | 9 | 15 | mA |
| ΔV _{OUT} /ΔI _{OUT} | Load Regulation | V _{IN} -V _{OUT} =1.0V 1mA ≤ I _{OUT} ≤ 100mA | | | 60 | mV |
| V _{DIF} | Dropout Voltage | I _{OUT} =100mA | | 0.1 | 0.2 | V |
| I _{SS} | Supply Current | V _{CE1} =0V V _{IN} =V _{CE2} =4.2V | | 28 | 56 | μA |
| I _{STANDBY} | Standby Current | V _{IN} =V _{CE} =8.0V | 0.01 | 0.1 | 1.0 | μA |
| I _{EXTLEAK} | EXT Leakage Current | | | | 0.5 | μA |
| ΔV _{OUT} /ΔV _{IN} | Line Regulation | I _{OUT} =50mA V _{OUT} +0.5V ≤ V _{IN} ≤ 8V | 0 | 0.05 | 0.20 | %/V |
| RR | Ripple Rejection Rate | f=1kHz, Ripple 0.5Vp-p V _{IN} -V _{OUT} =1.0V | | 60 | | dB |
| V _{EXT} | EXT Output Voltage | | | | 8 | V |
| I _{LIM} | Current Limit | Base Current, I _B , of External PNP Tr. | 5 | | 15 | mA |
| ΔV _{OUT} /ΔT | Output Voltage Temperature Coefficient | I _{OUT} =10mA -40°C ≤ T _{opt} ≤ 85°C | | ±100 | | ppm/°C |

*NOTE Output Current depends on the external PNP transistor. Use a low saturation transistor with hFE range of 100 to 300.

• VR2

T_{opt}=25°C

| Symbol | Item | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------------------|--|---|-------|-------|-------|------------|
| V _{OUT} | Output Voltage | V _{IN} -V _{OUT} =1.0V I _{OUT} =10mA | 3.234 | 3.300 | 3.366 | V |
| I _{OUT} | Output Current | V _{IN} -V _{OUT} =1.0V | 30 | | | mA |
| ΔV _{OUT} /ΔI _{OUT} | Load Regulation | V _{IN} -V _{OUT} =1.0V 1mA≤I _{OUT} ≤50mA | | 20 | 30 | mV |
| V _{DIF} | Dropout Voltage | I _{OUT} =1mA | | 20 | 30 | mV |
| I _{SS} | Supply Current | V _{CE2} =0V V _{IN} =V _{CE1} =4.2V | | 5 | 10 | μA |
| I _{STANDBY} | Standby Current | V _{IN} =V _{CE} =8.0V | 0.01 | 0.1 | 1.0 | μA |
| ΔV _{OUT} /ΔV _{IN} | Line Regulation | I _{OUT} =30mA V _{OUT} +0.5V≤V _{IN} ≤8V | 0 | 0.05 | 0.20 | %/V |
| RR | Ripple Rejection Rate | f=1kHz, Ripple 0.5Vp-p V _{IN} -V _{OUT} =1.0V | | 40 | | dB |
| ΔV _{OUT} /ΔT | Output Voltage Temperature Coefficient | I _{OUT} =10mA -40°C≤T _{opt} ≤85°C | | ±100 | | ppm/ °C |

• WDT

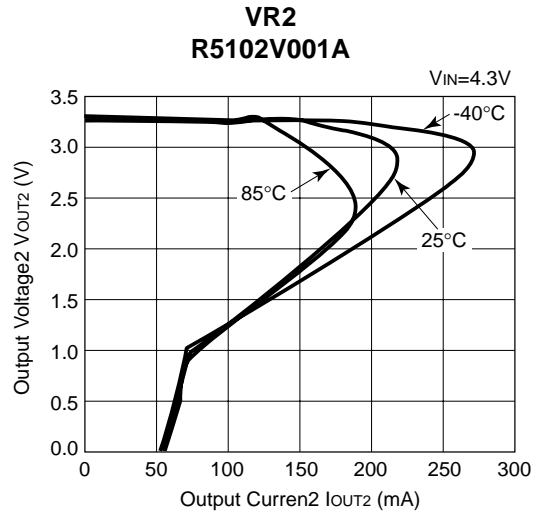
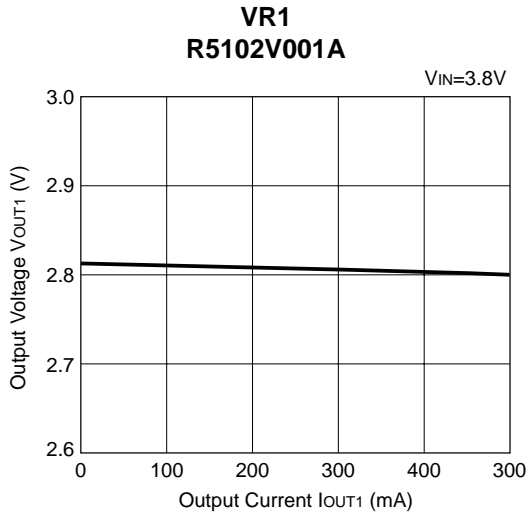
T_{opt}=25°C

| Symbol | Item | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------|--------------------------------------|---|---------------------------|------|---------------------------|------|
| I _{SS} | Supply Current | V _{IN} =V _{CE1} =V _{CE2} =4.2V | | 3 | 6 | μA |
| T _{WD} | Monitoring Time Period of WDT | C=0.68μF | 5 | | 10 | s |
| T _{WR} | Reset Hold Time of WDT | C=0.68μF | 0.5 | | 1.0 | s |
| V _{IHSCK} | SCK "H" Input Voltage | V _{IN} =5.0V | R _{OUT1} ×0.8 | | V _{IN} | V |
| V _{ILSCK} | SCK "L" Input Voltage | V _{IN} =5.0V | 0 | | R _{OUT1} ×0.1 | mV |
| I _{CTW} | CTW Output Current | V _{IN} =1.5V, V _{DS} =0.5V | 1 | 2 | | mA |
| I _{RESET} | RESET Output Current | V _{IN} =1.5V, V _{DS} =0.5V | 1 | 2 | | mA |
| I _{RLEAK} | RESET Leakage Current | V _{IN} =V _{DS} =8V | | | 1 | μA |
| V _{START} | RESET Minimum Operating Voltage | | | 0.8 | 1.5 | V |
| V _{CEH} | R _{OUT1} "H" Output Voltage | | 1.5 | | V _{IN} | V |
| V _{CEL} | R _{OUT1} "L" Output Voltage | | 0 | | 0.25 | V |
| T _{SCKW} | SCK Input Pulse Width | | 500 | | | ns |

TYPICAL CHARACTERISTICS

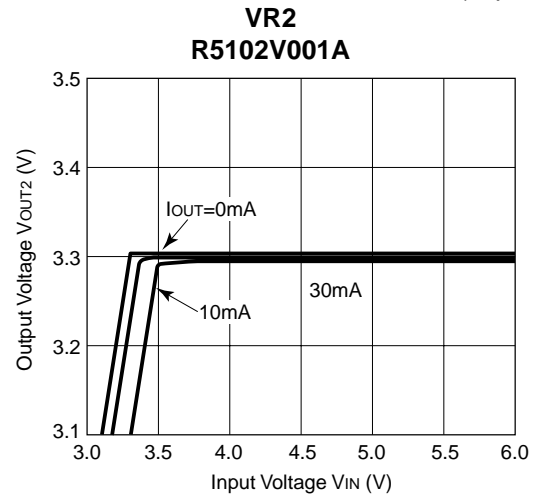
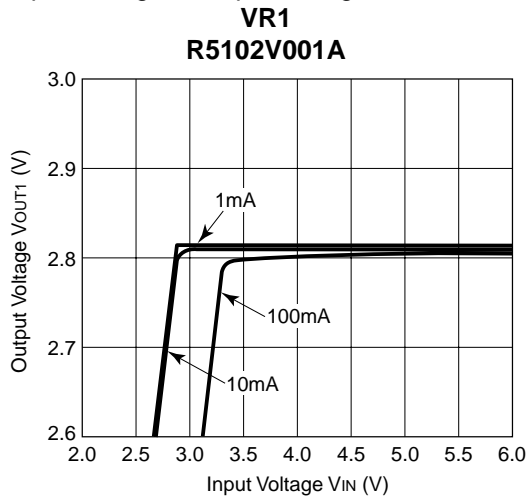
1) Output Voltage vs. Output Current

(Topt=25°C)

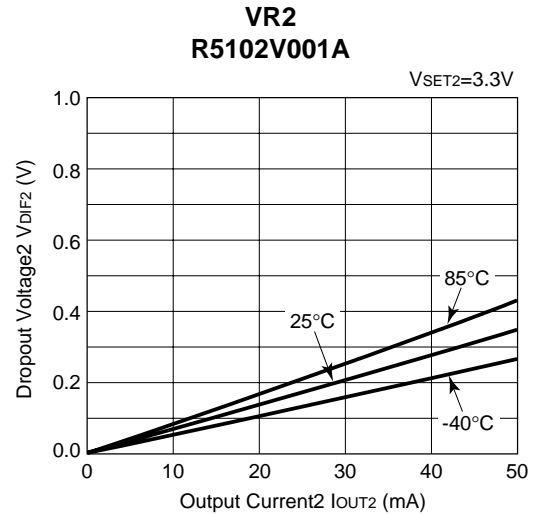
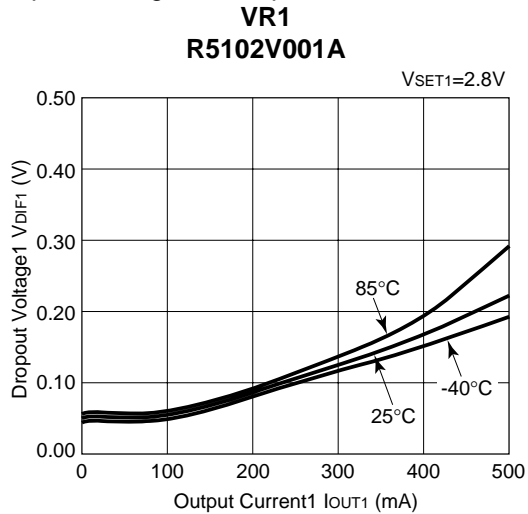


2) Output Voltage vs. Input Voltage

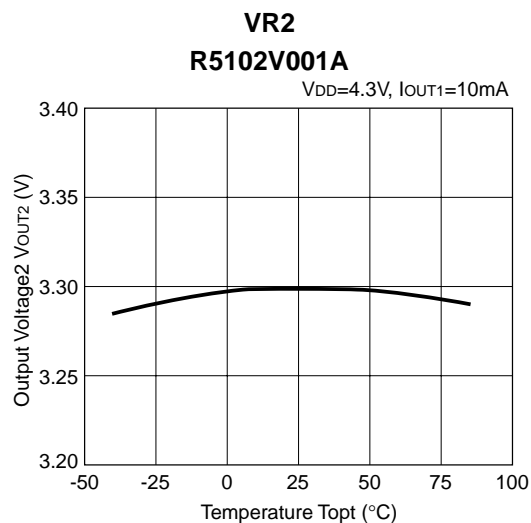
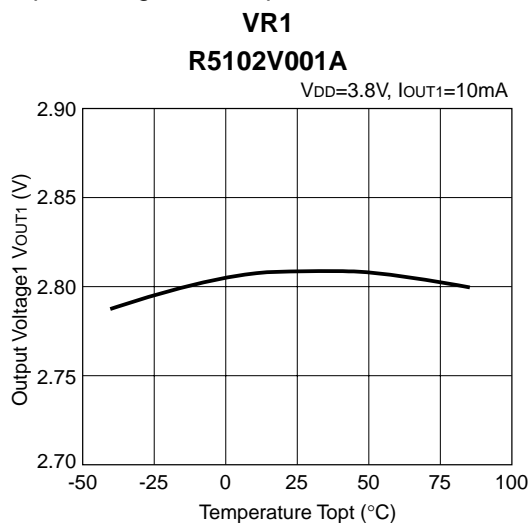
(Topt=25°C)



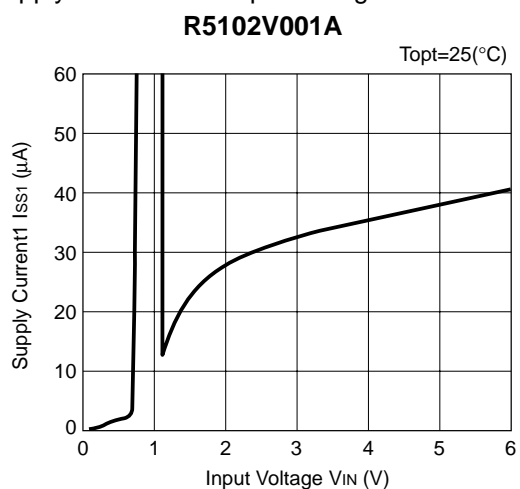
3) Dropout Voltage vs. Output Current



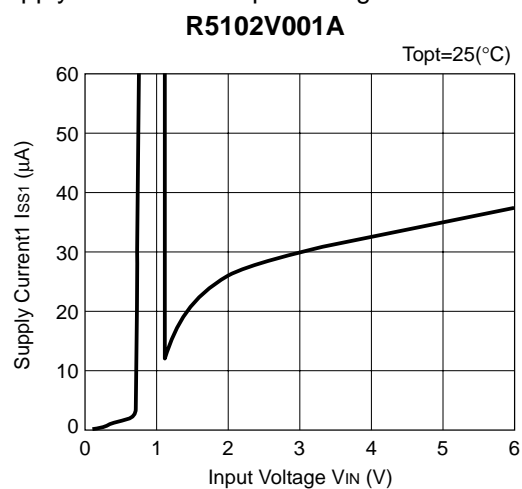
4) Output Voltage vs. Temperature



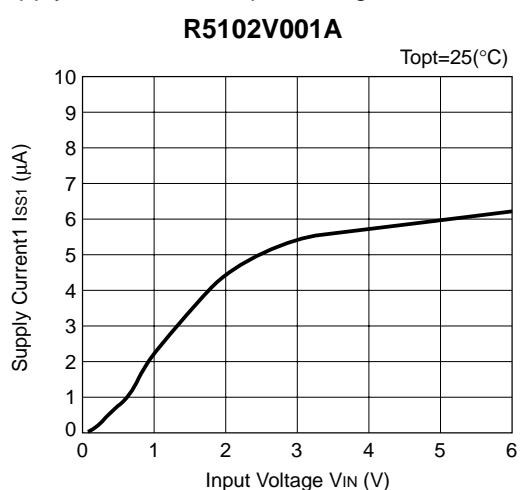
5) Supply Current1 vs. Input Voltage



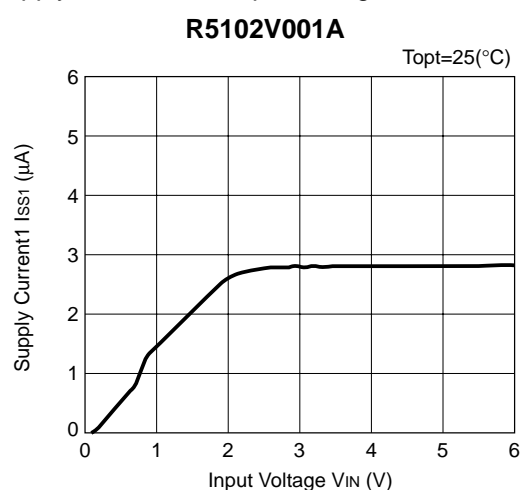
6) Supply Current2 vs. Input Voltage



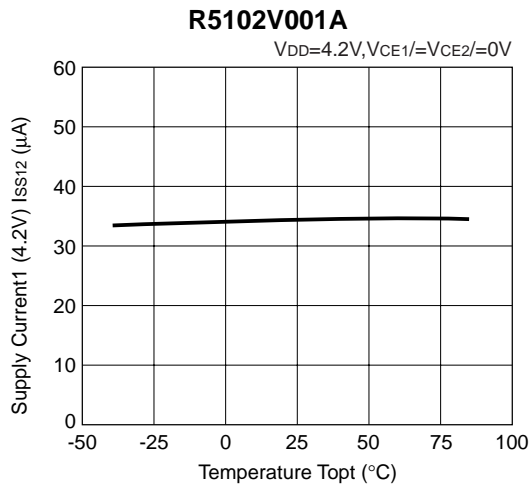
7) Supply Current3 vs. Input Voltage



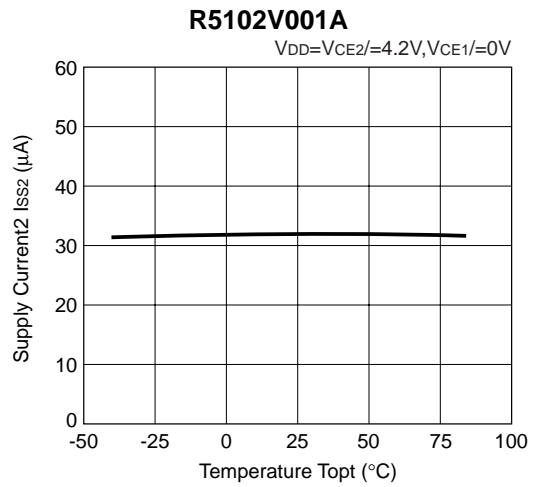
8) Supply Current4 vs. Input Voltage



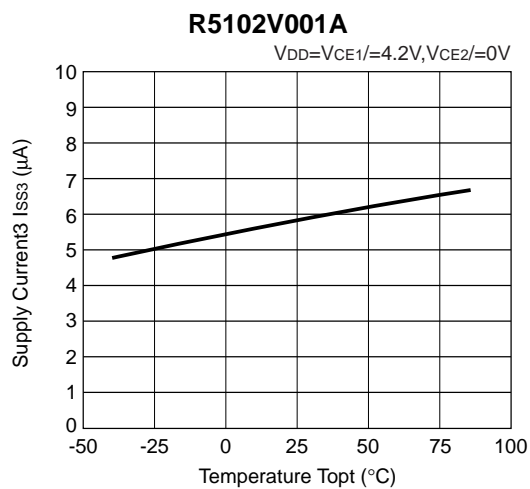
9) Supply Current1 vs. Temperature



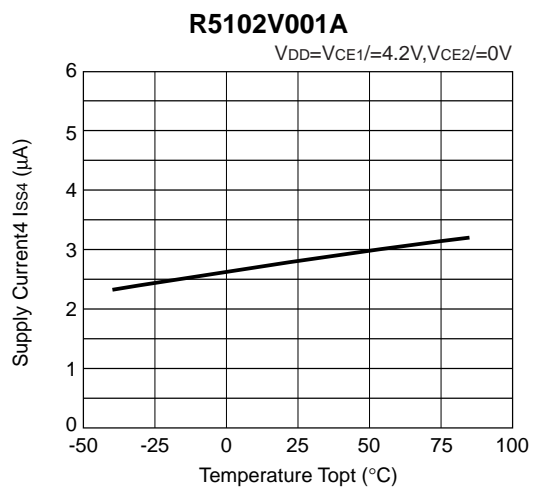
10) Supply Current2 vs. Temperature



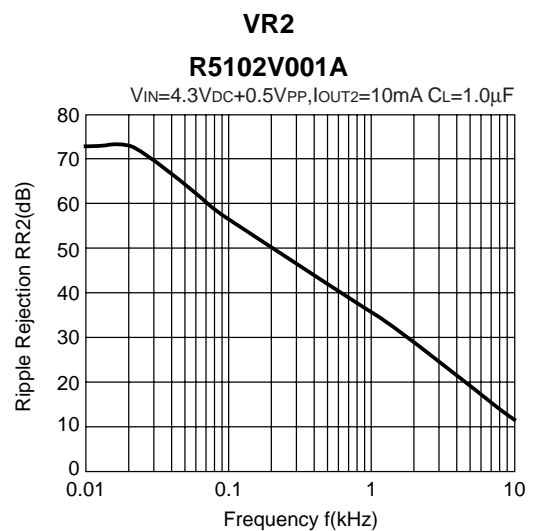
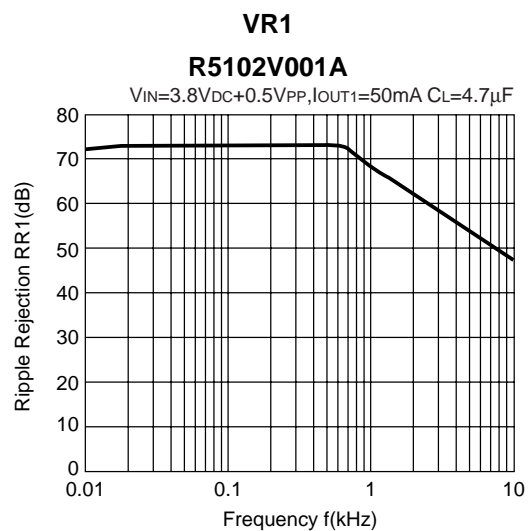
11) Supply Current3 vs. Temperature

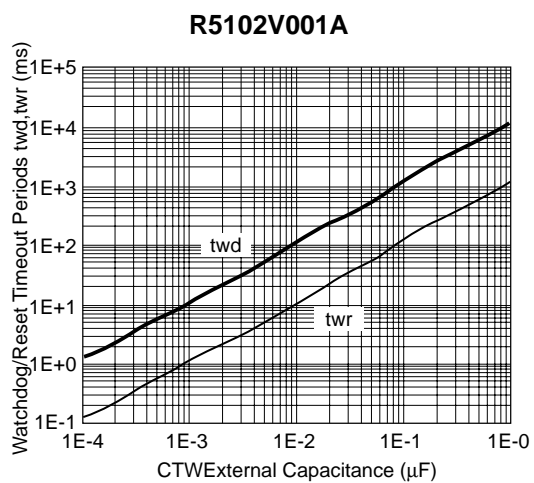


12) Supply Current4 vs. Temperature

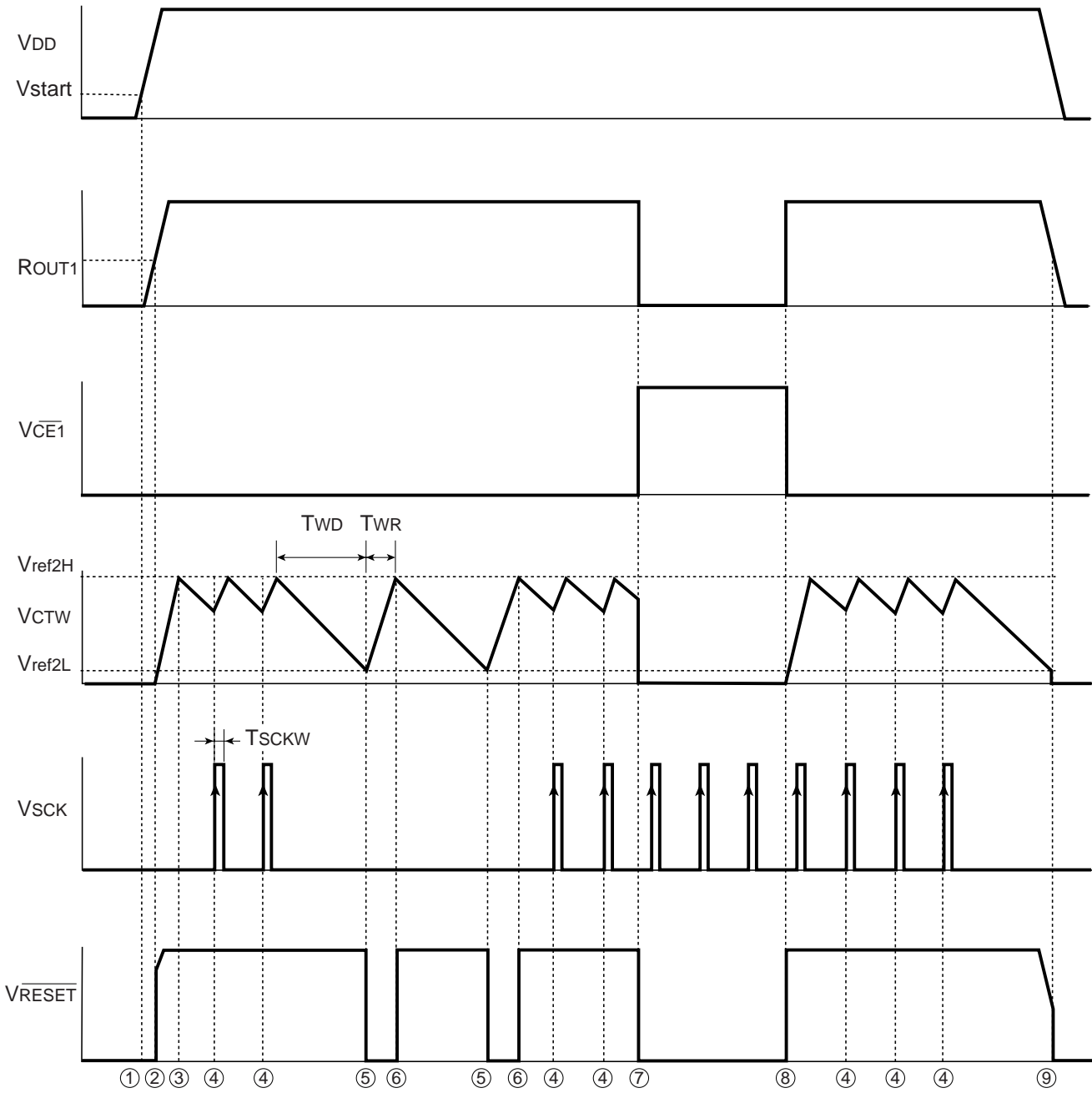


13) Ripple Rejection vs. Frequency



14) WDT Reset and Watchdog Timeout Periods vs. External Capacitance (T_{opt}=25°C)

TIMING DIAGRAM



OPERATION

- ① When V_{DD} is turned on and Input Voltage reaches V_{start} (nearly equal 0.8V), the output of \overline{RESET} pin becomes “L” level.
- ② An External Capacitor starts to be charged through the C_D pin when an Output Voltage of the Voltage Regulator1, V_{OUT1} , equal or more than 1.5V, watchdog timer starts to operate, and the $\overline{V_{RESET}}$ becomes to “H” level.
- ③ The operation mode changes from charging mode to discharging mode through C_{TW} pin when the voltage level of C_{TW} pin, V_{CTW} , reaches to the V_{ref2H} .
- ④ While the C_{TW} pin is on the discharging mode, if a clock pulse is entered (synchronous with a rising edge of the pulse), the operation mode for C_{TW} pin changes from discharging mode to charging mode. And the external capacitor connected to C_{TW} pin is charged until its voltage level reaches to V_{ref2H} .
- ⑤ While the C_{TW} pin is on the discharging mode, if V_{CTW} level drops to V_{ref2L} , about 0.2V without clock pulse to CLK pin, the voltage level of Reset pin becomes from “H” to “L”.
- * Watchdog Timeout period, t_{WD} ,: Discharging Time of C_{TW} pin level from V_{ref2H} to V_{ref2L}
 t_{WD} can be set by connecting an external capacitor to C_w pin, t_{WD} can be calculated as shown below;
 $t_{WD} (ms) \approx 10000 \times C_w (\mu F)$; C_w means a value of an external capacitor connected to C_w pin.
- ⑥ C_{TW} pin mode is changed to charging mode from discharging mode when the Reset signal is generated.
- * Reset timeout period of the watchdog timer, t_{WR} ,: Time interval between Charging time of the C_{TW} pin from V_{ref2L} to V_{ref2H} . t_{WR} can be calculated by the next equation as shown below;
 $t_{WR} (ms) \approx t_{WD}(ms)/10$
- ⑦ When $\overline{CE1}$ pin voltage becomes to equal or more than 1.5V, (or crosses this level from “L” to “H”) and output voltage level of Voltage Regulator 1 becomes to equal or less than 1.5V, watchdog timer stops operation and $\overline{V_{RESET}}$ becomes to “L” level.
- ⑧ The Voltage level of $\overline{CE1}$ pin becomes to equal or less than 0.25V (or crosses this level from “H” to “L”), and output voltage of the Voltage Regulator1 becomes to equal or more than 1.5V, charging to an external capacitor of C_{TW} pin starts and watchdog timer operates, thus $\overline{V_{RESET}}$ becomes to “H” level.
- ⑨ When a Voltage level of V_{DD} pin becomes lower and output voltage of Voltage Regulator 1 becomes to equal or less than 1.5V, the watchdog timer will be halted and $\overline{V_{RESET}}$ becomes to “L” level.

APPLICATION NOTES

Phase Compensation

Phase compensation of VR1 is made by external capacitor to be stable operation under variable output current. Therefore, use a tantalum capacitor, C_L , with a value as much as $10\mu\text{F}$ or more in any case.

If the value of ESR with the capacitor is large, loop oscillation might be occurred to the output. To avoid the case, careful evaluation including the frequency characteristics is required.

External PNP Transistor

When you choose the external transistor; basically consider of output current, input voltage, and power dissipation. Generally, the transistor with low $V_{CE(SAT)}$ and h_{FE} value of which is in the range of 100 to 300, is appropriate.

Mounting on Board

Make the impedance between V_{DD} and GND minimize, otherwise when a large current flows, it would be a cause of making noise and unstable operation. And use a bypass capacitor with a value as much as $10\mu\text{F}$ between V_{DD} pin and GND pin and make its wiring short as possible.

TYPICAL APPLICATION

