FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-28829-1E

ASSP For Screen Display Control

CMOS

On-Screen Display Controller

MB90050

■ DESCRIPTION

The MB90050 is an on-screen display controller for displaying text and graphics on the TV screen.

The MB90050 controls a display area of 35 characters by 16 lines, and provides each character composed of 24 × 32 dots at most. The display functions include a wealth of characters with qualifying functions such as character background shading (shadow casting) , sprite character functions and graphic character functions, contributing to the use of control GUI displays. The MB90050 incorporates display memory (VRAM) , character font ROM, and sync signal generation circuit and video signal generation circuit supporting the NTSC and PAL systems, allowing text and graphics to be displayed in conjunction with a small number of external components.

■ FEATURES

- Main screen display capacity
  35 characters × 16 lines (maximum 560 characters)
- Character configuration
  Normal characters : 24 × 32 dots
  Graphic characters : 12 × 16 dots* (colorable per 1 dot)

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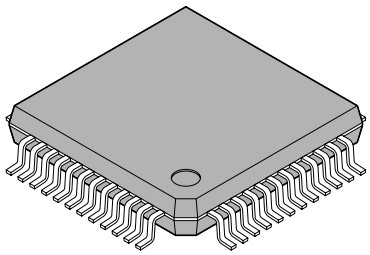
■ PACKAGE

48-pin plastic QFP



(FPT-48P-M15)

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- Font display configuration
  Three horizontal width settings (selectable setting L/M/S for each character) per character.
  L size : 24 dots
  M size : 18 dots
  S size : 12 dots
  Two vertical height settings (selectable A/B for each line) per line.
  A : 18 to 32 dots (setting per 2 dots)
  B : 18 to 32 dots (setting per 2 dots)
  (These sizes are dot sizes of typical character. Each size of graphic characters uses half the number of dots of typical characters. Note, however, that both of the typical and graphic characters are the same in character area size.
- Character types
  Usable all 512 character types (font ROM+, font RAM)
  Font ROM : 512 character types (all area user setting)
  Font RAM : 8 character types (all area user command setting)
  Capable of setting a specific eight-character area in font ROM so that the area is replaced with font RAM.
- Display modes
  Character : Normal character/graphic character (set for each character)
  Character trimming : Side trimming 1/side trimming 2/patern background 1/patern background 2 (set for each screen)
  Character background : None/Solid-fill/Shaded background (concave) /Shaded background (convex) (set for each character)
  Line background : None/Solid-fill/Shaded background (concave) /Shaded background (convex) (set for each line)
  Character enlargement : Normal, Double width, Double height, Double width × double height (set for each line)
  Brink : OFF/ON (set for each character)
- Main screen display position control
  Horizontal display position : Control in 2-dot units (movable through the entire screen)
  Vertical display position : Control in 2-dot units (movable through the entire screen)
  Line spacing control : 0 to 14 dots, 2-dot units (set for each line)
  Sprite character display control
  Capable of displaying one block for an arbitrary character on the topmost layer on the screen.
  Sprite character display : OFF/ON (graphic character display)
  Sprite character types : 256 types (character codes 000_H to $0FF_H$)
  Sprite character configuration : 1 character/2 characters horizontal/2 characters vertical/ 2×2 characters
  Sprite character horizontal display position : Control in 1-dot units
  Sprite character vertical display position : Control in 1-dot units
  Screen background color display control
  Capable of displaying an arbitrary color on the entire bottommost layer on the screen.
  Screen background color display : OFF/ON
- Display colors
  Digital output : 16 colors selectable from among 64 colors (built in palette circuit)
  Video output : Any 16 colors selectable (Command setting enable)

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- Display colors and setting units

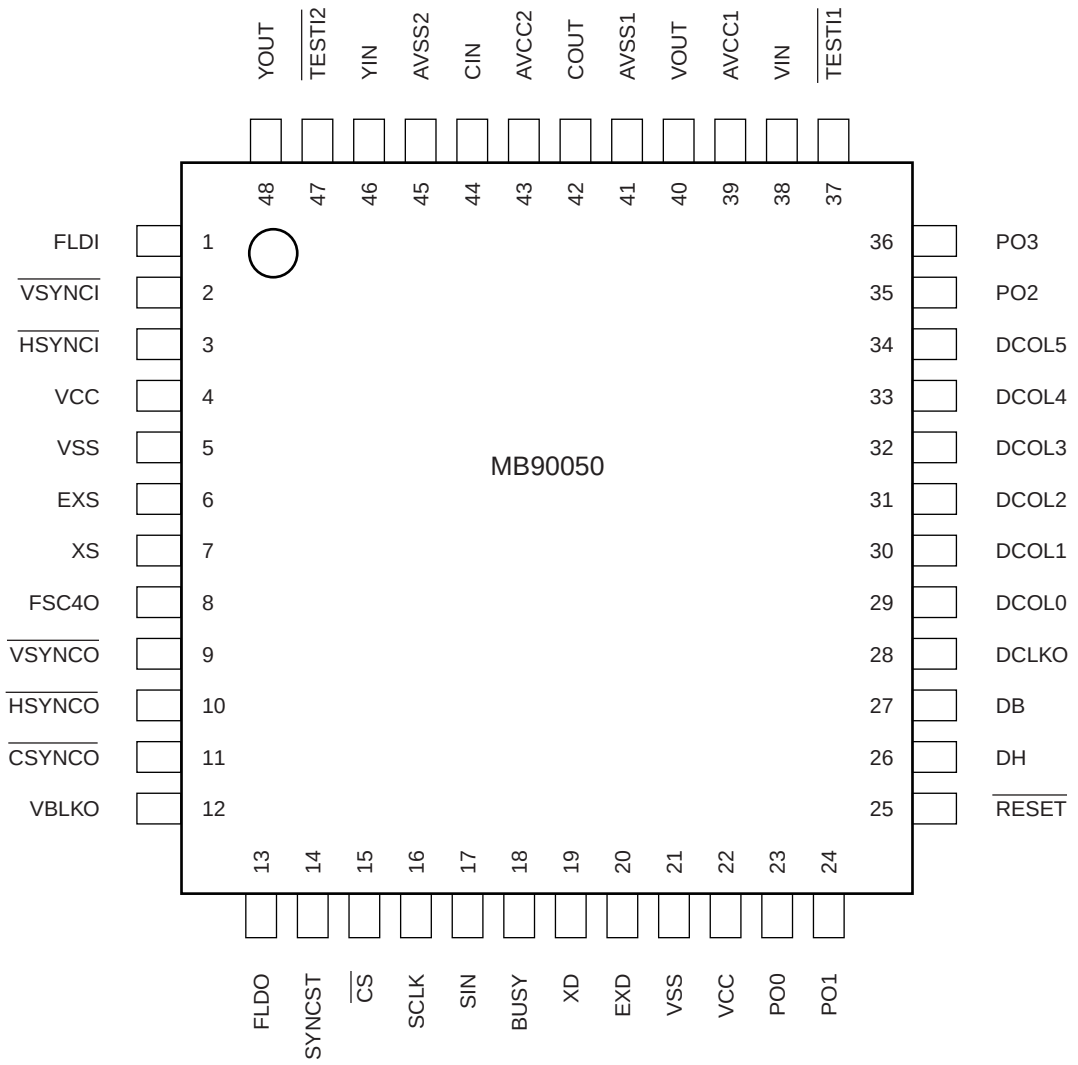
Character color	: 16 colors (set for each character)
Character background color	: 16 colors (set for each character)
Character trimming color	: 16 colors (set for each line)
Line background color	: 16 colors (set for each line)
Graphic character color	: 16 colors (set for each dot)
Sprite character color	: 16 colors (set for each dot)
Screen background character color	: 16 colors (set for each dot)
Screen background color	: 16 colors (set for all screen)
Shaded background frame highlight color	: 16 colors (set for all screen)
Shaded background frame shadow color	: 16 colors (set for all screen)

- Digital display signal output
  Color signal output : DCOL5 to DCOL0 pins (6 bits)
  Display period signal output : VOB1 pin
  Translucent display period signal output : VOB2 pin
- Analog (video) signal input/output
  Composit video input/output : VIN, VOUT pins
  Y/C video input/output : YIN, YOUT pins, CIN, COUT pins
- Internal sync control
  Internal sync signal generator and video signal generator supporting the NTSC and PAL systems.
- External interface
  16-bit serial input (3-signal input)
  Chip select signal
  Serial clock signal
  Serial data signal
- Package
  QFP-48 (FPT-48P-M15)
- Supply voltage
  +5 V±10%

* : 1 dot of graphic characters is the same size as 2 × 2 dots of normal characters.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-48P-M15)

■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O	Circuit type	Function
6 7	EXS XS	I/O	A	Crystal oscillation circuit pins for color burst clock generator. Connect an external crystal oscillator (14.31818 MHz for NTSC or 17.734475 MHz for PAL) and load capacitance (C) to these pins to form a crystal oscillation circuit.
20 19	EXD XD	I/O	B	LC oscillation circuit pins for display dot clock generator. Connect these pins to external “L” and “C” to from an LC oscillation circuit.
15	$\overline{CS}$	I	C	Chip select signal input pin. For serial command transfer, set this pin to the Low level.
16	SCLK	I	C	Serial clock signal input pin. This pin feeds a clock signal upon transfer of a serial command. It feeds serial data at the rising edge.
17	SIN	I	C	Serial data signal input pin. Input data during serial command transfer.
18	BUSY	O	F	Busy signal output pin. This pin outputs a significant level signal during VRAM filling. Do not input a serial command while the pin outputs the significant level signal. Supplying a low level signal to the $\overline{CS}$ pin during the significant level signal output period terminates the VRAM fill operation and causes this pin to output an insignificant level signal. The pin enables output (ON/OFF) control, output logic control, and internal pull-up ON/OFF control depending on the command setting. The pin can also serve as the ACK signal output pin using the command setting for output selection control (BUS = 1). In this case, the pin outputs the significant level signal upon completion of VRAM filling. When the $\overline{RESET}$ pin inputs a low level signal, this pin outputs the busy signal, turns off the internal pull-up resistor, and sets the output to OFF (output tied to the low).
2	$\overline{VSYNCI}$	I	D	Vertical sync signal input pin. (The input signal to this pin is disabled when the composite sync signal input is selected by the command setting.) Active low signal or active high signal input is command-selectable for the pin. When the $\overline{RESET}$ pin inputs the low level signal, this pin inputs the active low signal.
3	$\overline{HSYNCI}$	I	D	Horizontal sync signal input pin. (This pin can also serve as a composite sync signal input pin with the command setting.) Active low signal or active high signal input is command-selectable for the pin. When the $\overline{RESET}$ pin inputs the low level signal, this pin inputs the active low, horizontal sync signal.
1	FLDI	I	D	Field signal input pin. The internal field signal identically detected from among input sync signals or the input signal to this pin is command-selectable for field control. During operation under external synchronization control, the input signal is used to control the least significant bit of the font ROM/RAM raster address. The input signal to this pin is disabled during operation under internal synchronization control.

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Pin no.	Pin name	I/O	Circuit type	Function
9	$\overline{\text{VSYNCO}}$	O	F	Vertical sync signal output pin. The pin enables output (ON/OFF) control, output logic control, and internal pull-up ON/OFF control depending on the command setting. When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin turns off the internal pull-up resistor and sets the output to OFF (output tied to the high).
10	$\overline{\text{HSYNCO}}$	O	F	Horizontal sync signal output pin. The pin enables output (ON/OFF) control, output logic control, and internal pull-up ON/OFF control depending on the command setting. When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin turns off the internal pull-up resistor and sets the output to OFF (output tied to the high).
11	$\overline{\text{CSYNCO}}$	O	F	Composite sync signal output pin. The pin enables output (ON/OFF) control, output logic control, and internal pull-up ON/OFF control depending on the command setting. When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin turns off the internal pull-up resistor and sets the output to OFF (output tied to the high).
12	VBLKO	O	F	Vertical blanking interval (VBI) output pin. The pin enables output (ON/OFF) control, output logic control, and internal pull-up ON/OFF control depending on the command setting. When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin turns off the internal pull-up resistor and sets the output to OFF (output tied to the low).
13	FLDO	O	F	Field signal output pin. During operation under internal synchronization control, this pin outputs the internally generated field signal. During operation under external synchronization control, the pin outputs the field signal (internally detected field signal or external input field signal) used for internal operations. The pin enables output (ON/OFF) control, output logic control, and internal pull-up ON/OFF control depending on the command setting. When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin turns off the internal pull-up resistor and sets the output to OFF (output tied to the low).
14	SYNCST	O	F	Synchronization detection signal output pin. This pin outputs a significant level signal with a sync signal detected and an insignificant level signal with no sync signal detected. The pin enables output (ON/OFF) control, output logic control, and internal pull-up ON/OFF control depending on the command setting. When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin turns off the internal pull-up resistor and sets the output to OFF (output tied to the low).

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Pin no.	Pin name	I/O	Circuit type	Function
28	DCLKO	O	G	Dot clock signal output pin. This pin outputs an LC oscillation clock signal. The pin enables output (ON/OFF) control depending on the command setting. The normal clock (that stops oscillation during horizontal synchronization) or continuous clock (that does not stop oscillation during horizontal synchronization) can be command-selected for the output using the command setting for output selection control (CKS). When the $\overline{\text{TESTI2}}$ pin inputs a low level signal, this pin outputs the continuous clock signal that does not stop oscillation during horizontal synchronization (where the output selection control (CKS) setting is disabled). When the $\overline{\text{RESET}}$ pin inputs the low level signal, the pin outputs a dot clock signal.
8	FSC4O	O	G	Crystal oscillator 4FSC clock signal output pin. This pin enables output (ON/OFF) control depending on the command setting. The crystal oscillation clock (4FSC) or its 1/4 frequency clock (FSC) can be command-selected for the output using the command setting for output selection control (FSS). When the $\overline{\text{TESTI2}}$ pin inputs the low level signal, this pin outputs the 4FSC clock signal (where the output selection control (FSS) setting is disabled). When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin outputs the 4FSC clock signal.
26	DH	I/O	H	Halftone display period signal output pin. This pin enables output (ON/OFF) control and output logic control depending on the command setting. When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin sets the output to OFF (output tied to the low). (The input feature of the pin is a test function. Use the pin usually only for output.)
27	DB	I/O	H	Display period signal output pin. This pin enables output (ON/OFF) control and output logic control depending on the command setting. When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin sets the output to OFF (entering the low level signal fixed output state). (The input feature of the pin is a test function. Use the pin usually only for output.)
34 33 32 31 30 29	DCOL5 DCOL4 DCOL3 DCOL2 DCOL1 DCOL0	I/O	H	Display color signal output pin. This pin enables output (ON/OFF) control and output logic control depending on the command setting. When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin sets the output to OFF (entering the low level signal fixed output state). (The input feature of the pin is a test function. Use the pin usually only for output.)
36 35 24 23	PO3 PO2 PO1 PO0	I/O	H	Port signal output pin. This pin enables output level (High/Low) control depending on the command setting. When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin sets the output to OFF (entering the low level signal fixed output state). (The input feature of the pin is a test function. Use the pin usually only for output.)

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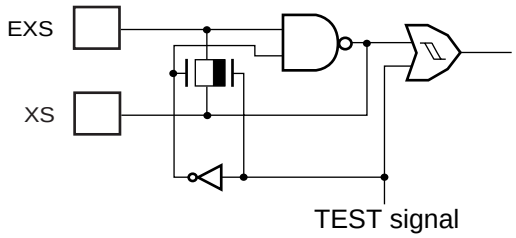
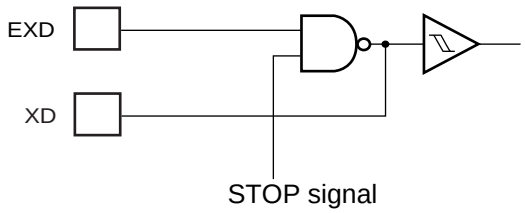
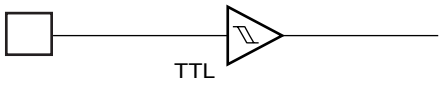
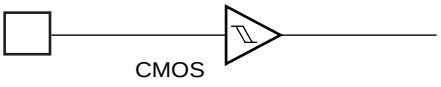
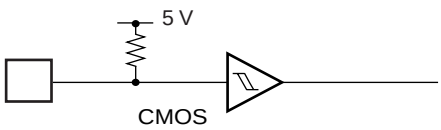
Pin no.	Pin name	I/O	Circuit type	Function
25	$\overline{\text{RESET}}$	I	C	Reset signal input pin. Upon input of the low level signal, this pin causes an internal reset. After the power supply is inserted, the reset input is required for normal operation. During regular operation, the pin inputs the high level signal.
37	$\overline{\text{TESTI1}}$	I	E	Test signal input pin. Input High level signal during normal operation. (Input of the Low level signal activates test mode operation.)
47	$\overline{\text{TESTI2}}$	I	E	Test signal input pin. Input High level signal during normal operation.
38	VIN	I	I	Composite video signal input pin. This pin inputs a DC-reproduced signal of 2 V_{P-P} (pedestal level 1.57 V, sync tip level 1 V) .
46	YIN	I	I	Luminance video signal (Y video signal) input pin. This pin inputs a DC-reproduced signal of 2 V_{P-P} (pedestal level 1.57 V, sync tip level 1 V) .
44	CIN	I	I	Saturation video signal (C video signal) input pin. This pin inputs a signal at 1.57 VDC and a color burst signal amplitude of 0.57 V_{P-P}.
40	VOUT	O	I	Composite video signal output pin. This pin outputs a signal of 2 V_{P-P} (pedestal level 1.57 V, sync tip level 1 V) . When the $\overline{\text{RESET}}$ signal inputs the low level signal, this pin outputs the black video (pedestal level without color burst) signal.
48	YOUT	O	I	Luminance video signal (Y video signal) output pin. This pin outputs a signal of 2 V_{P-P} (pedestal level 1.57 V, sync tip level 1 V) . When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin outputs the black video (pedestal level) signal.
42	COUT	O	I	Saturation video signal (C video signal) output pin. This pin outputs a signal at 1.57 VDC and a color burst signal amplitude of 0.57 V_{P-P}. When the $\overline{\text{RESET}}$ pin inputs the low level signal, this pin outputs the black video signal (a DC voltage of 1.57 V without color burst).
4 22	VCC	—	—	Power supply pin for digital circuit. These pins supply +5 V and make all VCC pins same potential.
5 21	VSS	—	—	Digital ground pins. These pins make all VSS pins and AVSS1/AVSS2 pins same potential.
39	AVCC1	—	—	Power supply pin for analog circuit and composite video signal Input/Output (VIN-VOUT) circuit. This pin supplies +5 V. Input analog ground level when not using this analog circuit.
43	AVCC2	—	—	Power supply pin for analog circuit, luminance video signal Input/Output (YIN-YOUT) circuit, and saturation video signal Input/Output (CIN-COUT) circuit. This pin supplies +5 V. Input analog ground level when not using this analog circuit.
41 45	AVSS1 AVSS2	—	—	Analog ground pins. These pins make AVSS1/AVSS2 pins and VSS pins same potential.

Note :
A : Crystal oscillation
B : LC oscillation
C : TTL level, Hysteresis input
D : CMOS level, Hysteresis input
E : CMOS level, Hysteresis input, with pull-up resistor (approx. 50 kΩ)
F : Open-drain output, with pull-up resistor SW (approx. 50 kΩ)
G : CMOS output
H : CMOS I/O (Input is for test.)
I : Analog I/O

■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A		• Crystal oscillation Oscillator feedback resistor (approx. 1MΩ)
B		• LC oscillation
C		• TTL hysteresis input
D		• CMOS hysteresis input
E		• CMOS hysteresis input with pull-up resistor (approx. 50 kΩ)

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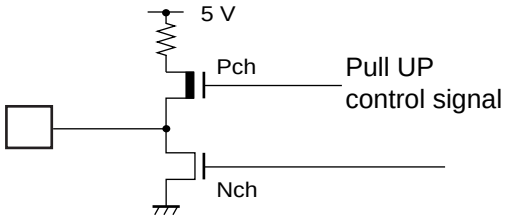
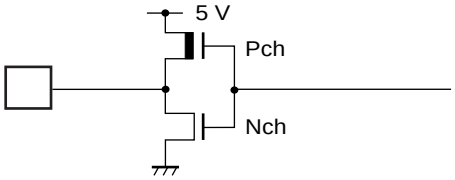
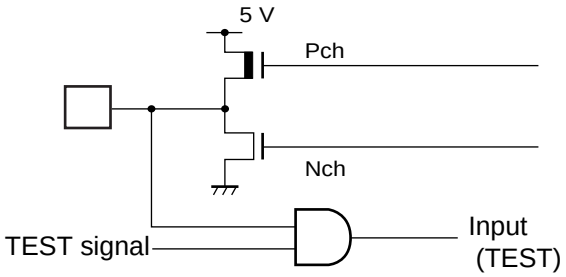
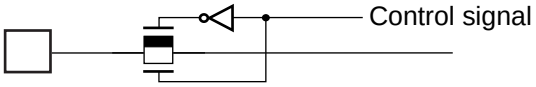
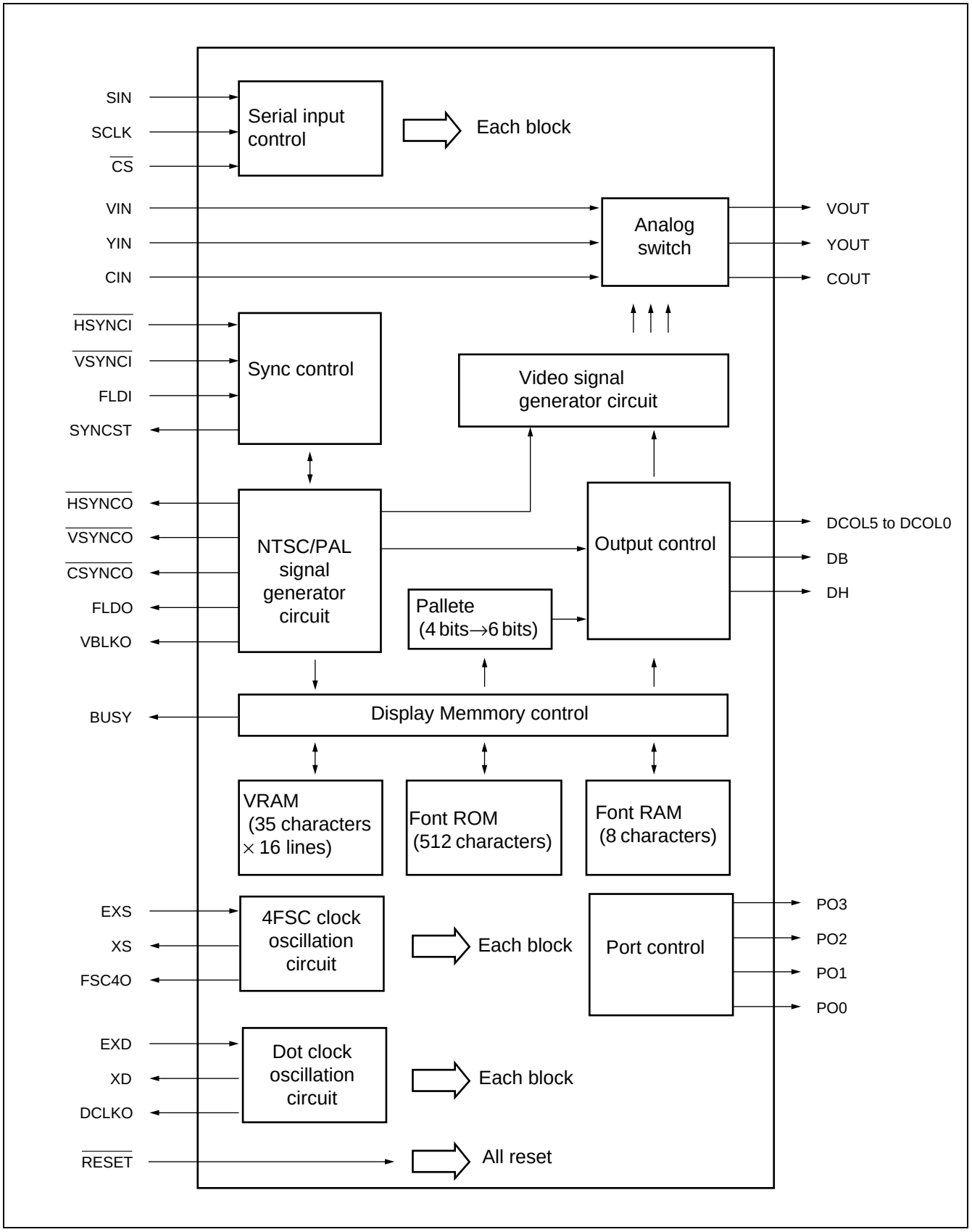
Type	Circuit	Remarks
F		• Nch open-drain output with pull-up resistor SW (approx. 50 kΩ)
G		• CMOS output
H		• CMOS I/O Input is for test.
I		• Analog I/O CMOS analog SW

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{DD}	V_{SS} – 0.5	V_{SS} + 7.0	V	
Input voltage	V_{IN}	V_{SS} – 0.5	V_{DD} + 0.5	V	
Output voltage	V_{OUT}	V_{SS} – 0.5	V_{DD} + 0.5	V	
Power consumption	P_d	—	500	mW	
Operating temperature	Ta	–40	+85	°C	
Storage temperature	T_{stg}	–55	+125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks (circuit type)
		Min	Max		
Power supply voltage	V_{DD}	4.5	5.5	V	
"H" level input voltage	V_{IH1}	0.7 × V_{DD}	V_{DD} + 0.3	V	G
	V_{IH1S}	0.8 × V_{DD}	V_{DD} + 0.3	V	D, E
	V_{IH2S}	0.6 × V_{DD}	V_{DD} + 0.3	V	C
"L" level input voltage	V_{IL1}	V_{SS}–0.3	0.3 × V_{DD}	V	G
	V_{IL1S}	V_{SS}–0.3	0.2	V	D, E
	V_{IL2S}	V_{SS}–0.3	0.6	V	C
Analog input voltage	A_{VIN}	0	V_{DD}	V	
Operating temperature	T_a	–40	+85	°C	

Notes : • Do not make a potential difference between AVSS (AVSS1/2) and VSS.
- It is possible to set AVCC1 = AVSS when not using composite video signal (VIN-VOUT pins) .
- It is possible to set AVCC2 = AVSS when not using Y/C separated video signals (YIN-YOUT and CIN-COUT pins) .

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(Ta = –40 °C to +85 °C, V_{SS} = 0 V)

Parameter	Sym-bol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
“H” level output voltage	V_{OH}	All output pins	VCC = 4.5 V, IOH = –4.0 mA	4.0	—	—	V
“L” level output voltage	V_{OL}	All output pins	VCC = 4.5 V, IOL = 4.0 mA	—	—	0.4	V
Pull-up resistor	R_P	E, F	VCC = 5.5V	25	50	200	kΩ
Power supply current	I_{DD}	VCC	VCC = 5.5 V, 4FSC = 20 MHz, DCLK = 20 MHz	—	35	45	mA
Analog power supply current	I_A	AVCC1, AVCC2	VCC = AVCC1 = AVCC2 = 5.5 V, 4FSC = 0 MHz, VIN, YIN, CIN = 1.65V, No load	—	22	40	mA
ON resistor	R_{ON}	VIN-VOUT, YIN-YOUT, CIN-COUT	VCC = AVCC1 = AVCC2 = 4.5 V, IOL = 100 μA	—	215	310	Ω
OFF leak current	I_{OFF}	VIN, YIN, CIN	VCC = AVCC1 = AVCC2 = 5.5 V, VIN, YIN, CIN = 5.5V	—	0.1	10	μA
Output resistor	R_{OUT}	VOUT, YOUT, COUT	VCC = AVCC1 = AVCC2 = 4.5 V, IOL = 100 μA	100	—	1800	Ω

Analog Ladder Voltage

(AVCC = AVCC1 = AVCC2 = 5.0 V)

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
VOHR0	Resistance ladder voltage 00 (–40 IRE)	930	1000	1040	mV
VOHR1	Resistance ladder voltage 01 (–36 IRE)	988	1057	1098	mV
VOHR2	Resistance ladder voltage 02 (–32 IRE)	1046	1114	1156	mV
VOHR3	Resistance ladder voltage 03 (–28 IRE)	1104	1171	1214	mV
VOHR4	Resistance ladder voltage 04 (–24 IRE)	1162	1229	1272	mV
VOHR5	Resistance ladder voltage 05 (–20 IRE)	1220	1286	1330	mV
VOHR6	Resistance ladder voltage 06 (–16 IRE)	1278	1343	1388	mV
VOHR7	Resistance ladder voltage 07 (–12 IRE)	1336	1400	1446	mV
VOHR8	Resistance ladder voltage 08 (–8 IRE)	1394	1457	1504	mV
VOHR9	Resistance ladder voltage 09 (–4 IRE)	1452	1514	1562	mV
VOHR10	Resistance ladder voltage 10 (0 IRE)	1510	1571	1620	mV
VOHR11	Resistance ladder voltage 11 (4 IRE)	1568	1629	1678	mV
VOHR12	Resistance ladder voltage 12 (8 IRE)	1626	1686	1736	mV
VOHR13	Resistance ladder voltage 13 (12 IRE)	1684	1743	1794	mV
VOHR14	Resistance ladder voltage 14 (16 IRE)	1742	1800	1852	mV
VOHR15	Resistance ladder voltage 15 (20 IRE)	1800	1857	1910	mV
VOHR16	Resistance ladder voltage 16 (24 IRE)	1858	1914	1968	mV
VOHR17	Resistance ladder voltage 17 (28 IRE)	1916	1971	2026	mV
VOHR18	Resistance ladder voltage 18 (32 IRE)	1974	2029	2084	mV
VOHR19	Resistance ladder voltage 19 (36 IRE)	2032	2086	2142	mV
VOHR20	Resistance ladder voltage 20 (40 IRE)	2090	2143	2200	mV
VOHR21	Resistance ladder voltage 21 (44 IRE)	2148	2200	2258	mV
VOHR22	Resistance ladder voltage 22 (48 IRE)	2206	2257	2316	mV
VOHR23	Resistance ladder voltage 23 (52 IRE)	2264	2314	2374	mV
VOHR24	Resistance ladder voltage 24 (56 IRE)	2322	2371	2432	mV
VOHR25	Resistance ladder voltage 25 (60 IRE)	2380	2429	2490	mV
VOHR26	Resistance ladder voltage 26 (64 IRE)	2438	2486	2548	mV
VOHR27	Resistance ladder voltage 27 (68 IRE)	2496	2543	2606	mV
VOHR28	Resistance ladder voltage 28 (72 IRE)	2554	2600	2664	mV
VOHR29	Resistance ladder voltage 29 (76 IRE)	2612	2657	2722	mV
VOHR30	Resistance ladder voltage 30 (80 IRE)	2670	2714	2780	mV
VOHR31	Resistance ladder voltage 31 (84 IRE)	2728	2771	2838	mV
VOHR32	Resistance ladder voltage 32 (88 IRE)	2786	2829	2896	mV
VOHR33	Resistance ladder voltage 33 (92 IRE)	2844	2886	2954	mV
VOHR34	Resistance ladder voltage 34 (96 IRE)	2902	2943	3012	mV
VOHR35	Resistance ladder voltage 35 (100 IRE)	2960	3000	3070	mV

Note : Refer to “VOUT Output”, “YOUT Output” and “COUT Output” about output waveform images.

MB90050 Palette Initial Value

- Pedestal level

Color code	Comment	Relative value	Absolute value	Register setting value
		PED (IRE)	PED (IRE)	PED (HEX)
—	Pedestal	0	40	0A

- Sink chip level

Color code	Comment	Relative value	Absolute value	Register setting value
		SYN (IRE)	SYN (IRE)	SYN (HEX)
—	Sink chip	–40	0	00

- Translucence level

Color code	Comment	Relative value	Absolute value	Register setting value
		HAN (IRE)	HAN (IRE)	HAN (HEX)
—	translucence	32	72	12

- Color burst level

Color code	Comment	Relative value				Absolute value				Register setting value			
		BST0 (IRE)	BST1 (IRE)	BST2 (IRE)	BST3 (IRE)	BST0 (IRE)	BST1 (IRE)	BST2 (IRE)	BST3 (IRE)	BST0 (HEX)	BST1 (HEX)	BST2 (HEX)	BST3 (HEX)
—	Burst	0	–24	0	24	40	16	40	64	0A	04	0A	10

- Y (COLOR)

Color code	Comment	Relative value	Absolute value	Register setting value
		Luminance (IRE)	YD (IRE)	YD (HEX)
15	White-1	100	140	23
14	Yellow-1	72	112	1C
13	Cyan-1	64	104	1A
12	Green-1	56	96	18
11	Magenta-1	40	80	14
10	Red-1	32	72	12
9	Blue-1	24	64	10
8	Black-1	16	56	0E
7	White-0	92	132	21
6	Yellow-0	64	104	1A
5	Cyan-0	56	96	18
4	Green-0	48	88	16
3	Magenta-0	32	72	12
2	Red-0	24	64	10
1	Blue-0	16	56	0E
0	Black-0	8	48	0C

• C (COLOR)

Color code	Comment	Relative value		Absolute value				Register setting value			
		Phase (degrees)	Amplitude (IRE)	0	90	180	270	CD0 (HEX)	CD1 (HEX)	CD2 (HEX)	CD3 (HEX)
15	White-1	0	0	40	40	40	40	0A	0A	0A	0A
14	Yellow-1	195	20	35	21	45	59	09	05	0B	0F
13	Cyan-1	284	36	5	49	75	31	01	0C	13	08
12	Green-1	241	30	14	25	66	55	03	06	11	0E
11	Magenta-1	61	30	66	55	14	25	11	0E	03	06
10	Red-1	104	36	75	31	5	49	13	08	01	0C
9	Blue-1	15	20	45	59	35	21	0B	0F	09	05
8	Black-1	0	0	40	40	40	40	0A	0A	0A	0A
7	White-0	0	0	40	40	40	40	0A	0A	0A	0A
6	Yellow-0	195	20	35	21	45	59	09	05	0B	0F
5	Cyan-0	284	36	5	49	75	31	01	0C	13	08
4	Green-0	241	30	14	25	66	55	03	06	11	0E
3	Magenta-0	61	30	66	55	14	25	11	0E	03	06
2	Red-0	104	36	75	31	5	49	13	08	01	0C
1	Blue-0	15	20	45	59	35	21	0B	0F	09	05
0	Black-0	0	0	40	40	40	40	0A	0A	0A	0A

• V (COLOR)

Color code	Comment	Absolute value				Register setting value			
		0	90	180	270	VD0 (HEX)	VD1 (HEX)	VD2 (HEX)	VD3 (HEX)
15	White-1	140	140	140	140	23	23	23	23
14	Yellow-1	107	93	117	131	1B	17	1D	21
13	Cyan-1	69	113	139	95	11	1C	23	18
12	Green-1	70	81	122	111	11	14	1F	1C
11	Magenta-1	106	95	54	65	1B	18	0D	10
10	Red-1	107	63	37	81	1B	10	09	14
9	Blue-1	69	83	59	45	11	15	0F	0B
8	Black-1	56	56	56	56	0E	0E	0E	0E
7	White-0	132	132	132	132	21	21	21	21
6	Yellow-0	99	85	109	123	19	15	1B	1F
5	Cyan-0	61	105	131	87	0F	1A	21	16
4	Green-0	62	73	114	103	0F	12	1D	1A
3	Magenta-0	98	87	46	57	19	16	0B	0E
2	Red-0	99	55	29	73	19	0E	07	12
1	Blue-0	61	75	51	37	0F	13	0D	09
0	Black-0	48	48	48	48	0C	0C	0C	0C

• M (MONO)

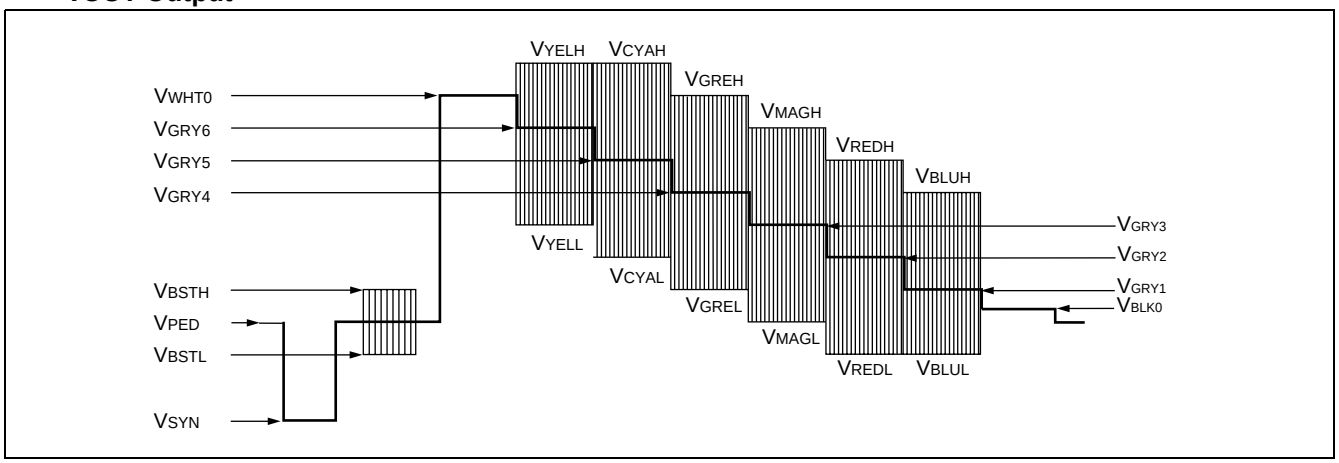
Color code	Comment	Relative value	Absolute value	Register setting value
		Luminance (IRE)	MD (IRE)	MD (HEX)
15	Level-17	100	140	23
14	Level-16	80	120	1E
13	Level-15	68	108	1B
12	Level-14	60	100	19
11	Level-13	44	84	15
10	Level-12	36	76	13
9	Level-11	24	64	10
8	Level-10	16	56	0E
7	Level-07	92	132	21
6	Level-06	72	112	1C
5	Level-05	60	100	19
4	Level-04	52	92	17
3	Level-03	36	76	13
2	Level-02	28	68	11
1	Level-01	16	56	0E
0	Level-00	8	48	0C

Note : Minimum value for absolute value of IRE is 0.
Maximum value for absolute value of IRE is 140.
Relative value is the value when the pedestal level is 0IRE.

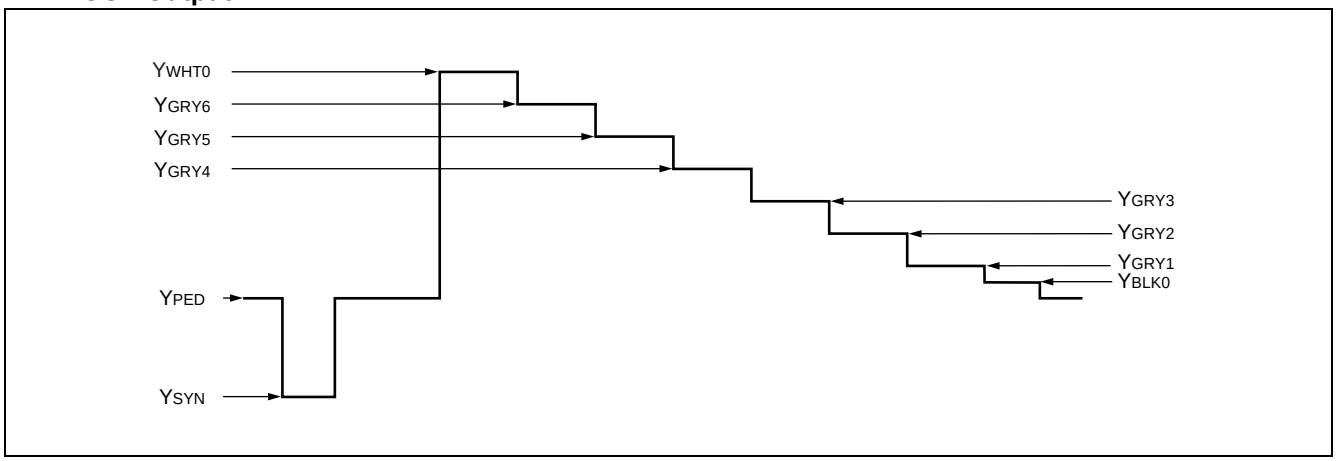
• D (DIGITAL)

Color code	Comment	Display color signal output pin						Register setting value
		DCOL5	DCOL4	DCOL3	DCOL2	DCOL1	DCOL0	DD (HEX)
15	Level-15	0	0	1	1	1	1	0F
14	Level-14	0	0	1	1	1	0	0E
13	Level-13	0	0	1	1	0	1	0D
12	Level-12	0	0	1	1	0	0	0C
11	Level-11	0	0	1	0	1	1	0B
10	Level-10	0	0	1	0	1	0	0A
9	Level-09	0	0	1	0	0	1	09
8	Level-08	0	0	1	0	0	0	08
7	Level-07	0	0	0	1	1	1	07
6	Level-06	0	0	0	1	1	0	06
5	Level-05	0	0	0	1	0	1	05
4	Level-04	0	0	0	1	0	0	04
3	Level-03	0	0	0	0	1	1	03
2	Level-02	0	0	0	0	1	0	02
1	Level-01	0	0	0	0	0	1	01
0	Level-00	0	0	0	0	0	0	00

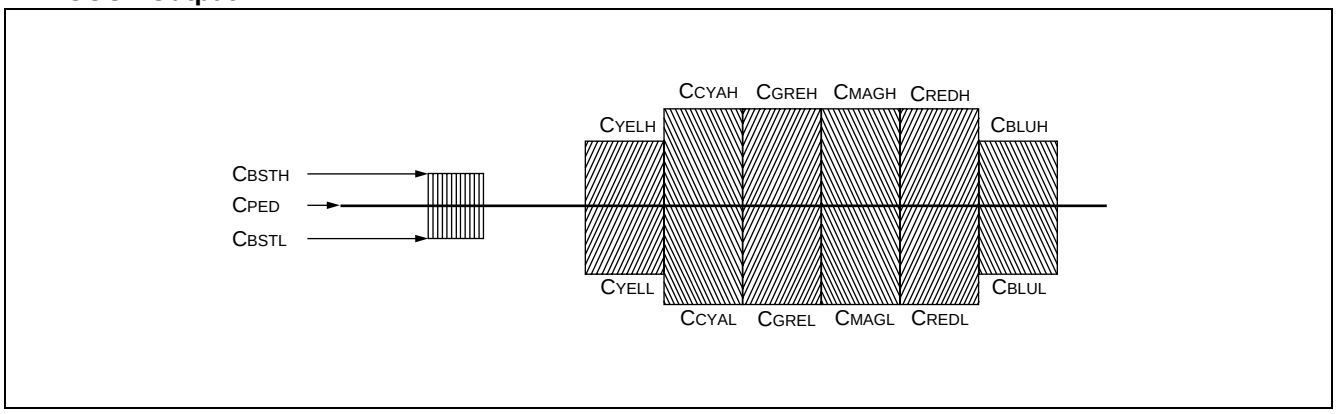
- **VOUT Output**



- **YOUT Output**



- **COUT Output**



Note : Voltage of each output depends on Pallete setting value.

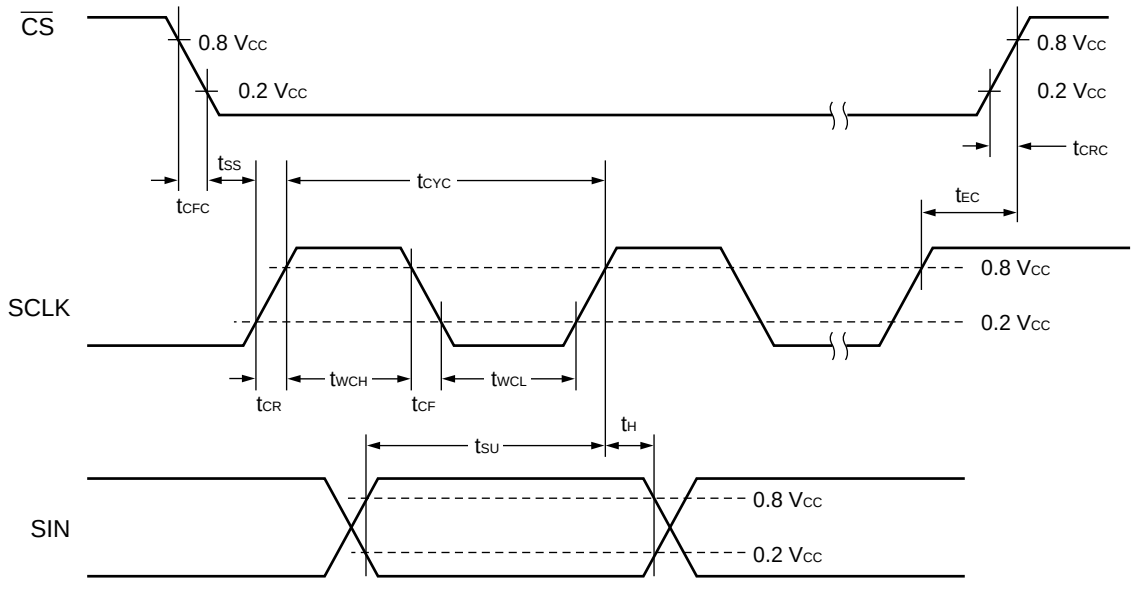
2. AC Characteristics

(Ta = –40 °C to +85 °C, V_{CC} = 5.0 V±10 %, V_{SS} = 0 V)

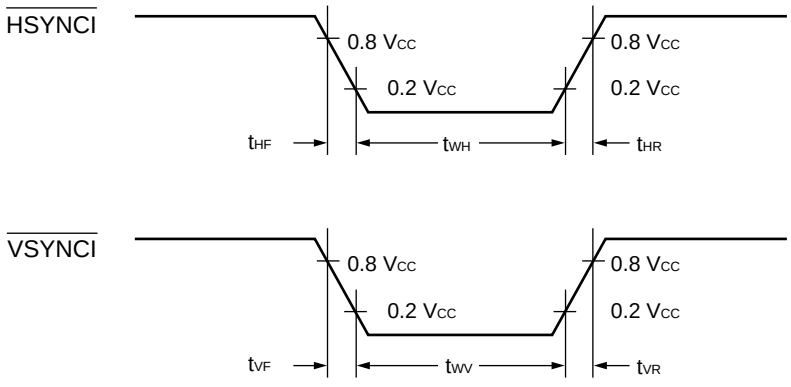
Parameter	Sym-bol	Pin name	Value		Unit	Remarks
			Min	Max		
Shift clock cycle time	t_{CYC}	SCLK	250	—	ns	Refer to “Serial Input Timing”
Shift clock pulse width	t_{WCH}	SCLK	100	—	ns	
	t_{WCL}		100	—	ns	
Shift clock signal rise/fall time	t_{CR}	SCLK	—	200	ns	
	t_{CF}		—	200	ns	
Shift clock start time	t_{SS}	SCLK	100	—	ns	
Data setup time	t_{SU}	SIN	100	—	ns	
Data hold time	t_H	SIN	50	—	ns	
Chip select end time	t_{EC}	$\overline{CS}$	100	—	ns	
Chip select signal rise/fall time	t_{CRC}	$\overline{CS}$	—	200	ns	
	t_{CPC}		—	200	ns	
Horizontal sync signal rise time	t_{HR}	$\overline{HSYNCI}$	—	200	ns	Refer to “Vertical• Horizontal Sync Signal Input Timing”
Horizontal sync signal fall time	t_{HF}	$\overline{HSYNCI}$	—	200	ns	
Vertical sync signal rise time	t_{VR}	$\overline{VSYNCI}$	—	200	ns	
Vertical sync signal fall time	t_{VF}	$\overline{VSYNCI}$	—	200	ns	
Horizontal sync signal pulse width	t_{WH}	$\overline{HSYNCI}$	4.0	8.0	µs	
Vertical sync signal pulse width	t_{WV}	$\overline{VSYNCI}$	1	5	H*	
Field signal pulse width	t_{WF}	FLDI	1	—	H*	Refer to “Field Signal Input Timing”
Reset input pulse width	t_{WR}	$\overline{RESET}$	10	—	µs	Refer to “Reset Signal Input Timing”

* : 1 H is assumed to be one horizontal sync signal period.

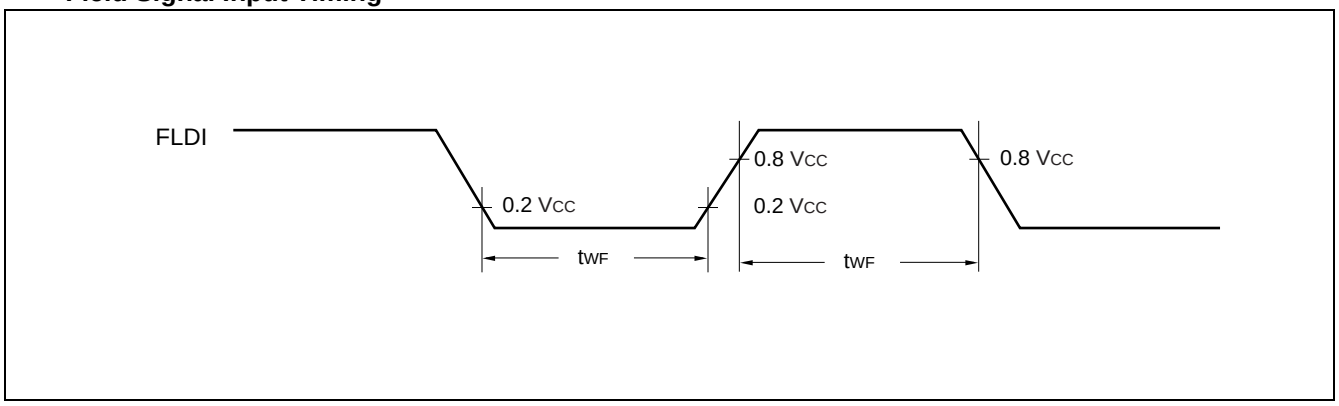
- **Serial Input Timing**



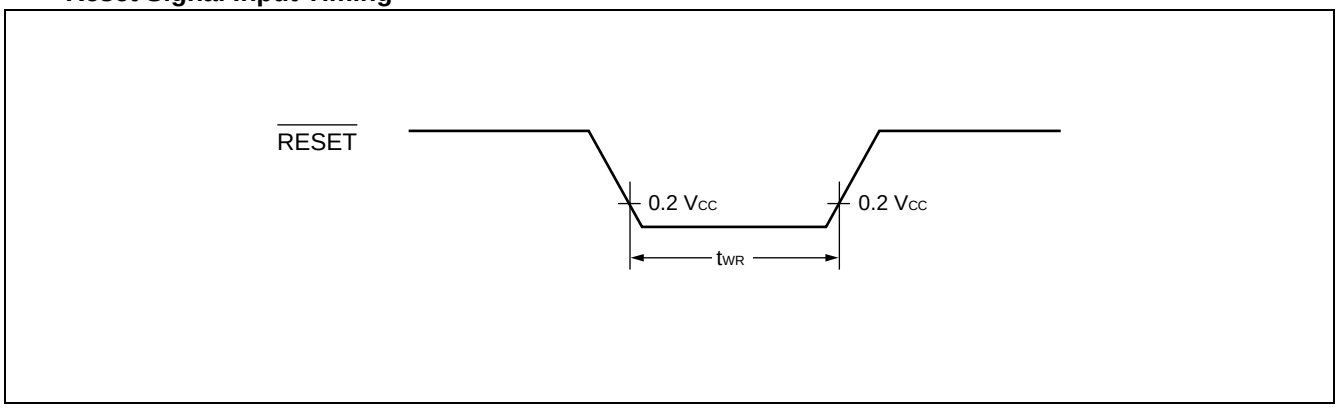
- **Vertical•Horizontal Sync Signal Input Timing**



- **Field Signal Input Timing**



- **Reset Signal Input Timing**



3. Recommended Input Timings

H/V-separated sync signal input timing

Parameter	NTSC	PAL	Unit	Remaeks
Vertical sync signal frequency	60 (59.94)	30	Hz	*1
Vertical sync signal pulse width	1 to 5	1 to 4	H	*2
Horizontal sync signal period	63.492 (63.5555)	64	µs	*1
Horizontal sync signal pulse width	4.19 to 5.71 (4.7±0.1)	4.5 to 4.9	µs	*1

*1 : Parenthesized values are specifications for color information display.

*2 : 1 H is assumed to be one horizontal sync signal period.

4. Clock Timing

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Dot clock for display*	f_{DC}	EXD XD	8	—	20	MHz	
Clock for color burst (NTSC) *	4 f_{SC}	EXS XS	—	14.318185	—	MHz	
Clock for color burst (PAL) *			—	17.734475	—	MHz	

* : Input the signal with a duty cycle of 50%.

5. Output Timings

(1) Horizontal timing

Symbol	NTSC (or simple PAL)	PAL (or simple NTSC)	Remarks
HPS	0	0	Refer to "NTSC/PAL Horizontal Timing".
EQP1E	34	42	
HPE	68	84	
BSTS	76	100	
BSTE	112	140	
HBLKE	143	186	
SEP1S	388	484	
EQP2S	455	568	
EQP2E	489	610	
SEP2S	842	1050	
HBLKS	888	1106	
IHCLR	910	1135 (1137) *	

* : Parenthesized values assume the last raster in each V cycle (field) .

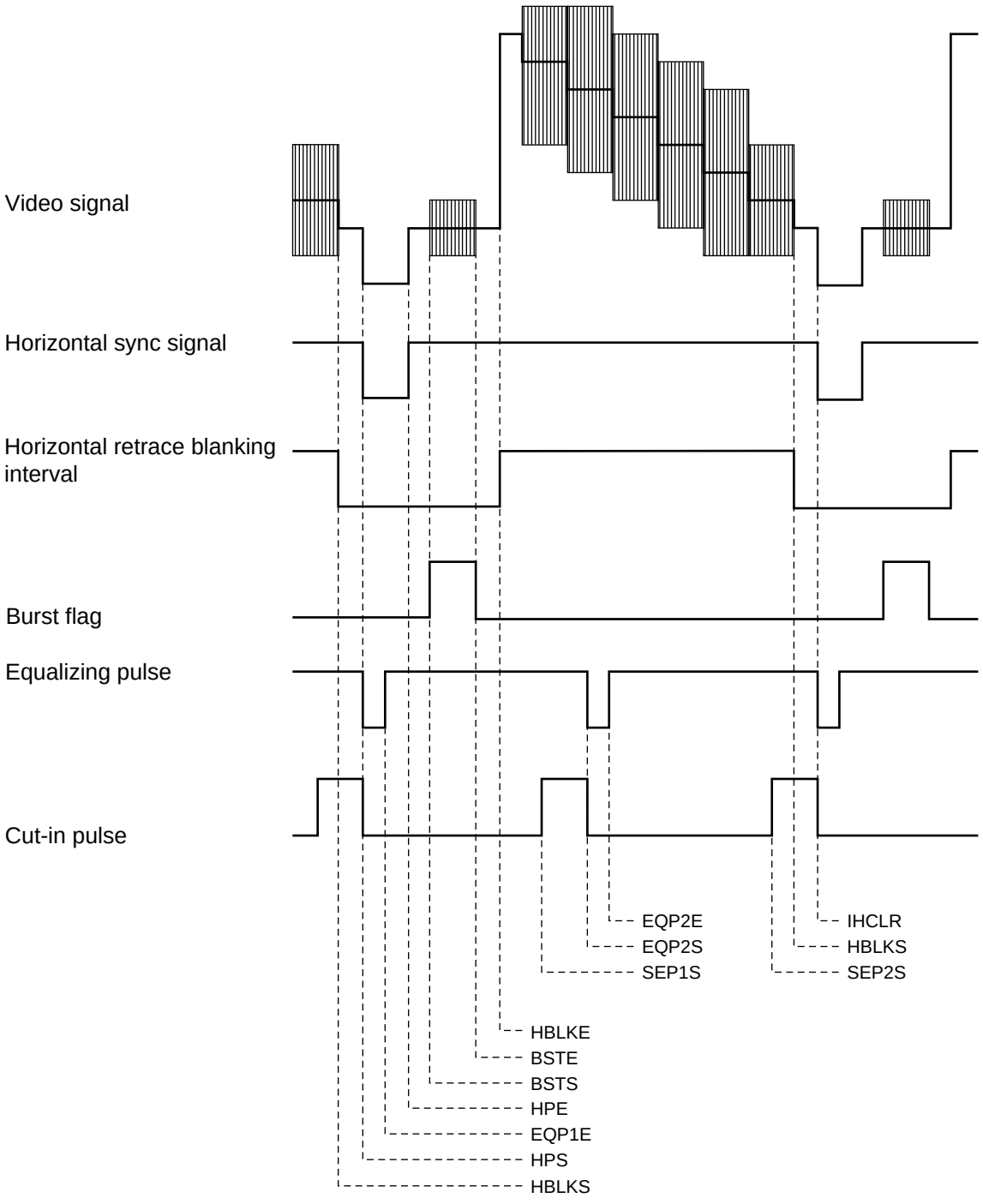
Note : The values in the above list are 4 fsc count values.

(2) Verticl timing

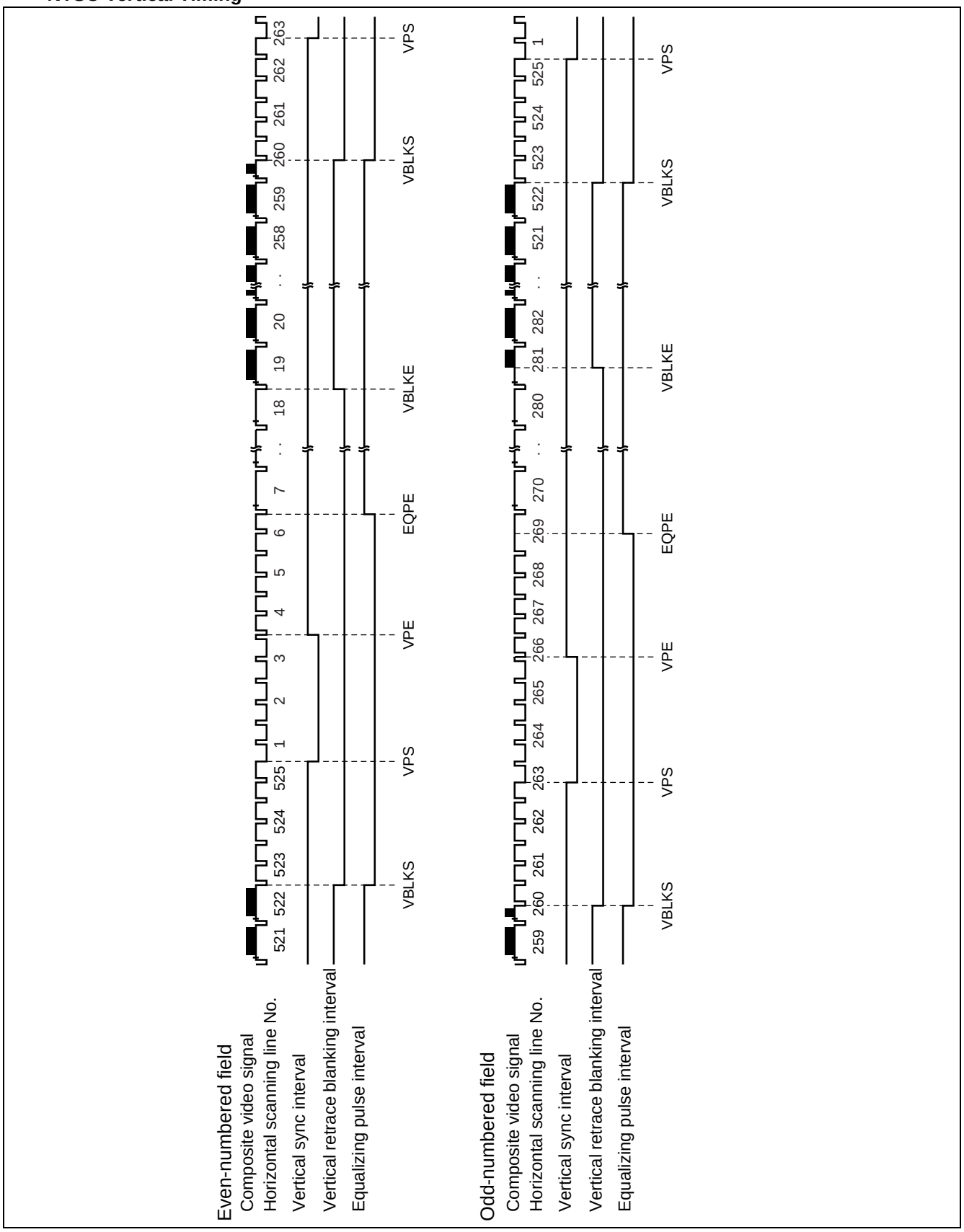
Symbol	NTSC (or simple NTSC)		PAL (or simple PAL)		Remarks
	Interlaced	Non interlaced	Interlaced	Non interlaced	
VPS	0	0	0	0	Refer to "NTSC Vertical Timing" and "PAL Vertical Timing".
VPE	6	6	5	5	
EQPE	12	12	10	10	
VBLKE	36	36	45	45	
VBLKS	519	519	620	620	
VPS	525	526	625	624	

Note : The values in the about list are 1/2 H count values. (1 H is assumed to be one horizontal sync signal period.)

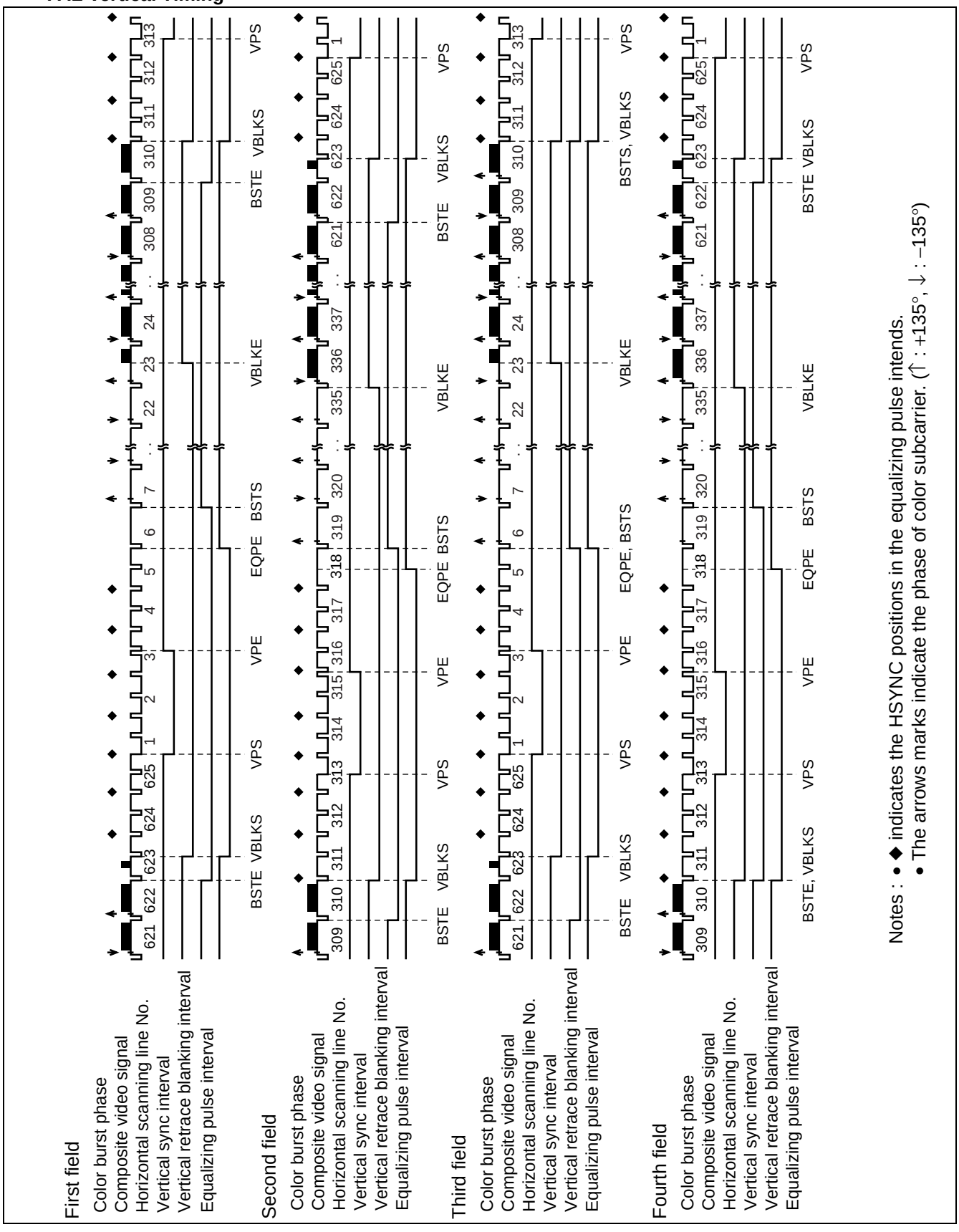
- **NTSC/PAL Horizontal Timing**



- **NTSC Vertical Timing**



- **PAL Vertical Timing**



■ COMMAND LIST

Command no.	Command code/data													Function
	15 to 12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0000	AY3	AY2	AY1	AY0	FL	0	AX5	AX4	AX3	AX2	AX1	AX0	VRAM write address setting
1	0001	MS1	MS0	MM1	MM0	MB3	MB2	MB1	MB0	MC3	MC2	MC1	MC0	Character data setting 1
2	0010	MR	MG	MBL	M8	M7	M6	M5	M4	M3	M2	M1	M0	Character data setting 2
3	0011	LHS	LW2	LW1	LW0	LFD	LFC	LFB	LFA	LF3	LF2	LF1	LF0	Line control data setting 1
4	0100	LDS	0	LG1	LG0	LD	LE	LM1	LM0	L3	L2	L1	L0	Line control data setting 2
5-0	0101	0	0	0	0	SDS	UDS	0	DSP	0	0	0	0	Screen output control 1
5-1	0101	0	1	FM1	FM0	BT1	BT0	BD1	BD0	0	0	0	0	Screen output control 1
5-2	0101	1	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Vertical display position control
5-3	0101	1	1	0	X8	X7	X6	X5	X4	X3	X2	X1	X0	Horizontal display position control
6-0	0110	0	0	0	0	0	HB2	HB1	HB0	0	HA2	HA1	HA	Character vertical size control
6-1	0110	0	1	0	0	BH3	BH2	BH1	BH0	BS3	BS2	BS1	BS0	Shaded background frame color control
6-2	0110	1	0	TC	HC	TC3	TC2	TC1	TC0	HC3	HC2	HC1	HC0	Transparent/semi-transparent colors control
6-3	0110	1	1	GF	GC	GF3	GF2	GF1	GF0	GC3	GC2	GC1	GC0	Graphic color control
7-3	0111	1	1	1	0	0	0	0	0	U3	U2	U1	U0	Screen background control
8-1	1000	0	1	SD1	SD0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0	Sprite character control 1
8-2	1000	1	0	1	SBL	0	SH2	SH1	SH0	0	0	0	0	Sprite character control 2
9-0	1001	0	0	SY9	SY8	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0	Sprite character control 3
9-1	1001	1	0	SX9	SX8	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0	Sprite character control 4

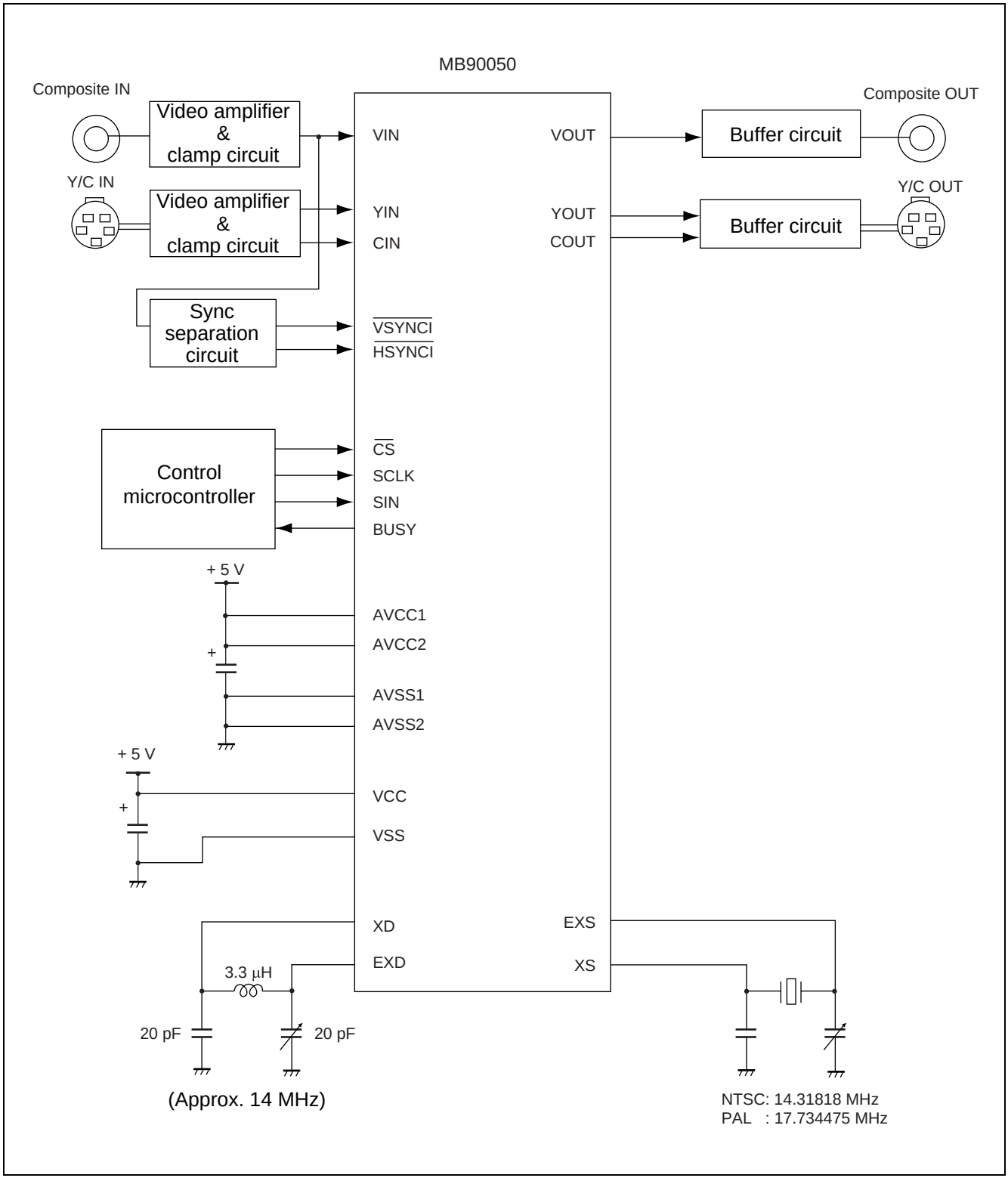
(Continued)

(Continued)

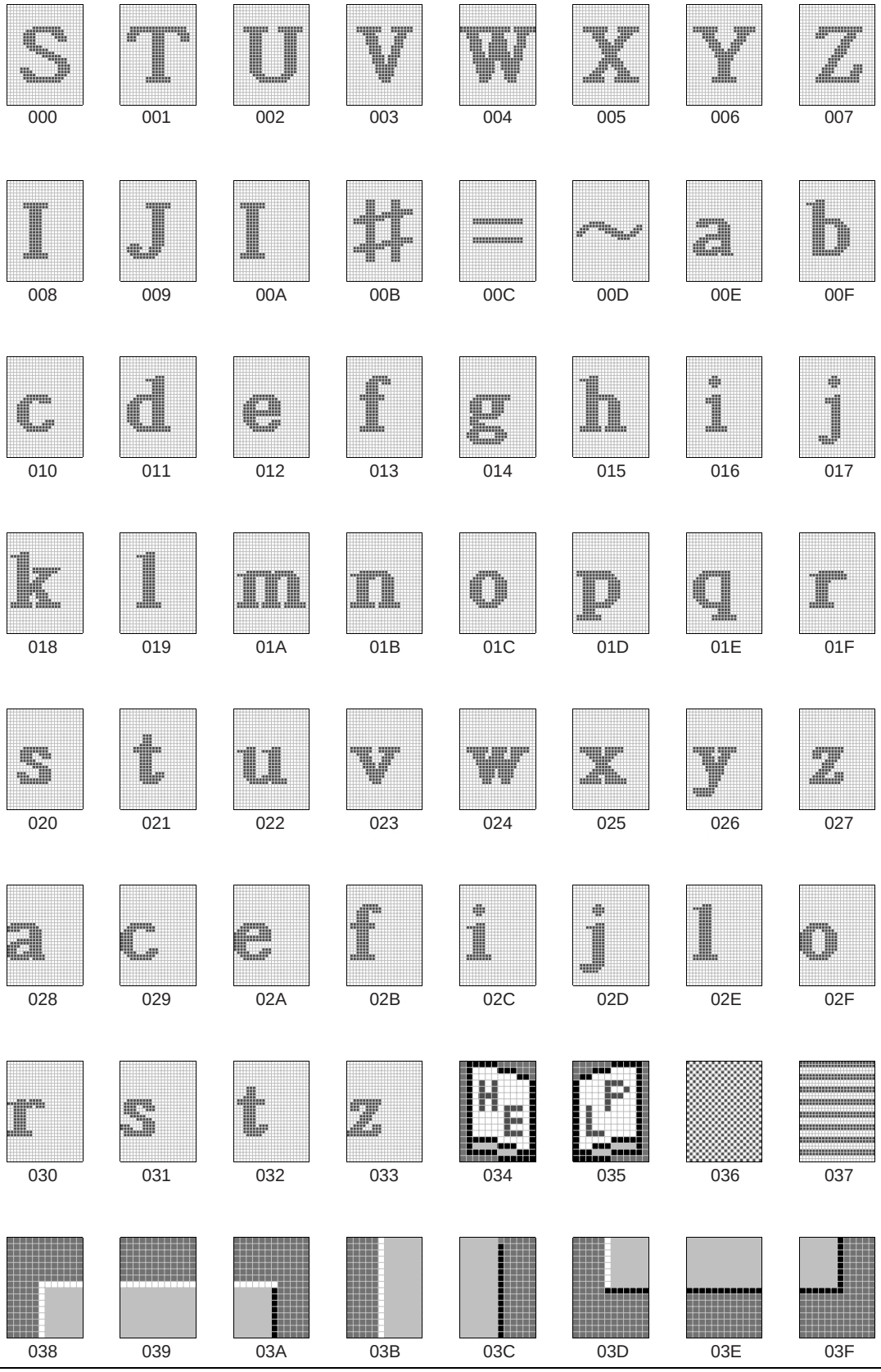
Command no.	Command code/data													Function
	15 to 12	11	10	9	8	7	6	5	4	3	2	1	0	
11-0	1011	0	0	FDS	FDC	MC	NP2	NP1	NP0	IN1	IN0	IE1	IE0	Sync control 1
11-1	1011	0	1	0	0	VIX	HIX	0	0	VHE	HE	0	0	Sync control 2
11-3	1011	1	1	0	0	0	H2	H1	H0	0	F2	F1	F0	Sync detection control
12-0	1100	0	0	STO	BUO	VSO	HSO	CSO	VBO	FDO	DHO	DBO	DCO	Output pin control 1
12-1	1100	0	1	STX	BUX	VOX	HOX	COX	VBX	FDX	DHX	DBX	DCX	Output pin control 2
12-2	1100	1	0	STU	BUU	VSU	HSU	CSU	VBU	FDU	0	0	0	Output pin control 3
12-3	1100	1	1	CKO	FSO	CKS	FSS	0	0	PO3	PO2	PO1	PO0	Output pin control 4
13-0	1101	0	0	0	PLV	PLY	PLC	PLM	PLD	PL3	PL2	PL1	PL0	Color palette setting
13-1	1101	1	AA2	AA1	AA0	0	0	AD5	AD4	AD3	AD2	AD1	AD0	Analog level control
14-0	1110	0	0	0	0	0	0	0	FRS	0	0	FA1	FA0	Font RAM setting 1
14-1	1110	0	1	0	0	0	0	0	0	0	FR2	FR1	FR0	Font RAM setting 2

Note : When a reset signal is input (L level signal input to $\overline{\text{RESET}}$ pin) , the screen output control 1 (command 5 to command 0) bits (SDS, UDS and DSP) and the output pin control 1 to 4 (command 12-0 to command 12-3) bits are initialized to “0”.The color palette setting (command 13-0) and analog level control (command 13-1) bits are internally set to their predetermined initial values.The contents of other register bits, VRAM and font RAM are undefined. After reset input (release) is completed, set all command and font RAM settings.

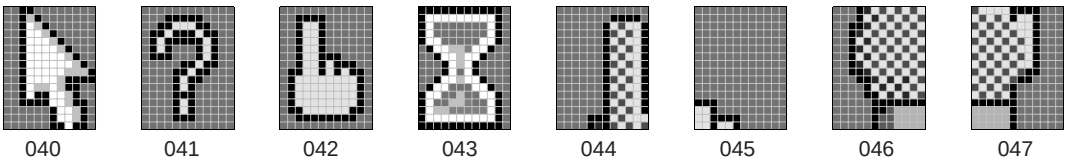
■ SAMPLE CIRCUIT

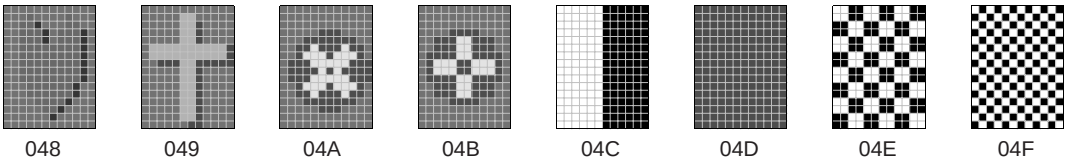


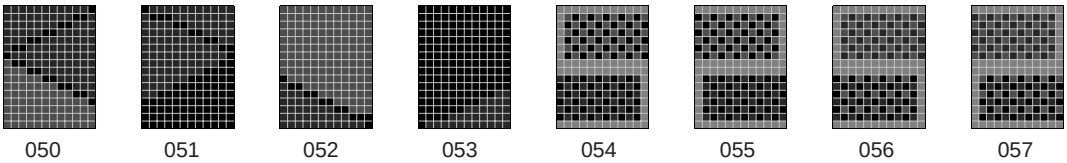
■ MB90050-001 FONT DATA (MB90050-001 is typical product.)

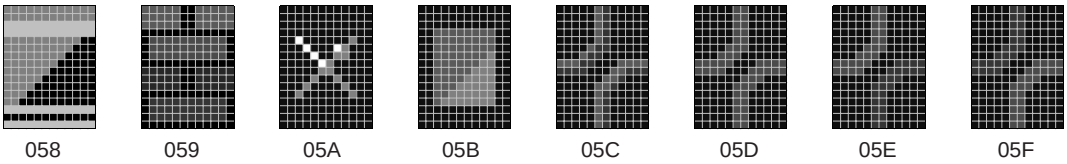


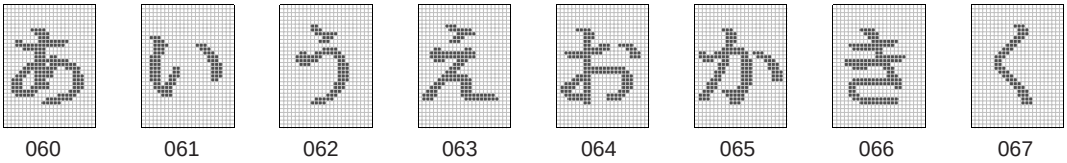
(Continued)

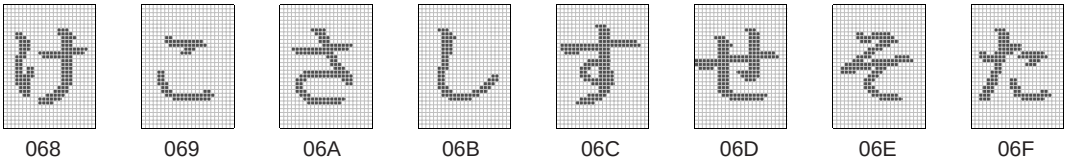

040 041 042 043 044 045 046 047

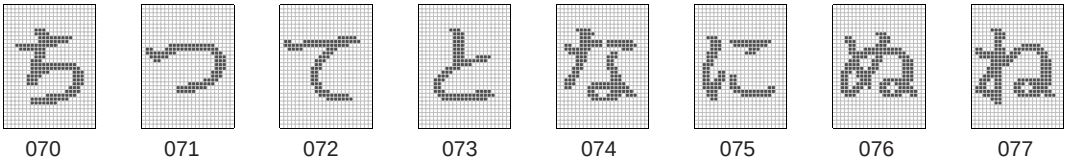

048 049 04A 04B 04C 04D 04E 04F


050 051 052 053 054 055 056 057


058 059 05A 05B 05C 05D 05E 05F


060 061 062 063 064 065 066 067


068 069 06A 06B 06C 06D 06E 06F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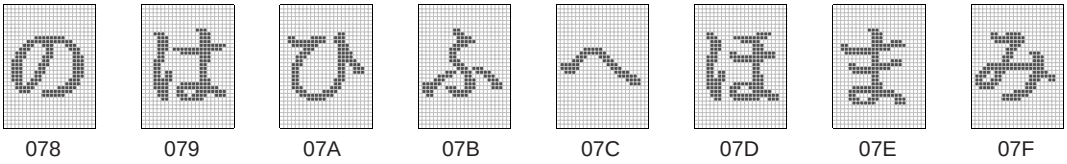
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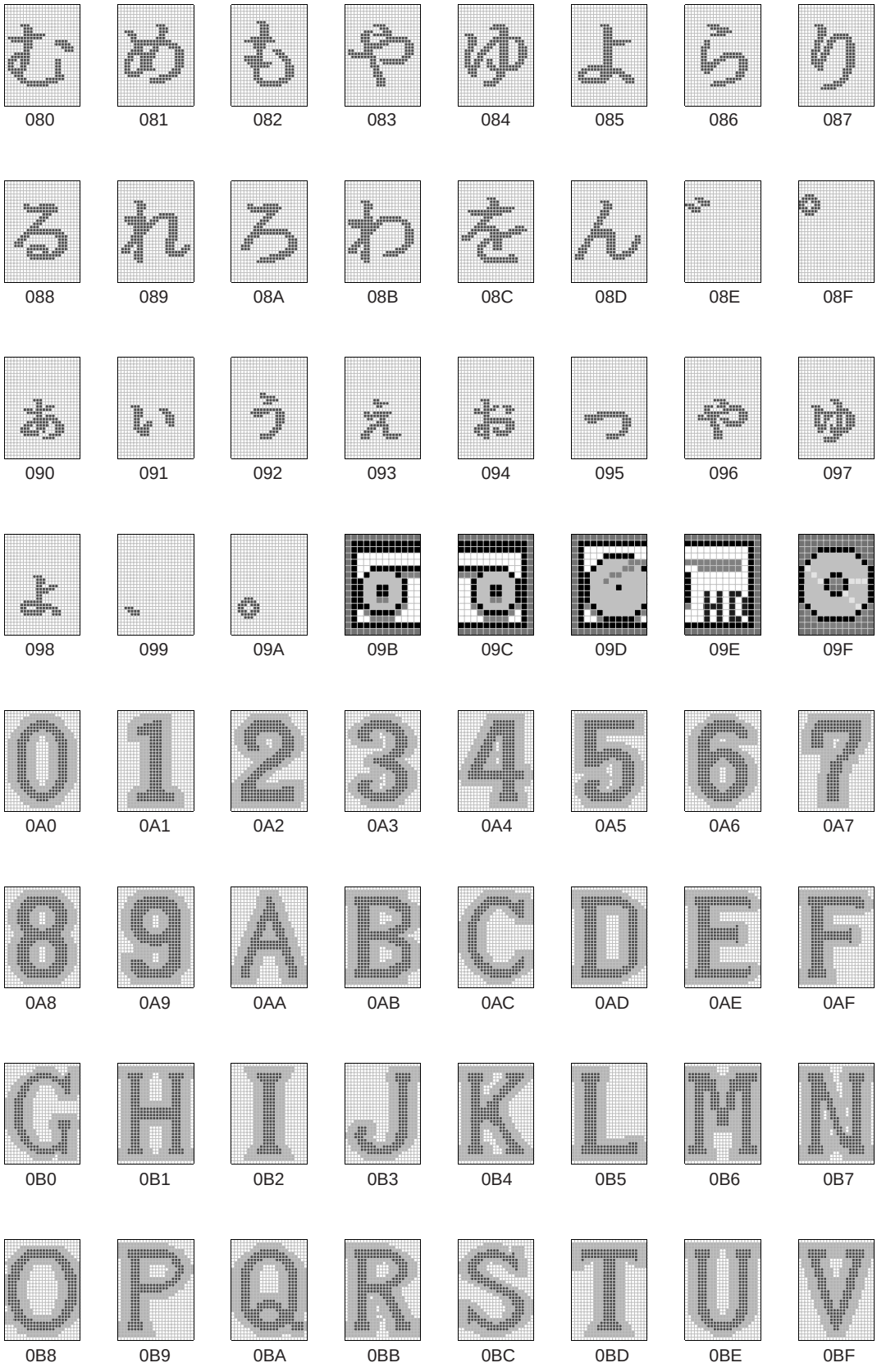
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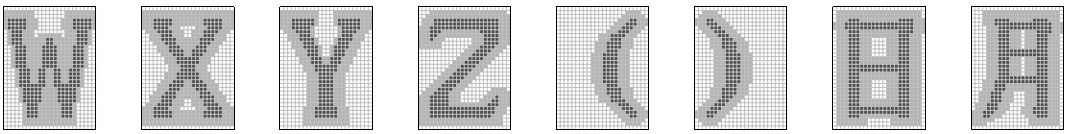
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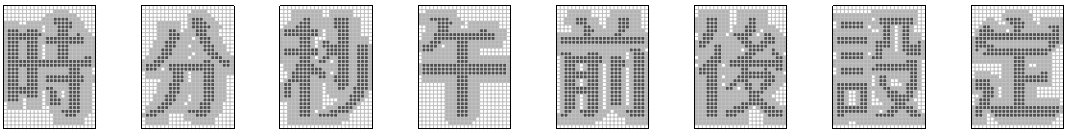
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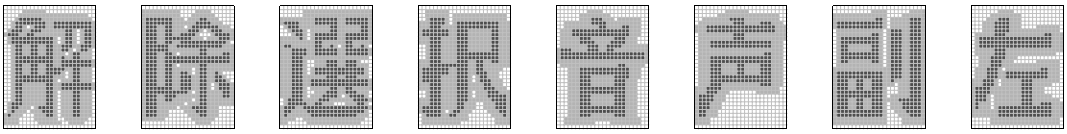
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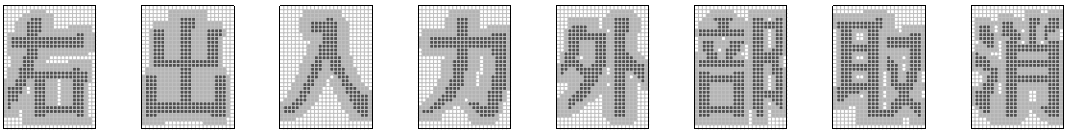
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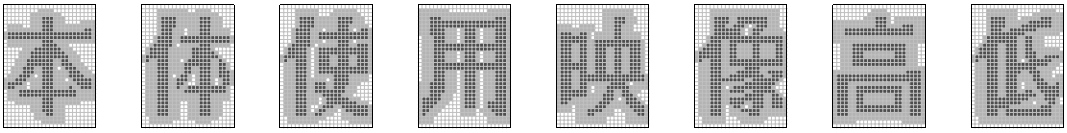
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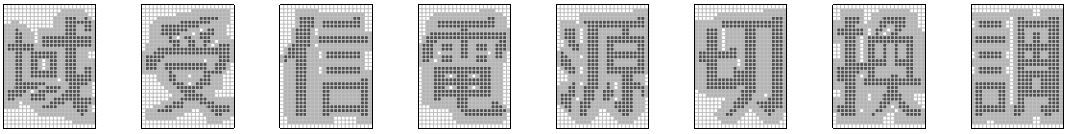
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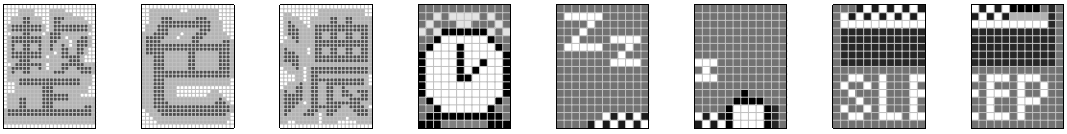
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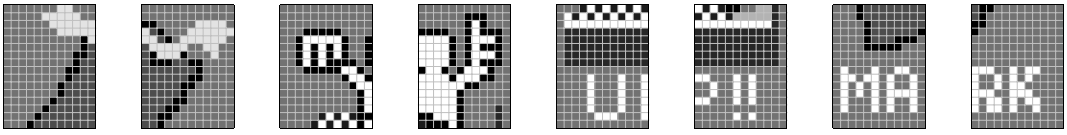
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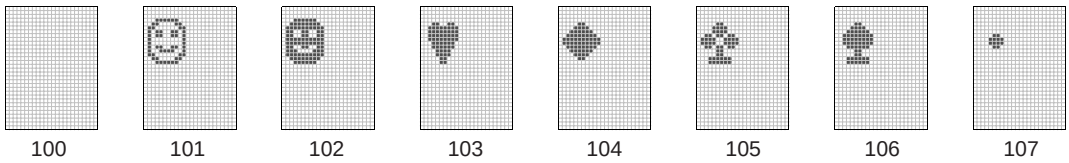
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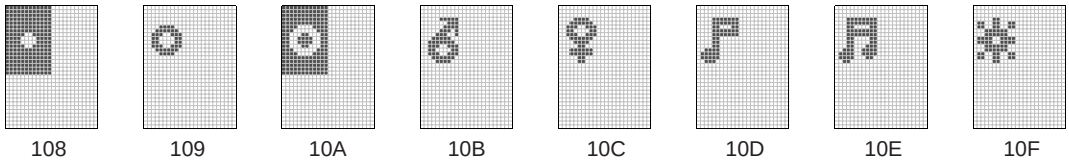
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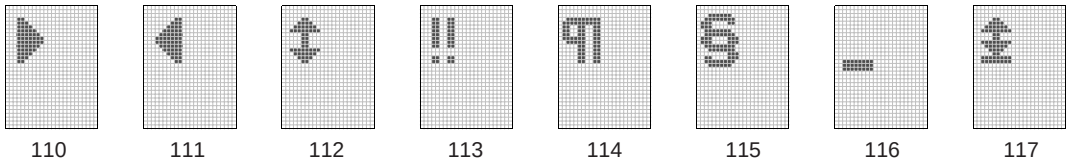
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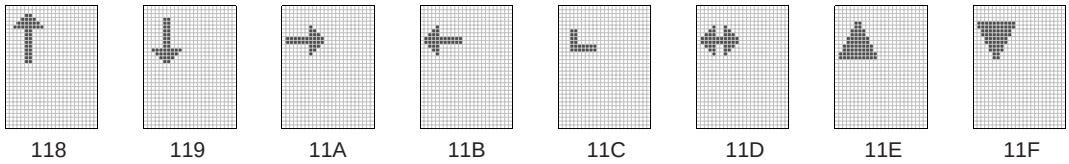
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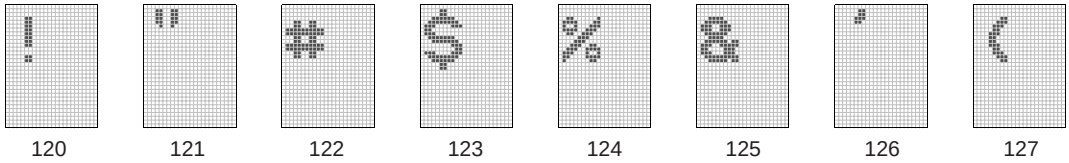
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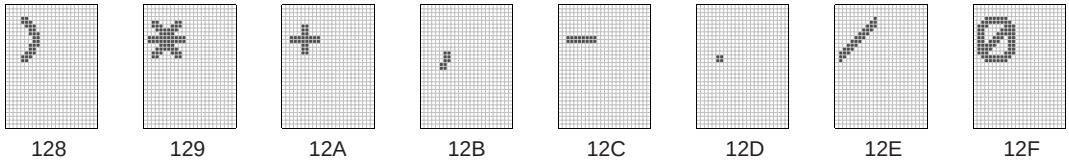
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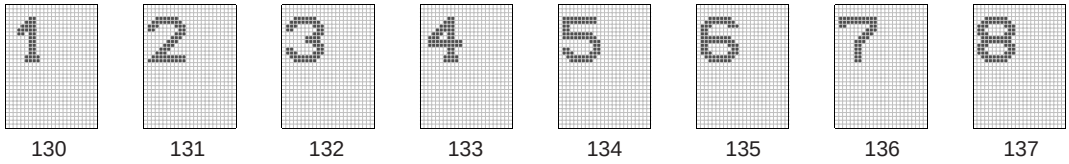
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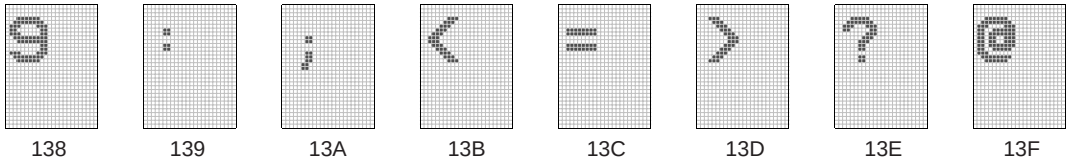
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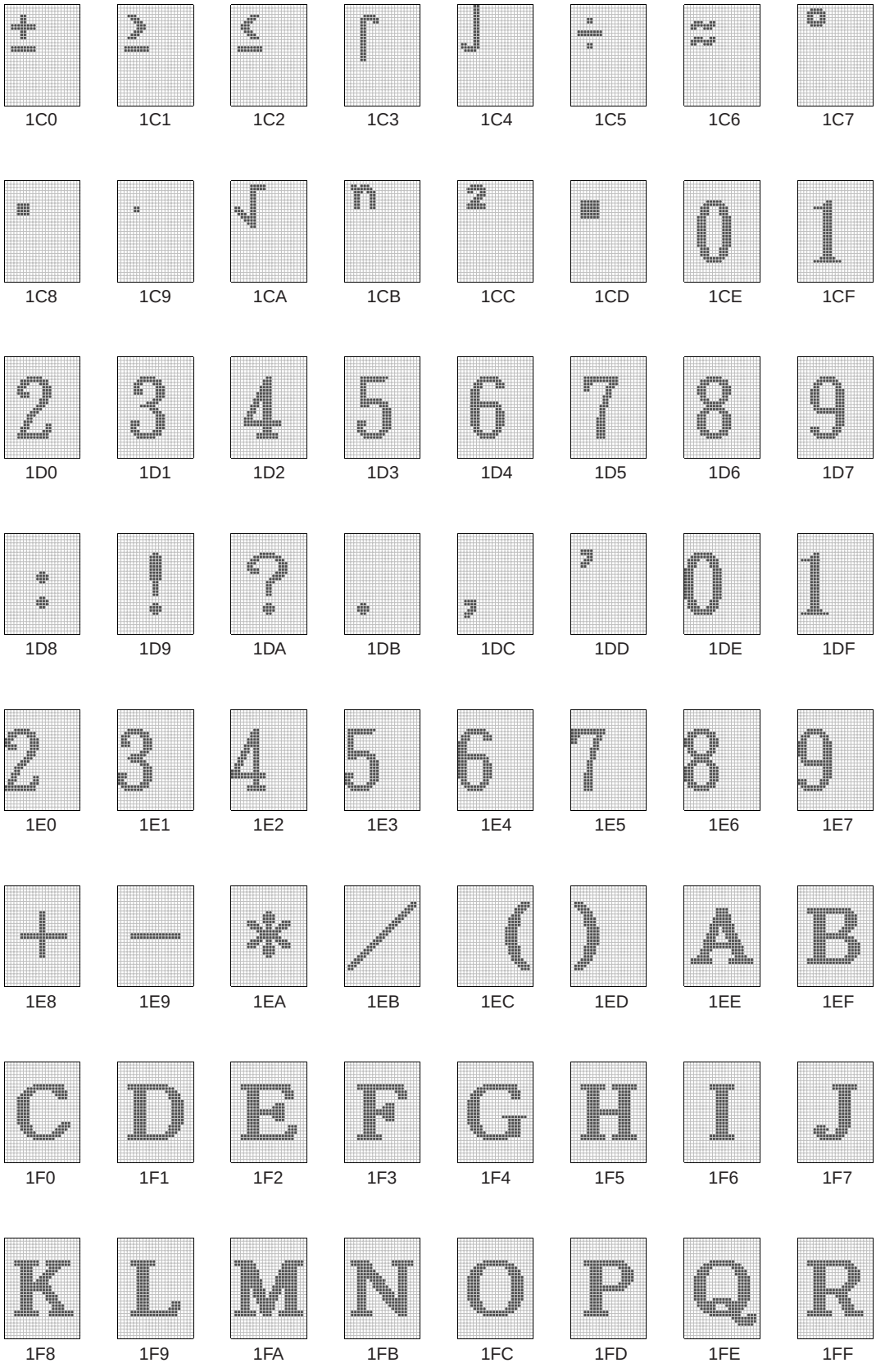
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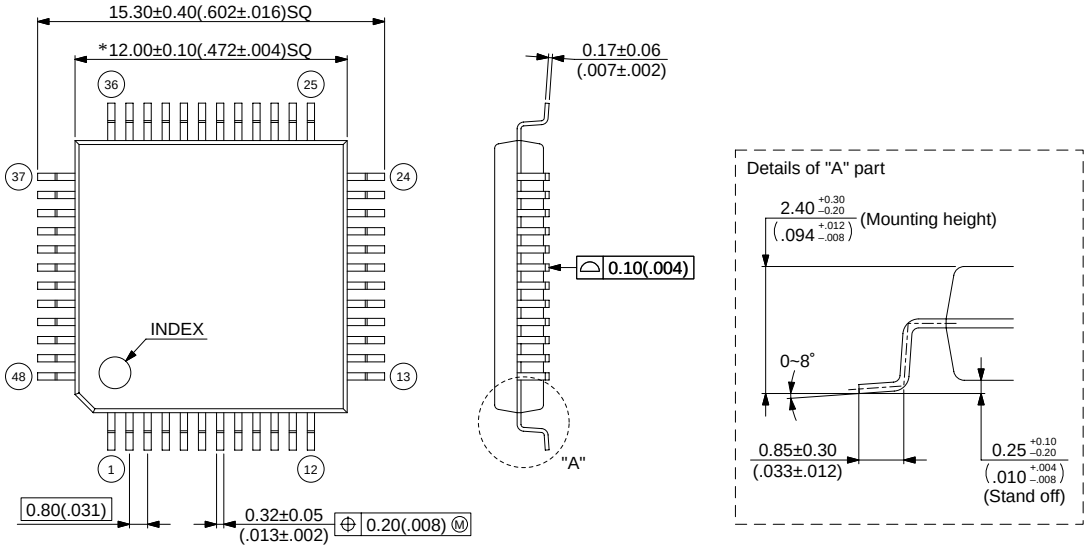
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90050PF	48-pin, plstic QFP (FPT-48P-M15)	

■ PACKAGE DIMENSION

48-pin, plstic QFP
(FPT-48P-M15)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)

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